

DATA SHEET

74F656A

Octal buffer/driver with parity,
non-inverting (3-State)

Product specification
Supersedes data of 1991 Jul 17
IC15 Data Handbook

2000 Jun 30

Octal buffer/driver with parity, non-inverting (3-State)

74F656A

FEATURES

- Significantly improved AC performance over 74F656
- High impedance NPN base input for reduced loading (40µA in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40µA vs. FAST std of 600µA)
- 74F656A combines 74F244 and 74F280A functions in one package
- Non-inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300mil) package
- Inputs on one side and outputs on the other side simplifies PC board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (−40°C to +85°C)

DESCRIPTION

The 74F656A is an octal buffer and line driver with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F656A	6.5ns	64mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	PKG DWG #
24-pin Plastic Slim DIP (300mil)	N74F656AN	I74F656AN	SOT222-1
24-pin Plastic SOL	N74F656AD	I74F656AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

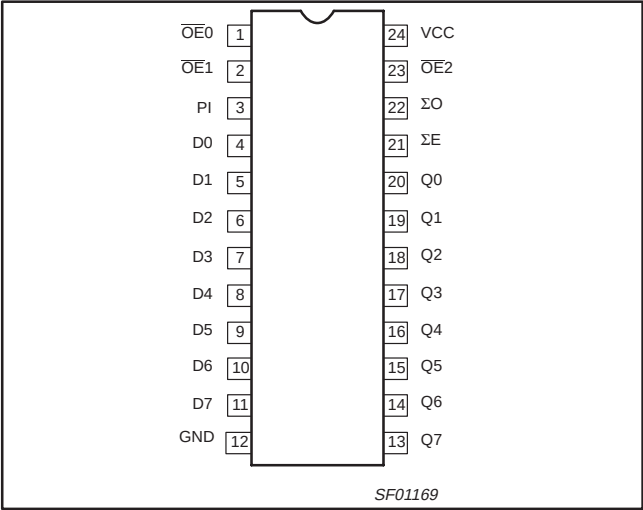
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}0, \overline{OE}1, \overline{OE}2$	Output Enable Inputs (active Low)	1.0/0.033	20µA/20µA
$\Sigma E, \Sigma O$	Parity outputs	750/106.7	15mA/64mA
Q0–Q7	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

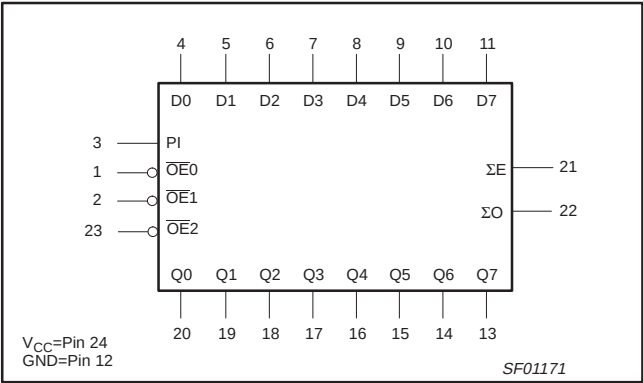
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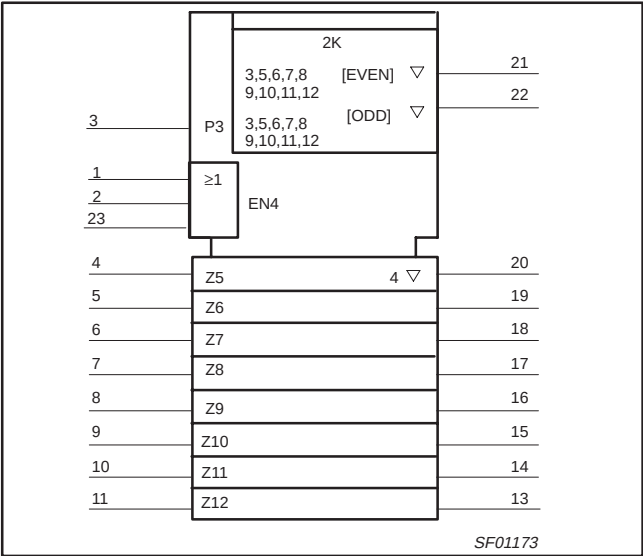
PIN CONFIGURATION



LOGIC SYMBOL



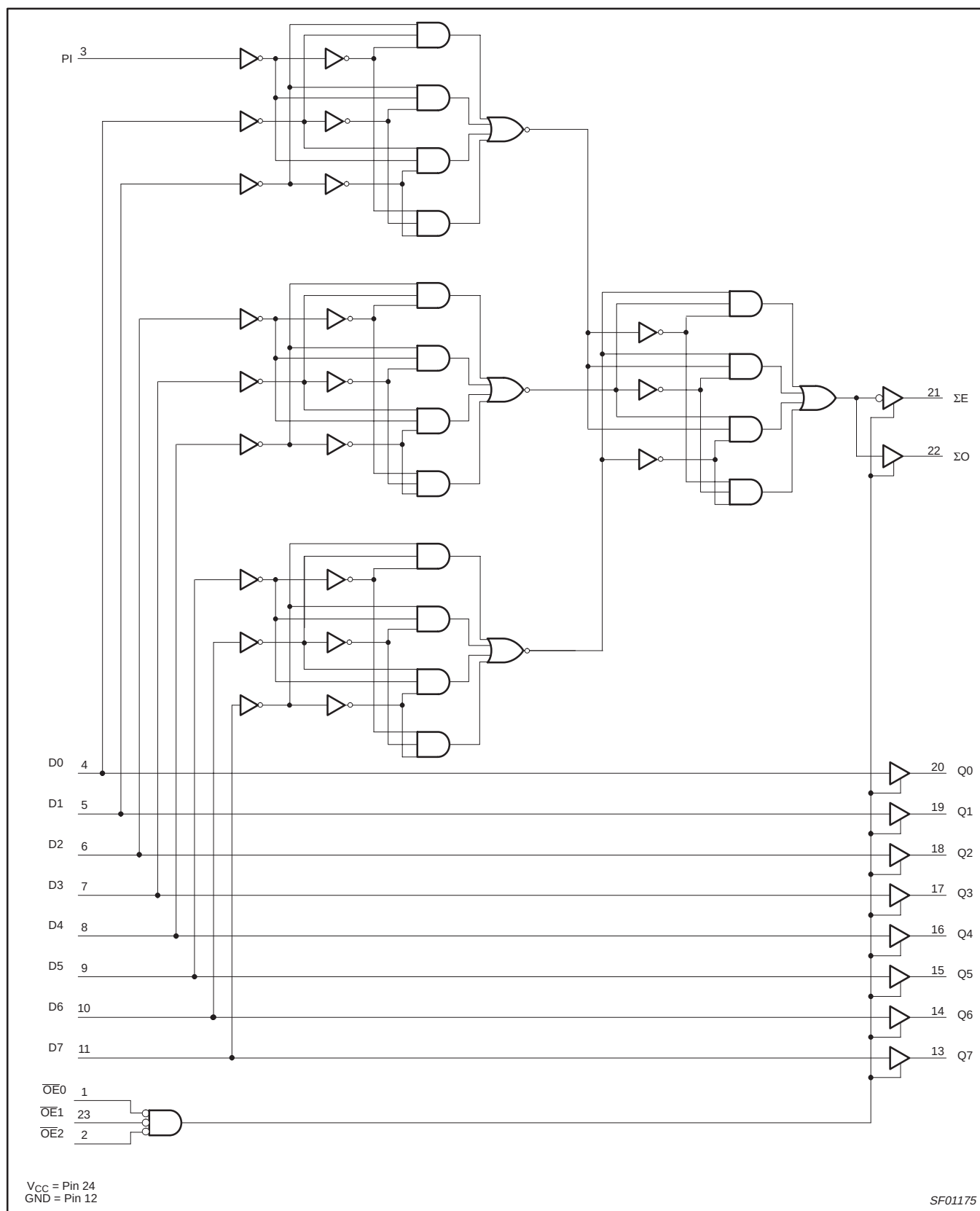
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



Octal buffer/driver with parity, non-inverting (3-State)

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FUNCTION TABLE

INPUTS				OUTPUTS
OE0	OE1	OE2	Dn	Qn
L	L	L	L	L
L	L	L	H	H
H	X	X	X	Z
X	H	X	X	Z
X	X	H	X	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, D0–D7)	ΣE	ΣO
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}n = \text{High}$	Z	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
 Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state		128	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current				64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	–40		85	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS ¹			LIMITS			UNIT
							MIN	TYP ²	MAX	
V _{OH}	High-level output voltage			V _{CC} = MIN, V _{IL} = MAX V _{IH} = MIN	I _{OH} = −3mA	±10%V _{CC}	2.4			V
						±5%V _{CC}	2.7	3.3		V
					I _{OH} = −15mA	±10%V _{CC}	2.0			V
V _{OL}	Low-level output voltage			V _{CC} = MIN, V _{IL} = MAX V _{IH} = MIN	I _{OL} = 64mA	±10%V _{CC}			0.55	V
						±5%V _{CC}		0.42	0.55	V
V _{IK}	Input clamp voltage			V _{CC} = MIN, I _I = I _{IK}				−0.73	−1.2	V
I _I	Input current at maximum input voltage			V _{CC} = 0.0, V _I = 7.0V					100	μA
I _{IH}	High-level input current	Commercial range	Dn	V _{CC} = MAX, V _I = 2.7V					40	μA
			PI, $\overline{\text{OEn}}$						20	μA
		Industrial range	Dn						80	μA
			PI, $\overline{\text{OEn}}$						40	μA
I _{IL}	Low-level input current		Dn	V _{CC} = MAX, V _I = 0.5V					−40	μA
			PI, $\overline{\text{OEn}}$						−20	μA
I _{OZH}	Off-state current High-level voltage applied			V _{CC} = MAX, V _O = 2.7V					50	μA
I _{OZL}	Off-state current Low-level voltage applied			V _{CC} = MAX, V _O = 0.5V					−50	μA
I _{OS}	Short-circuit output current ³			V _{CC} = MAX			−100		−225	mA
I _{CC}	Supply current (total)	I _{CCH}		V _{CC} = MAX				50	80	mA
		I _{CCL}						78	110	mA
		I _{CCZ}						83	90	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

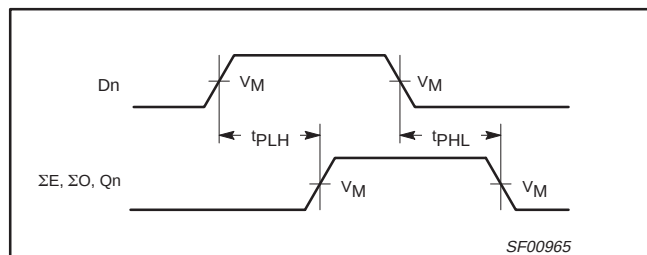
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS								UNIT
			T _{amb} = +25°C, V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		T _{amb} = -40°C to +85°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	2.0 2.5	8.0 9.0	ns ns	
t _{PLH} t _{PHL}	Propagation delay Dn to ΣE, ΣO	Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	4.5 5.5	16.5 18.0	ns ns	
t _{PZH} t _{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	3.5 4.0	7.0 8.0	10.5 11.0	3.5 4.5	11.5 12.0	3.0 4.0	13.0 13.5	ns ns	
t _{PHZ} t _{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	1.5 1.5	10.0 10.0	ns ns	

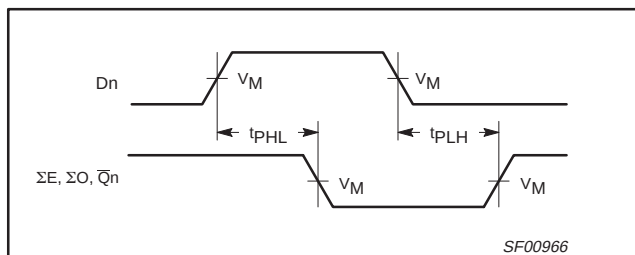
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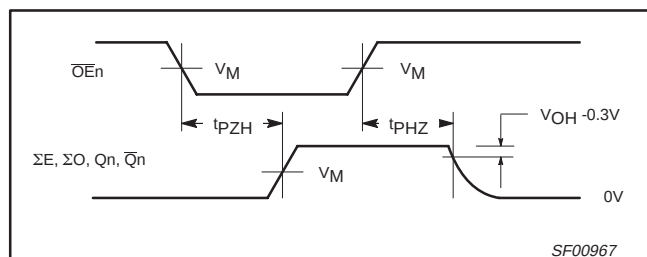
AC WAVEFORMS



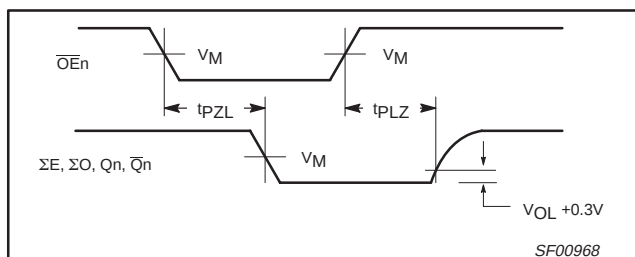
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs

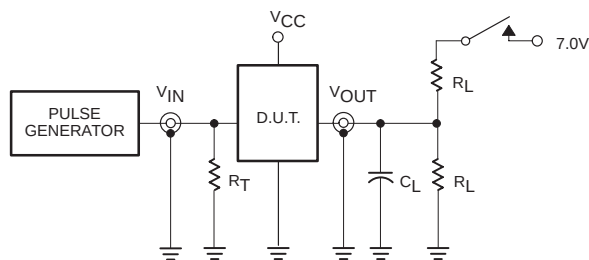


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



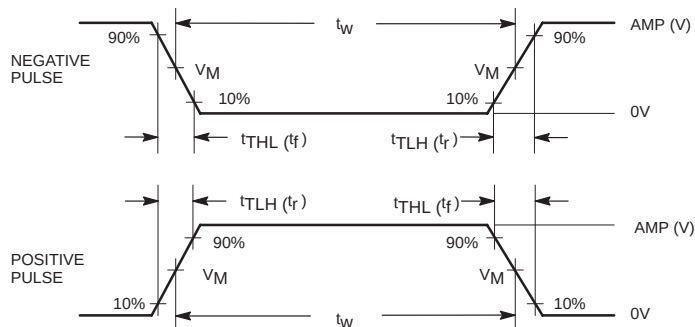
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;
 see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance;
 see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of
 pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

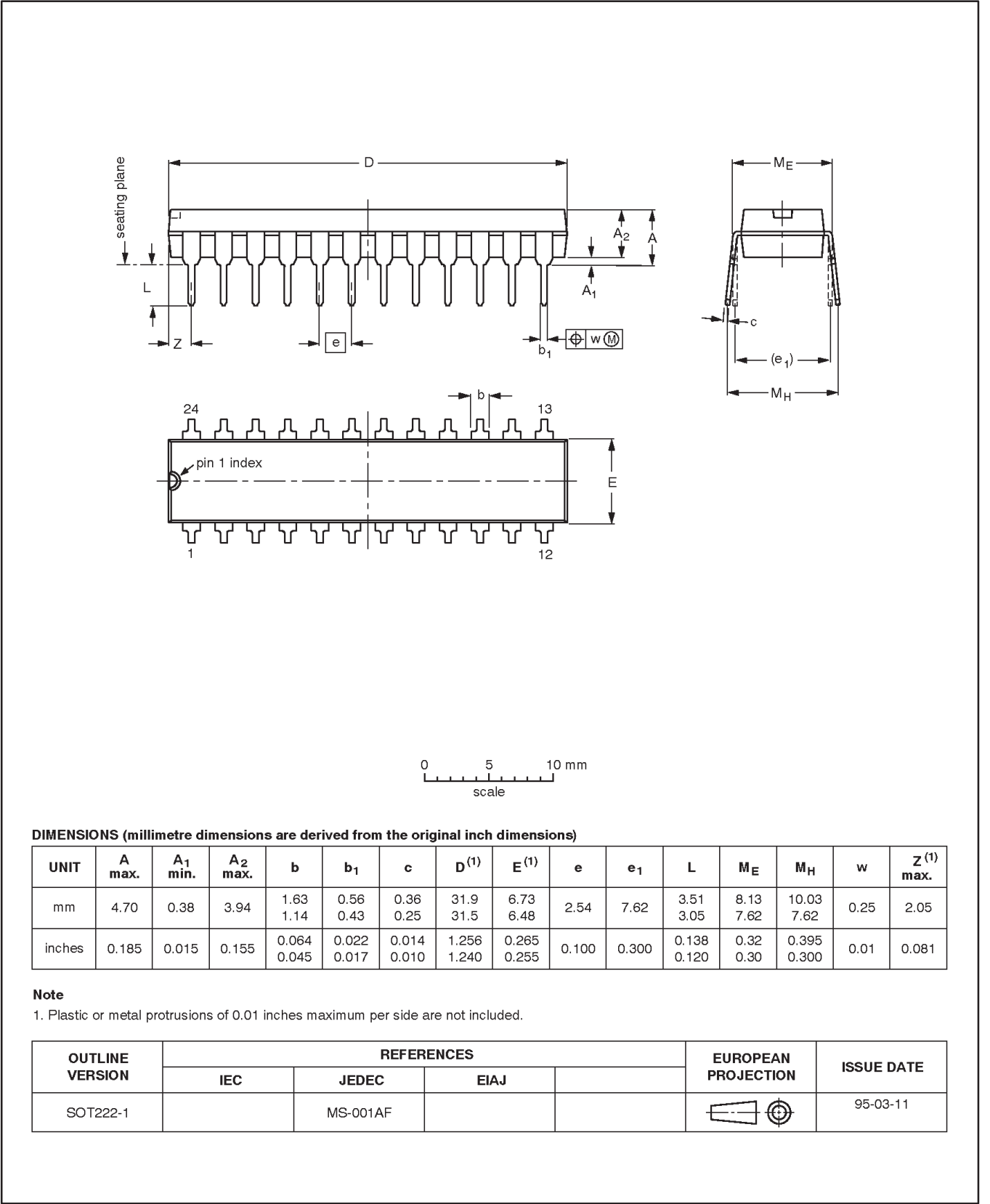
SF00777

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

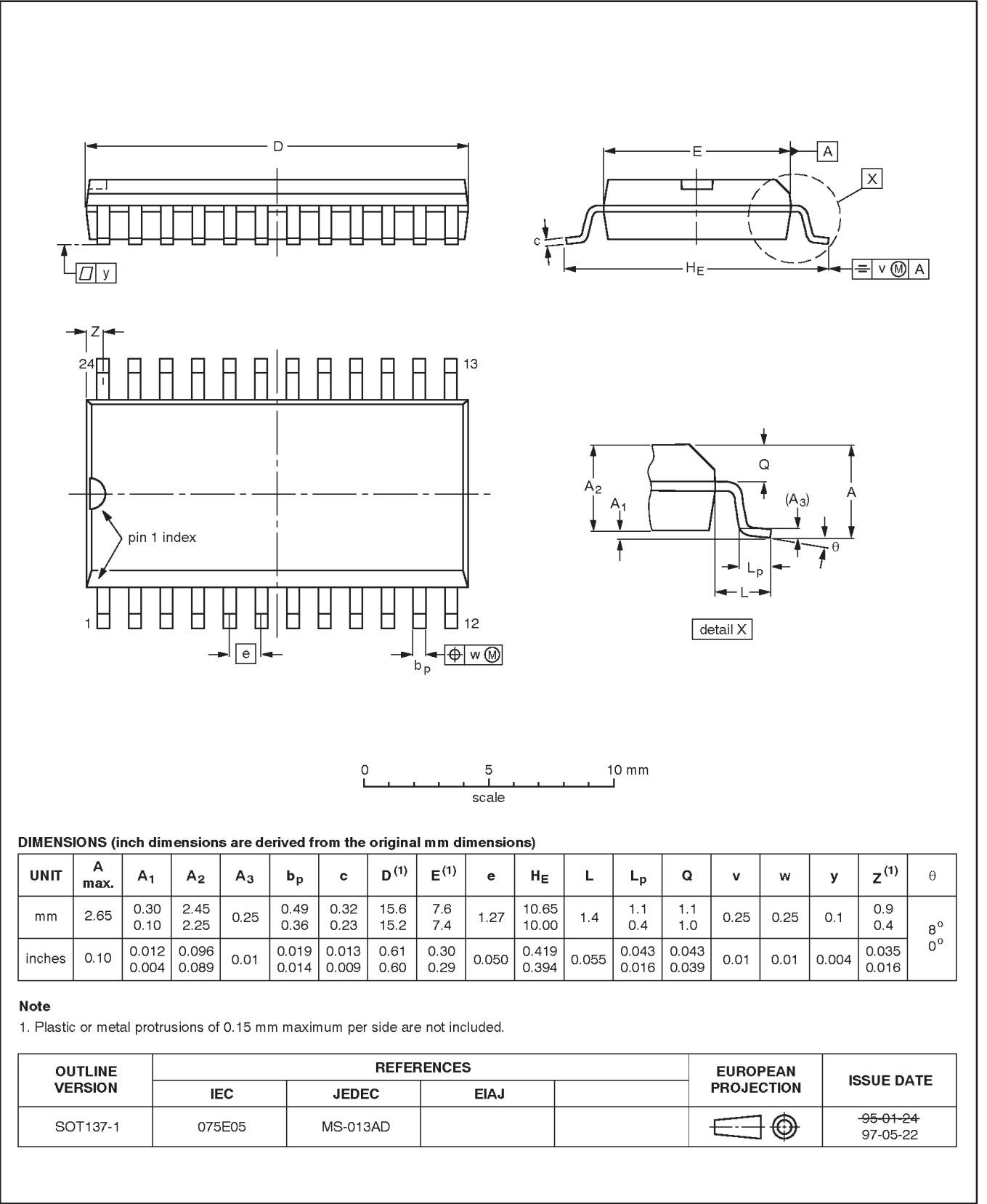


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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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