Power-Up Considerations

INTRODUCTION

When powering up all microcontrollers it is necessary for the power supply voltage to traverse voltage ranges where the device is not guaranteed to operate before the power supply voltage reaches its final state. Since some circuits on the device (logic) will start operating at voltage levels lower than other circuits on the chip (memory), the device may power-up in an unknown state. To guarantee that the device starts up in a known state, it is necessary that it contain a power-up reset circuit. PIC16C5X microcontrollers are equipped with on-chip power-on reset circuitry, which eliminates the need for external reset logic. This circuit will function in most power-up situations where V_{CC} rise time is fast enough (50 ms or less). This application note describes the typical power-up sequence for PIC16C5X microcontrollers. Methods of assuring reset on power-up and after a brownout are discussed and simple, low cost external solutions are discussed for power-up situations where the PIC16C5X's internal circuitry cannot provide the reset.

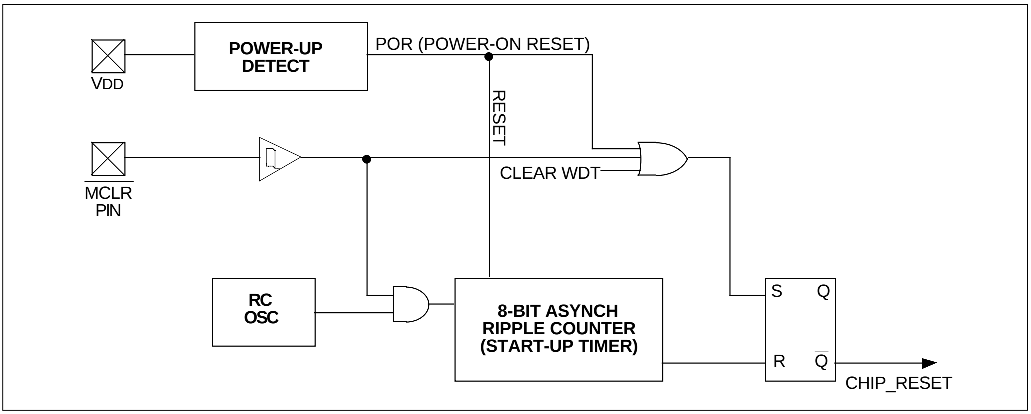
POWER-UP SEQUENCE

The PIC16C5X incorporates complex power-on reset (POR) circuitry on-chip which provides solid, reliable internal chip reset for most power-up situations. To use this feature, the user merely needs to tie $\overline{\text{MCLR}}$ to V_{DD}. A simplified block diagram of the on-chip reset circuitry is shown in Figure 1. On power-up, the reset latch and the start-up timer are reset to appropriate states by the power-on reset (POR). The start-up timer will begin counting once it detects $\overline{\text{MCLR}}$ to be high (i.e., external chip reset goes inactive). After the time-out period, which is typically 18 ms long, the timer will reset the reset latch and thus end the on-chip reset signal.

Figures 2 and 3 are two power-up situations with relative fast rise time on V_{DD}. In Figure 1, V_{DD} is stable when $\overline{\text{MCLR}}$ is brought high (i.e., reset pulse is being provided by external source). The chip actually comes out reset about t_{OST} ms after that, where t_{OST} = oscillator start-up timer. (The timer is called oscillator start-up timer because the time-out was incorporated primarily to allow the crystal oscillator to stabilize on power-up.) In Figure 3, the $\overline{\text{MCLR}}$ and V_{DD} are tied together and clearly the on-chip rest mechanism is being utilized. The V_{DD} is stable before the start-up timer expires and there is no problem with proper reset.

Figure 4, where V_{DD} rise time is much greater than t_{OST} (typically 18 ms) clearly is the potentially problematic situation. The POR (power-on reset) pulse comes when V_{DD} is about 1.5V. Most CMOS logic, including the start-up timer starts functioning between 1.5V to 2.0V. When the start-up timer starts times out, the chip reset is ended and the chip attempts to execute. If by this time the V_{DD} has reached V_{DD} MIN value, then all circuits are guaranteed to function correctly and power-up reset is successful. If, however, the V_{DD} slope was too slow and had not reached V_{DD} MIN, then the chip may or may not function properly.

FIGURE 1 - PIC16C5X INTERNAL RESET CIRCUIT



Power-Up Considerations

FIGURE 2 - EXTERNAL RESET PULSE

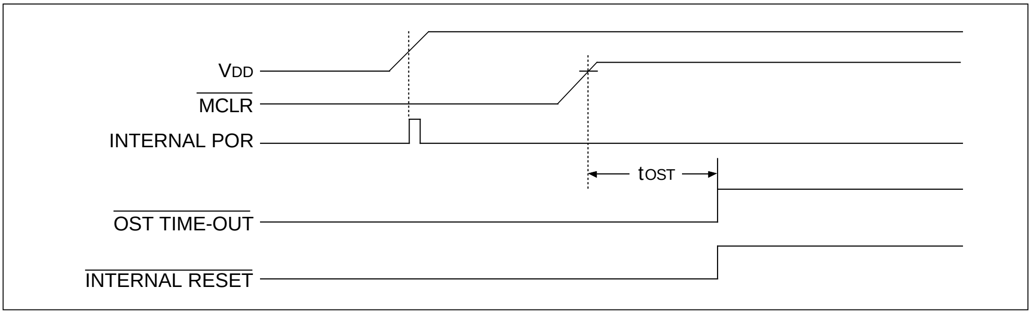


FIGURE 3 - INTERNAL RESET (VDD AND MCLR TIED TOGETHER)

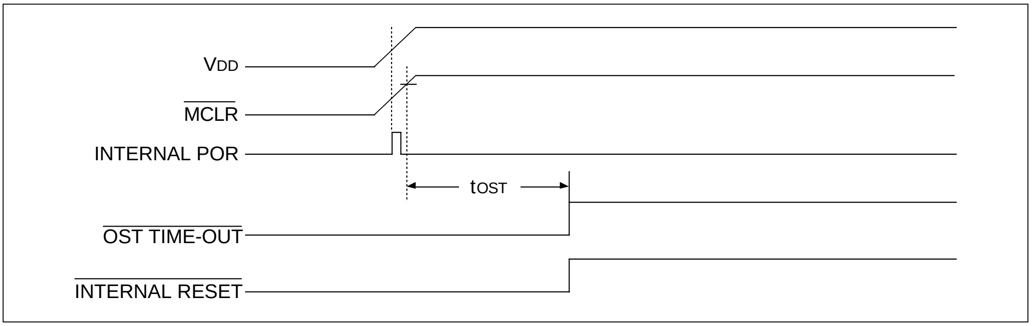
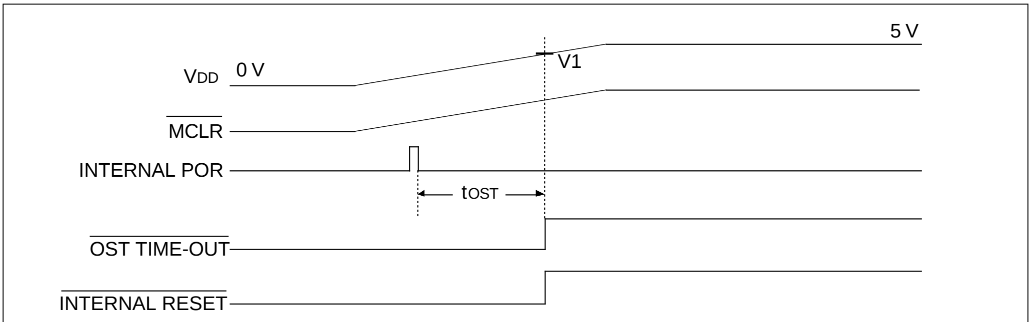


FIGURE 4 - INTERNAL RESET (VDD AND MCLR TIED TOGETHER): SLOW VDD RISE TIME

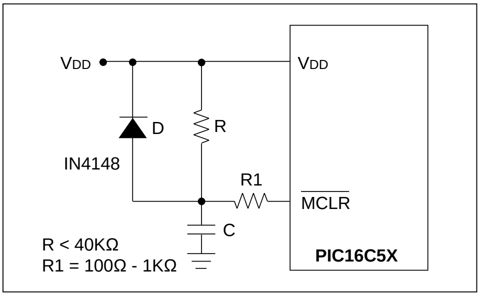


When V_{DD} rises slowly, the internal time-out period expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, $V1 \geq V_{DDMIN}$.

EXTERNAL POWER-ON RESET CIRCUIT

To use power supplies with slow rise times it is necessary to use an external power-on reset circuit such as the one shown in Figure 5. This circuit uses an external RC to generate the reset pulse. The time constant of the RC should be long enough to guarantee that the reset pulse is still present until V_{DD} has reached V_{DD} min. R should be 40K or less to guarantee that the $\overline{MCLR}$ will pull to within 0.2 volts of V_{DD}. (since the leakage spec on $\overline{MCLR}$ is ±5 µA, a resistor larger than 40K may cause input high voltage on this pin to be less than V_{DD} – 0.2V, the required spec). The diode D is used to rapidly discharge the capacitor on power-down. This is very important as a power-up reset pulse is needed after a short power-down (less than the time constant of RC) or after a power spike. The resistor R1 protects against high current flowing into $\overline{MCLR}$ pin from fully charged capacitor C in the event $\overline{MCLR}$ pin breakdown is induced through ESD or EOS. The circuit, however, does not protect against brown-out situations where the power does not drop to zero, but merely dips below V_{DD} MIN. In such a situation, voltage at the $\overline{MCLR}$ pin will not go low enough (i.e., below V_{IL}) to guarantee a reset pulse. The following section presents an example circuit to protect against such brown-outs.

FIGURE 5 - EXTERNAL POWER-ON RESET CIRCUIT



BROWNOUT PROTECTION

In many applications it is necessary to guarantee a reset pulse whenever V_{DD} is less than V_{DD} min. This can be accomplished using a brownout protection circuit such as the one shown in Figure 6. This is a simple circuit that causes a reset pulse whenever V_{DD} drops below the zener diode voltage plus the Vbe of Q1. A 3.3 volt zener will produce a reset pulse whenever V_{DD} drops below about 4 volts. This circuit has a typical accuracy of about ±100 mV. A less expensive, albeit less precise, brown-out circuit is shown in Figure 7. Transistor Q1 turns off when $Vbe = V_{DD} \bullet R1/(R1+R2)$ falls below 0.7 V allowing R3 to pull down $\overline{MCLR}$ input.

FIGURE 6 - BROWNOUT PROTECTION CIRCUIT

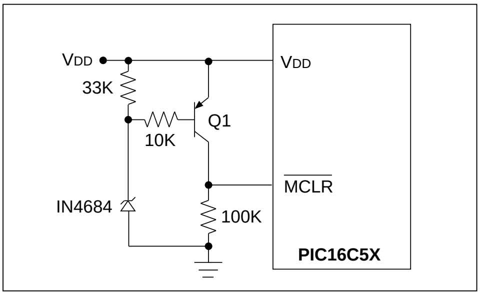
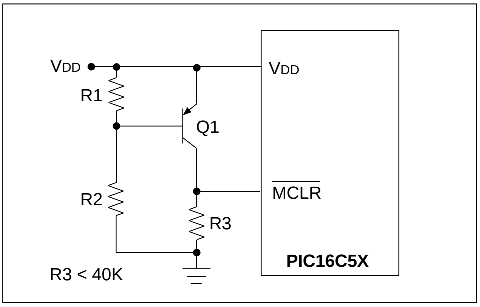


FIGURE 7 - BROWNOUT PROTECTION CIRCUIT



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