TB005

Using External RAM with PIC17CXX Devices

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Introduction

This Technical Brief shows how to connect a PIC17CXX device to external memory. It also provides instructions and calculations to help determine which speeds of SRAM work with which frequency crystal.

System Configuration

Are you doing FFT's? Storing arrays of data? Typically, low speed designs would use EEPROM to hold the data that is being generated. On the other hand, high speed designs need to use static RAM because of the faster access times. External SRAM can easily be integrated with a PIC17CXX device to create the SRAM bank your design requires. Data storage and retrieval is accomplished through table read and table write instructions.

All the equations for lead timing can also be applied to EPROMs.

The first thing you need to know is how much RAM the system requires. Table 1 shows how much external memory can be used with the PIC17CXX family members. The microcontroller is put into extended microcontroller mode which can access both the internal and external memory. Both the internal and external memory is 16-bits wide.

TABLE 1: INTERNAL/EXTERNAL MEMORY

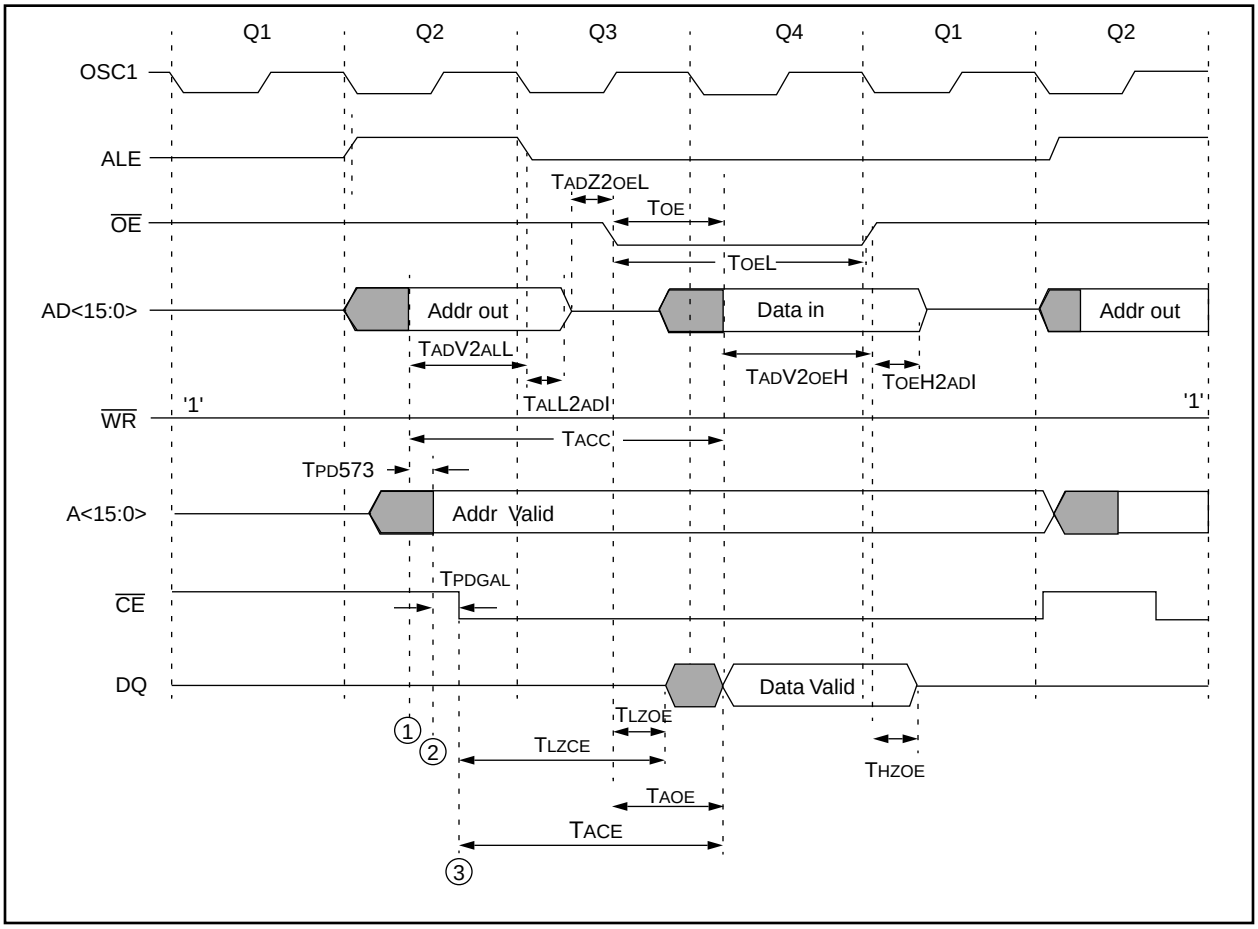
Device		Size (Words)	Address Range
PIC17C42	Internal	2048	0x0000 - 0x07FF
	External	63488	0x0800 - 0xFFFF
PIC17C43	Internal	4096	0x0000 - 0x0FFF
	External	61440	0x1000 - 0xFFFF
PIC17C44	Internal	8192	0x0000 - 0x1FFF
	External	57344	0x2000 - 0xFFFF

The next step is to connect the external SRAM to the PIC17CXX. Appendix A shows the schematic for connecting two MT5C2568 (32Kx8) SRAM devices to a PIC17C43. The MT5C2568 can be obtained from Micron Semiconductor. The only additional hardware required is two latches (74ACT373s or 74ACT573s). Both chips are octal latches but the 74ACT573 has the inputs and the outputs on opposite sides of the chip which makes interfacing to the microcontroller easier.

READ TIMINGS

Now that we know how to connect the hardware, the next step is to determine the speed grade of the SRAM. Let's first take a look at the read timings. Figure 1 shows a combined timing diagram for the read cycle of a PIC17C4X device and the MT5C2568 SRAM.

FIGURE 1: PIC17C4X/MT5C2568 READ CYCLE TIMING DIAGRAM



The value of TACE shows which speed grade of SRAM is required for the read cycle. Figure 1 has three key locations marked that help define TACE. Table 2 summarizes these locations.

TABLE 2: LOCATION MARKER DESCRIPTIONS FOR FIGURE 1

Location	Description	Value	
1	Address Setup Time. This location marks the spot where the address becomes valid out of the PIC17CXX before ALE goes LOW. (Q2 cycle)	0.25 * TCY - 10	time in nanoseconds before the Q3 cycle (TADV2ALL)
2	Propagation delay of the 74ACT573. This is the spot where the address to the SRAM becomes valid. (Q2 cycle)	6	time in nanoseconds before the Q3 cycle (TPD573)
3	Propagation delay of the address decoder. This spot is where the CE signal from the address decoder to the SRAM goes LOW. (Q2 cycle)	TPDGAL	time in nanoseconds before the Q3 cycle

TABLE 3: MEMORY INTERFACE READ REQUIREMENTS

Sym	Characteristic	Min	Typ	Max	Units
TADV2ALL	AD15:AD0 (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	—	—	ns
TALL2ADI	ALE↓ to address out invalid (address hold time)	5*	—	—	ns
TADZ2OEL	AD15:AD0 hi-impedance to $\overline{OE}$↓	10	—	—	ns
TADV2OEH	Data in valid before $\overline{OE}$↑ (data setup time)	35	—	—	ns
TOEH2ADI	$\overline{OE}$↑to data in invalid (data hold time)	0	—	—	ns
TOEL	$\overline{OE}$ pulse width	0.5Tcy - 35	—	—	ns
TOE	Output enable access time ($\overline{OE}$ low to Data Valid)	—	—	0.5TCY - 45	ns
TPD573	Propagation delay input to output	2	6	12	ns
TACC	Address access time	0.75Tcy - 30	—	—	ns
TPDGAL	Propagation delay input to combinatorial output	3	—	7.5 - 25	ns
TLZOE	$\overline{OE}$ to output in Low - Z	0	—	—	ns
TAOE	$\overline{OE}$ access time	—	—	5 - 8	ns
TLZCE	$\overline{CE}$ to output in Low - Z	3	—	—	ns
TACE	$\overline{CE}$ access time	—	—	10 - 25	ns
THZOE	Output disable to output in High - Z	—	—	5 - 7	ns

To determine TACE from Figure 1, the following equation can be used. Each part of the equation is related to a timing parameter or one of the marked locations in Figure 1.

TACE =	0.75 * TCY - 30	- Address access time - TACC
	- 6	- Propagation delay of the 74ACT573 - TPD573
	- TPDGAL	- Propagation delay of the address decoder

Finally, lets find some example speed grades for various crystal frequencies. One thing to remember is that this is only the read timing speed grade. You must also calculate the write timing speed grade. As you can see the speed grade for the SRAM is dependent on the address decoder. Typically, programmable array logic devices such as a 16V8 or a 22V10 are used. The propagation delays of these devices can be anywhere from 5 ns up to 30 ns.

8 MHz (TCY = 500 ns)	**16 MHz (TCY = 250 ns)**	**20 MHz (TCY = 200 ns)**	**25 MHz (TCY = 160 ns)**
TACE = 0.75 * 500 - 30	TACE = 0.75 * 250 - 30	TACE = 0.75 * 200 - 30	TACE = 0.75 * 160 - 30
- 6	- 6	- 6	- 6
- TPDGAL	- TPDGAL	- TPDGAL	- TPDGAL
TACE = 345	TACE = 157.5	TACE = 125	TACE = 90
- 6	- 6	- 6	- 6
- TPDGAL	- TPDGAL	- TPDGAL	- TPDGAL
TACE = 339 - TPDGAL	TACE = 151.5 - TPDGAL	TACE = 119 - TPDGAL	TACE = 84 - TPDGAL

To reduce the total propagation delay of the 74ACT573 and the address decoder, the address/data lines and ALE from the PIC17C4X can be routed to the address decoder. Now the address latches and the address decoding can be performed in parallel.

WRITE TIMINGS

Now that you have determined the read timing speed grade, it is time to calculate the write timing speed grade of the SRAM for your design. Figure 2 shows the combined timings for a write cycle of the PIC17C4X devices and the MT5C2568. Again, there are markings for some key locations which are described in Table 4.

FIGURE 2: PIC17C4X/MT5C2568 WRITE CYCLE TIMING DIAGRAM

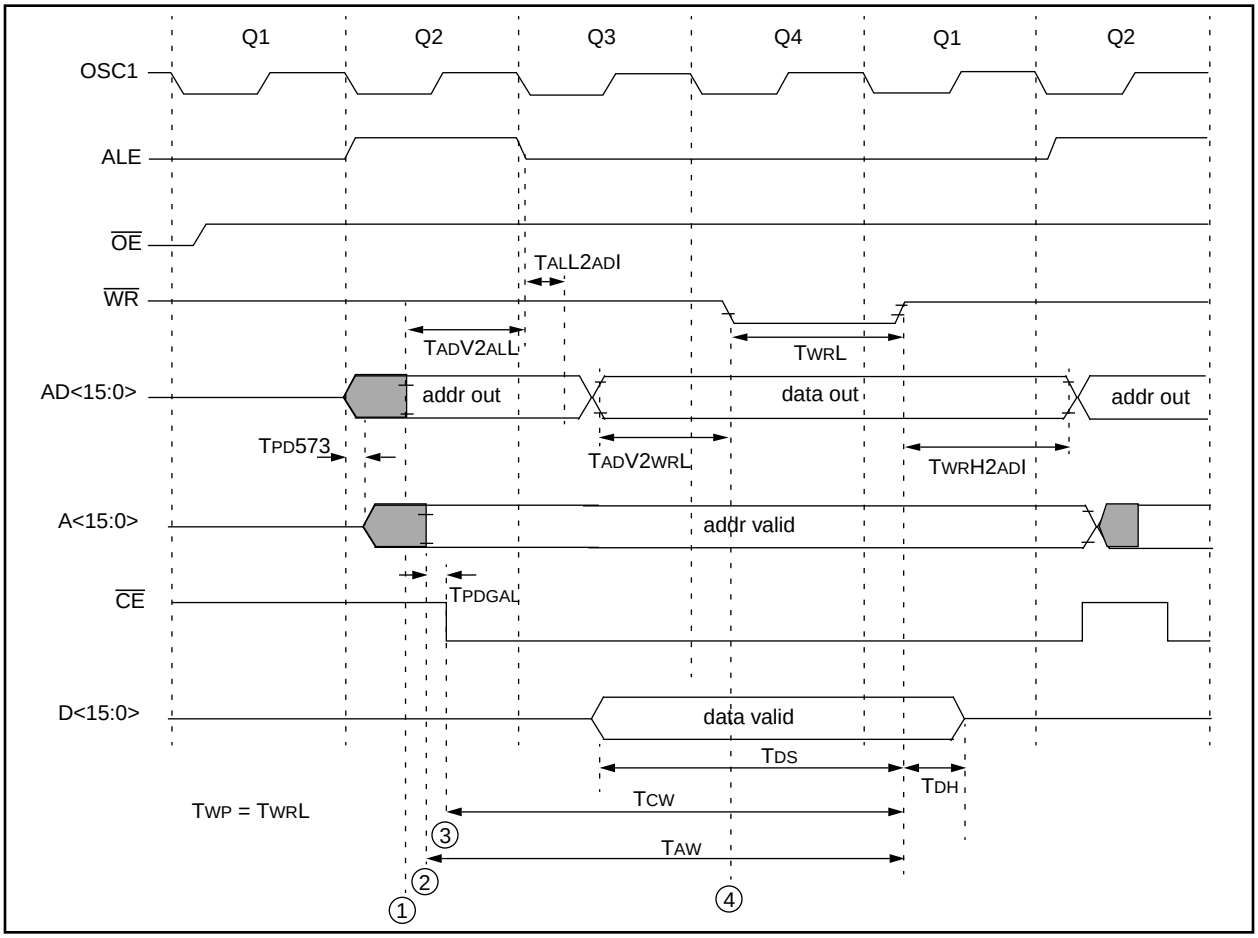


TABLE 4: LOCATION MARKER DESCRIPTIONS FOR FIGURE 3

Location	Description	Value	
1	Address Setup Time. This location marks the spot where the address becomes valid out of the PIC17CXX before ALE goes LOW. (Q2 cycle)	0.25 * TCY - 10	time in nanoseconds before the Q3 cycle (TADV2ALL)
2	Propagation delay of the 74ACT573. This is the spot where the address to the SRAM becomes valid. (Q2 cycle)	6	time in nanoseconds before the Q3 cycle
3	Propagation delay of the address decoder. This spot is where the CE signal from the address decoder to the SRAM goes LOW. (Q2 cycle)	TPDGAL	time in nanoseconds before the Q3 cycle
4	Write pulse goes LOW. The SRAM specifies that the address at it's inputs must be valid at or before this point. (Q4 cycle)		

TABLE 5: MEMORY INTERFACE WRITE REQUIREMENTS

Sym	Characteristic	Min	Typ	Max	Units
TADV2ALL	AD<15:0> (address) valid to ALE↓ (address setup time)	0.25Tcy - 10	—	—	ns
TALL2ADI	ALE↓ to address out invalid (address hold time)	0	—	—	ns
TADV2WRL	Data out valid to $\overline{WR}$↓ (data setup time)	0.25Tcy - 40	—	—	ns
TWRH2ADI	$\overline{WR}$↑ to data out invalid (data hold time)	—	0.25TCY	—	ns
TWRL	$\overline{WR}$ pulse width	—	0.25TCY	—	ns
TPD573	Propagation delay input to output	2	6	12	ns
TPDGAL	Propagation delay input to combinatorial output	3	—	7.5 - 25	ns
TDS	Data setup time	6 - 10	—	—	ns
TCW	$\overline{CE}$ to end of write	12 - 15	—	—	ns
TAW	Address valid to end of write	7 - 15	—	—	ns
TDH	Data hold time	0	—	—	ns
TWP	$\overline{WE}$ pulse width Low	7 - 15	—	—	ns

The critical timing specification for the write cycle is when the CE signal from the address decoder to the SRAM goes LOW. Typically the SRAM specifies this parameter (TAS for the MT5C2568). The other important SRAM specifications to check against the PIC17C4X are:

- TWP - Write enable LOW pulse width
- TDS - Data setup time, data valid before WE goes HIGH
- TDH - Data hold time, data valid after WE goes HIGH

The following are some calculations for the write cycle of various speed grades. These calculations are used to determine if any of the above specifications are invalid. The Micron MT5C2568 specifies the following values for the above parameters:

TAS - 0 ns min. for all speed grades

TWP - 15 ns min. for the 25 ns speed grade

TDS - 10 ns min. for the 25 ns speed grade

TDH - 0 ns min. for all speed grades

The PIC17C4X specifies the following values:

TWP - 0.25 * TCY	TWRL
TDS - 0.25 * TCY - 40 + TWP min.	TADV2WRL
TDH - 0.25 * TCY	TWRH2ADI

8 MHz (T_{CY} = 500 ns)	16 MHz (T_{CY} = 250 ns)	20 MHz (T_{CY} = 200 ns)	25 MHz (T_{CY} = 160 ns)
$T_{ADV2ALL}$ = 0.25 * 500 - 10	$T_{ADV2ALL}$ = 0.25 * 250 - 10	$T_{ADV2ALL}$ = 0.25 * 160 - 10	$T_{ADV2ALL}$ = 0.25 * 160 - 10
T_{AS} = $T_{ADV2ALL}$	T_{AS} = $T_{ADV2ALL}$	T_{AS} = $T_{ADV2ALL}$	T_{AS} = $T_{ADV2ALL}$
- 6	- 6	- 6	- 6
- T_{PDGAL}	- T_{PDGAL}	- T_{PDGAL}	- T_{PDGAL}
+ T_{CY}	+ T_{CY}	+ T_{CY}	+ Tcy
T_{WRL} = 0.25 * 500	T_{WRL} = 0.25 * 250	T_{WRL} = 0.25 * 160	T_{WRL} = 0.25 * 160
$T_{ADV2WRL}$ = 0.25 * 500 - 40 + 0.25 * 500	$T_{ADV2WRL}$ = 0.25 * 250 - 40 + 0.25 * 250	$T_{ADV2WRL}$ = 0.25 * 160 - 40 + 0.25 * 160	$T_{ADV2WRL}$ = 0.25 * 160 - 40 + 0.25 * 160
$T_{WRH2ADI}$ = 0.25 * 500	$T_{WRH2ADI}$ = 0.25 * 250	$T_{WRH2ADI}$ = 0.25 * 160	$T_{WRH2ADI}$ = 0.25 * 160
$T_{ADV2ALL}$ = 115	$T_{ADV2ALL}$ = 52.5	$T_{ADV2ALL}$ = 40	$T_{ADV2ALL}$ = 30
T_{AS} = 95	T_{AS} = 32.5	T_{AS} = 20	T_{AS} = 10
- 6	- 6	- 6	- 6
- T_{PDGAL}	- T_{PDGAL}	- T_{PDGAL}	- T_{PDGAL}
+ 125	+ 62.5	+ 50	+ 40
T_{WRL} = 125	T_{WRL} = 62.5	T_{WRL} = 50	T_{WRL} = 40
$T_{ADV2WRL}$ = 210	$T_{ADV2WRL}$ = 227.5	$T_{ADV2WRL}$ = 60	$T_{ADV2WRL}$ = 40
$T_{WRH2ADI}$ = 125	$T_{WRH2ADI}$ = 62.5	$T_{WRH2ADI}$ = 50	$T_{WRH2ADI}$ = 40
$T_{ADV2ALL}$ = 115	$T_{ADV2ALL}$ = 52.5	$T_{ADV2ALL}$ = 40	$T_{ADV2ALL}$ = 30
T_{AS} = 214 - T_{PDGAL}	T_{AS} = 89 - T_{PDGAL}	T_{AS} = 64 - T_{PDGAL}	T_{AS} = 44 - T_{PDGAL}
T_{WRL} > 15 ns	T_{WRL} > 15 ns	T_{WRL} > 15 ns	T_{WRL} > 15 ns
$T_{ADV2WRL}$ > 15 ns	$T_{ADV2WRL}$ > 15 ns	$T_{ADV2WRL}$ > 15 ns	$T_{ADV2WRL}$ > 15 ns
$T_{WRH2ADI}$ > 0 ns	$T_{WRH2ADI}$ > 0 ns	$T_{WRH2ADI}$ > 0 ns	$T_{WRH2ADI}$ > 0 ns

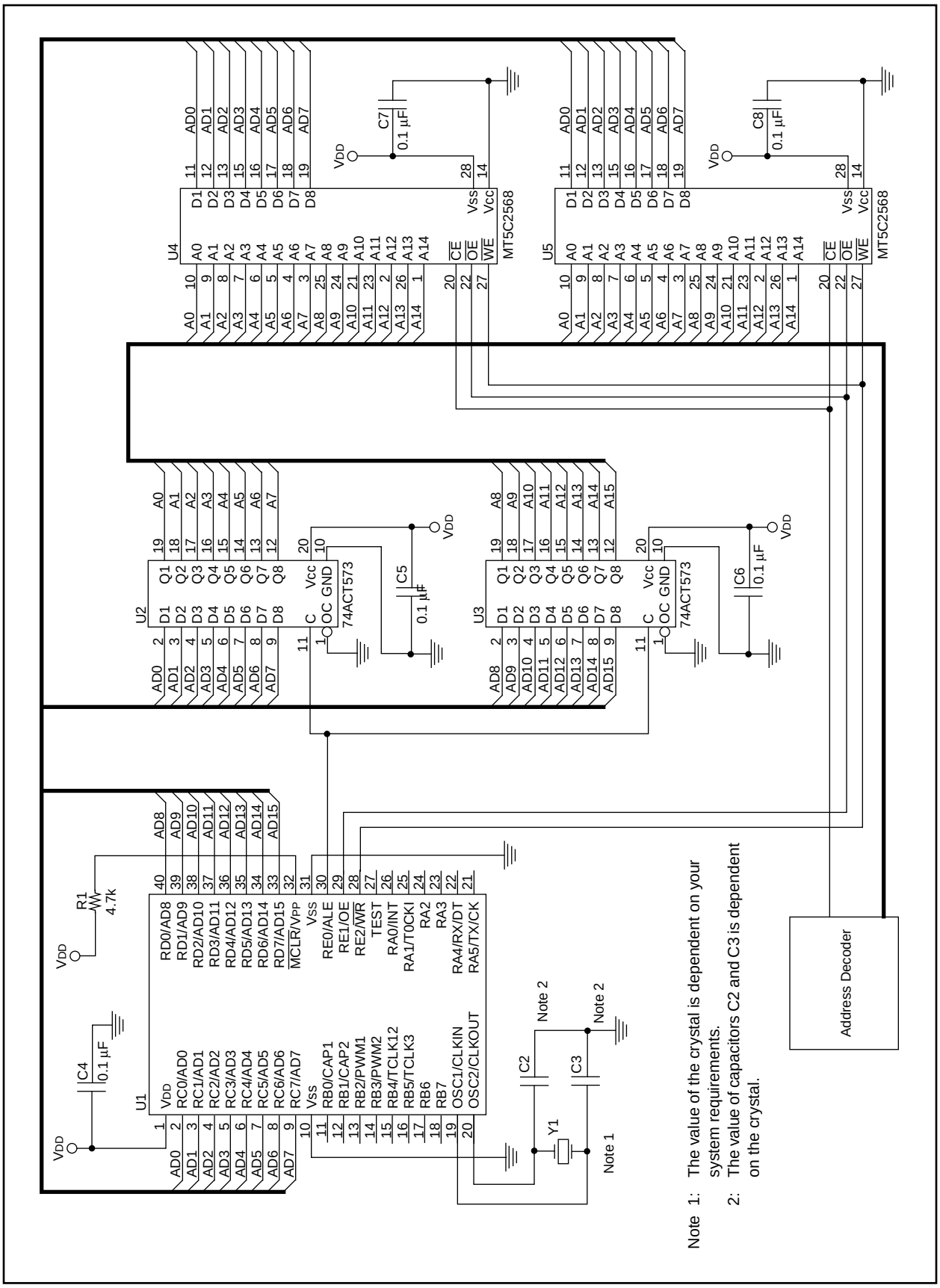
Assuming that a 16V8 with propagation delay of 25 ns is used for the address decoder, you can see that all crystal frequencies have a T_{AS} greater than 0. The other parameters $T_{ADV2WRL}$, $T_{WRH2ADI}$, and T_{WRL} all have at least 25 ns of spare room. The parameters $T_{ADV2WRL}$, $T_{WRH2ADI}$, and T_{WRL} were taken from a 25 ns speed grade SRAM. Therefore, all the speed grades of the MT5C2568 can be used for the write cycle of a PIC17C4X with an external oscillator frequency up to 25 MHz.

CONCLUSION

So now that we have done the calculations, let's determine the proper SRAM speed grade for the various frequencies. The only assumption is that a 25 ns 16V8 is used for address decoding.

- 8 MHz can use up to a 300 ns SRAM
- 16 MHz can use up to a 125 ns SRAM
- 20 MHz can use up to a 90 ns SRAM
- 25 MHz can use up to a 50 ns SRAM

APPENDIX A: PIC17C4X EXTERNAL RAM SCHEMATIC



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