TB011

Using SRAM With A PIC16CXX

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INTRODUCTION

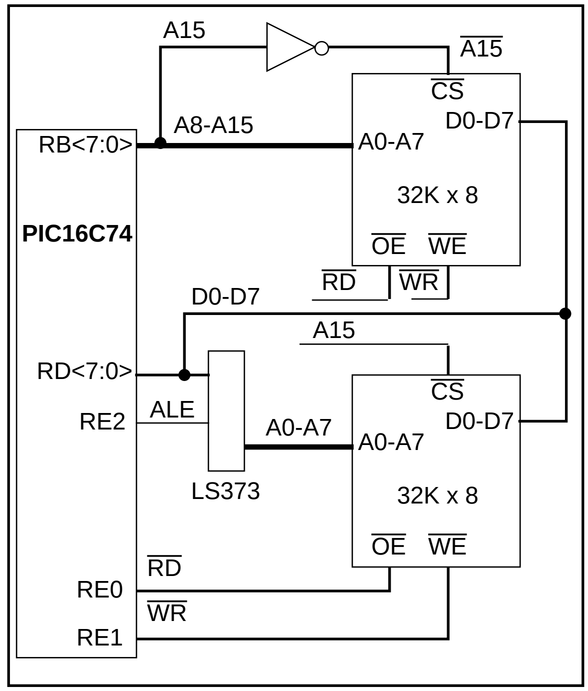
There are applications where a significant amount of data memory is required beyond what is in the micro-controller. For example, buffering communications data, creating large volatile tables and arrays. One interesting application is voice storage and playback. Some applications require relatively low frequencies, so a fast address/data bus and expensive FSRAM are not necessary.

This application note uses the PIC16C74. Since the PIC16C74 does not have an external address/data bus, one was created using the I/O ports. A software implementation of a multiplexed address/data bus is more than adequate for some applications. This application note discusses the read and write speeds achievable with the PIC16C74 running at 20 MHz, hardware connections necessary, and software routines for reading and writing to external memory.

IMPLEMENTATION

The multiplexed address/data bus was created using nineteen port pins (Figure 1). PORTD is address lines 0 through 7 multiplexed with data lines 0 through 7. PORTB is the upper address lines 8-15. RE0 is the $\overline{RD}$, RE1 is $\overline{WR}$ and RE2 is ALE (address latch enable). One SRAM chip is address range 0000H-7FFFH, and the other SRAM chip is address range 8000H-FFFFH. The chip selecting is done using A15 and $\overline{A15}$. A LS373 latch is needed to demultiplex the low order address/data bus.

FIGURE 1: BLOCK DIAGRAM OF MULTIPLEXED ADDRESS/ DATA BUS ON PIC16C74



The software needed to initialize the ports is in the subroutine `init_muxbus` (Appendix A). The initial states of the address lines and bus control signals are shown in the comments of the subroutine.

READ CYCLE

The software to do the read cycle is very straight forward. The read cycle drives the address on to the 16-bit bus, then latches the low order address lines 0-7 on to the memory device (Figure 2). When ALE goes low, address 0-7 is latched. Then the low order bus lines 0-7 are changed to input pins. Next, the read pin ($\overline{RD}$) goes low which turns on the output buffers of the memory device. Some time later, the data from the memory is driven on to the data lines 0-7. Then $\overline{RD}$ goes high and the output buffers of the memory device are disabled. Next, the low order data lines are changed back to outputs. The subroutine "`read_extmem`" shows the code used to emulate a read cycle on PORTB and PORTD.

You can ascertain from Table 1, that a slow SRAM can be used. There are three critical SRAM read cycle specifications:

TACC: Address access time

TOE: Output enable time

TDF: Data float time

The address access time TACC corresponds to the TAVDV (1.6 µs) of the emulated muxed bus. A FUJITSU MB84256C-70 has an access time of 70 ns. The output enable time TOE from the Fujitsu data sheet is 35 ns. The emulated muxed bus specification TRLDV (200 ns) corresponds to the TOE of the Fujitsu SRAM. The data float time TDF is only important if you are doing back to back bus cycles.

WRITE CYCLE

The write cycle moves data to the external SRAM. The address is driven on the sixteen address lines, then the low order address is latched by making ALE go high and then low. The "write" data is moved to the low order address lines (data lines). Finally, the WRITE pin is driven low and then high. When write goes high, the data is written to the SRAM. Figure 3 shows the bus timing diagram for the write cycle.

The write cycle is even simpler to implement in software than the read cycle. The subroutine "`write_extmem`" shows code used to write out data to an external SRAM.

The write pulse width is an important specification in memory design as well. For the PIC16C74 emulated address/data bus the write pulse width is TWLWH. This write pulse width is very large compared to actual address/data bus implementations. The TAVWH specification corresponds to the TAW specification of most memory devices. The emulated address/data bus has relatively slow bus timings compared with most memory access times such as EPROMs and SRAMs.

SUMMARY

A 40-pin PIC16CXX device such as the PIC16C74 can interface to external memory. This application note used sixteen address lines multiplexed with eight data lines to read/write to two external SRAMs. The read/write cycle times can be calculated easily given the single cycle instruction architectures of the PIC16CXX. Flash, EPROM and other parallel bus memory devices can be similarly utilized.

TABLE 1: READ AND WRITE CYCLE BUS TIMINGS

Timing	Description	Minimum	Maximum
TCY	Instruction cycle time @ 20 MHz	200 ns	DC
TLLLH	ALE pulse width	1 TCY	
TAVDV	Address valid to data valid		7 TCY
TRLDV	Read low to data valid	1 TCY	
TRHDZ	Read high to data float	0	1 TCY
TWLWH	WRITE pulse width	1 TCY	
TWHDX	WRITE high to data no longer valid (data hold time)		2 TCY
TAVWH	Address valid to write high		5 TCY

FIGURE 2: READ CYCLE ON MULTIPLEXED ADDRESS/DATA BUS

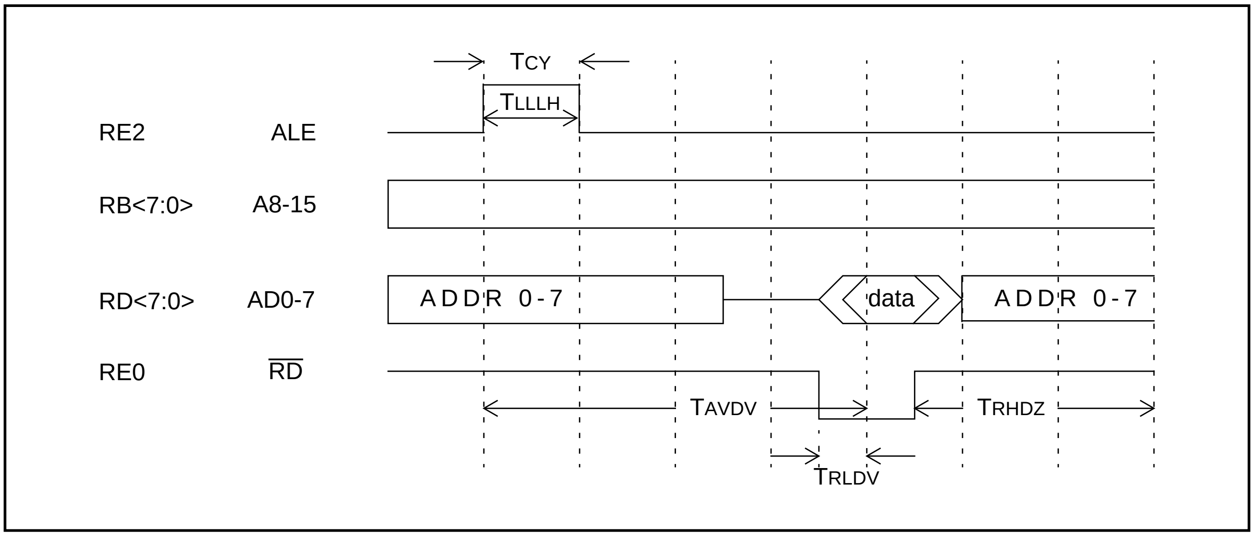
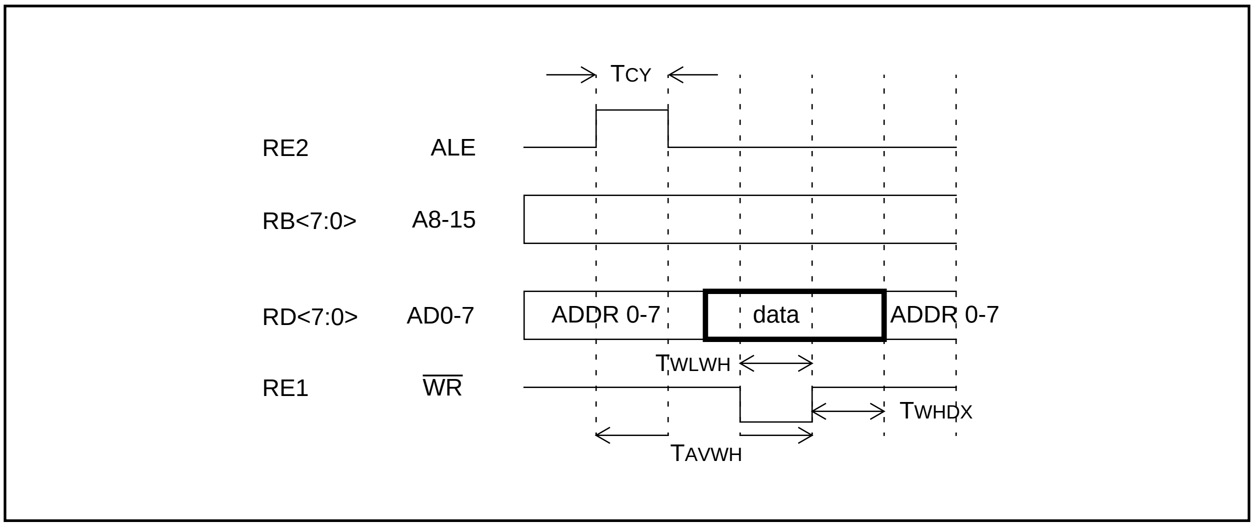


FIGURE 3: WRITE CYCLE BUS TIMINGS



APPENDIX A:PROGRAM LISTING: EXTERNAL MEMORY SUBROUTINES

```
;*******************************************************************
;*          Initialize the Multiplexed Address/Data Bus
;*
;* AD0-AD7 is PORTD 0-7
;* A8-A15 is PORTB 0-7
;* ALE is PORTE.2
;* RD# is PORTE.0
;* WR# is PORTE.1
;*
;* This init routine sets the multiplexed address/data bus up as
;* A0-A15 --> output low
;* ALE --> OUTPUT LOW
;* RD#,WR# --> OUTPUT HIGH
;*
;*******************************************************************

Init_MUXBUS
        bsf    STATUS,RP0         ;switch to bank 1 registers
        clrf   TRISB              ;set A8-A15 as output
        clrf   TRISD              ;set AD0-AD7 as output
        movlw  0xf8
        andwf  TRISE,F            ;ALE,RD#,WR# as output

        bcf    STATUS,RP0         ;switch to bank 0 registers

        clrf   ADHIGH             ;set A8-A15 to 0 (PORTB)
        clrf   ADLOW              ;set AD0-AD7 to 0 (PORTD)
        movlw  3                  ;ale=0,rd#=1,wr#=1
        movwf  PORTE
      return


;*******************************************************************
;*             Read External Memory of muxed bus
;*
;* INPUT: PORTB =A8-A15, PORTD = AD0-AD7
;* OUTPUT: W reg contains 8-bit data read from ext. mem.
;* CHANGED: W reg, ALE, RD#
;* (This READ routine has been modified to save the low order
;* address before a READ is done. The data read from memory will
;* destroy the address. After the read is done, the low order address
;* is written back out to PORTD.)
;*
;********************************************************************
read_extmem
        movf   ADLOW,W            ;save low order address
        movwf  ADLOW_IMAGE

        bsf    PORTE,ALE          ;ALE high for 200ns, RD#, WR# low
        bcf    PORTE,ALE          ;ALE goes low (A0-7 latched)
        bsf    STATUS,RP0
        movlw  0xff
        movwf  TRISD              ;make PORTD input
        bcf    STATUS,RP0

        bcf    PORTE,RD           ;drop READ low

        movf   ADLOW,W            ;move read data from AD bus to w reg
        bsf    PORTE,RD           ;pull READ high (RD pulse is 400ns)
        bsf    STATUS,RP0
        clrf   TRISD              ;make PORTD (ADLOW) output again
        bcf    STATUS,RP0
```

```
        movwf  w_image           ;save READ data
        movf   ADLOW_IMAGE,W     ;restore low order address
        movwf  ADLOW             ;on port
        movf   w_image,W         ;restore READ data to w

        return
;*******************************************************************
;*               Write to External Memory on muxed bus
;* INPUT:  PORTB= A8-A15, PORTD = AD0-AD7, W= 8-bit data to write
;* OUTPUT: NOTHING
;* CHANGED: PORTE IS TOGGLED FOR ALE,WR# AND PUT BACK TO 011B
;* (This WRITE routine has been modified to save the low order
;*  address before a write is done. Then the low order address
;* is put back on PORTD after the write.)
;*******************************************************************
write_extmem
        movwf  w_image           ;save w (data to write)
        movf   ADLOW,W
        movwf  ADLOW_IMAGE       ;save the low order address
        movf   w_image,W         ;restore w (data to write)

        bsf    PORTE,ALE         ;ALE high for 200ns, RD#,WR# low
        bcf    PORTE,ALE         ;latch lower address
        movwf  ADLOW             ;move write data to AD0-7
        bcf    PORTE,WR          ;WR# low for 200ns
        bsf    PORTE,WR          ;latch data in external memory

        movf   ADLOW_IMAGE,W
        movwf  ADLOW             ;restore low order address

        return
```

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