PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86E30/E31/E40 SL1873

PROGRAMMABLE CONSUMER CONTROLLER PROCESSOR

FEATURES

Part Number	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range	Speed (Mhz)
Z86E30	4	237	24	4.5V to 5.5V	16
Z86E31	2	124	24	4.5V to 5.5V	16
Z86E40	4	236	32	4.5V to 5.5V	16

*General-Purpose

- 8-Bit CMOS, One-Time Programmable (OTP) Microcontroller
- 28-Pin DIP/SOIC OTP, 28-Pin DIP Window, 40-Pin DIP OTP/Window, 44-Pin PLCC/QFP OTP, and 44-Pin PLCC Window Packages
- Software Programmable Low EMI Mode
- Software Enabled Watch-Dog Timer (WDT)
- Pull-Up Active/Open-Drain Programmable on Port 0, Port 1 and Port 2
- Programmable RC Oscillator, EPROM Protect, and RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: 0.6 µs
- Two Standby Modes: STOP and HALT
- 24/32 Input/Output Lines
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Three Expanded Register File (ERF) Control Registers
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Auto Latches
- Auto Power-On Reset (POR)
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E30/E31/E40 One-Time Programmable (OTP) Consumer Controller Processors are members of Zilog's Z8® single-chip microcontroller family featuring enhanced wake-up circuitry, programmable Watch-Dog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces with three Expanded Register Files (ERF) support a wide range of memory configurations. Through the ERF, the deisgner has access to three additional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E30/E31 have 24 pins, and the Z86E40 has 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

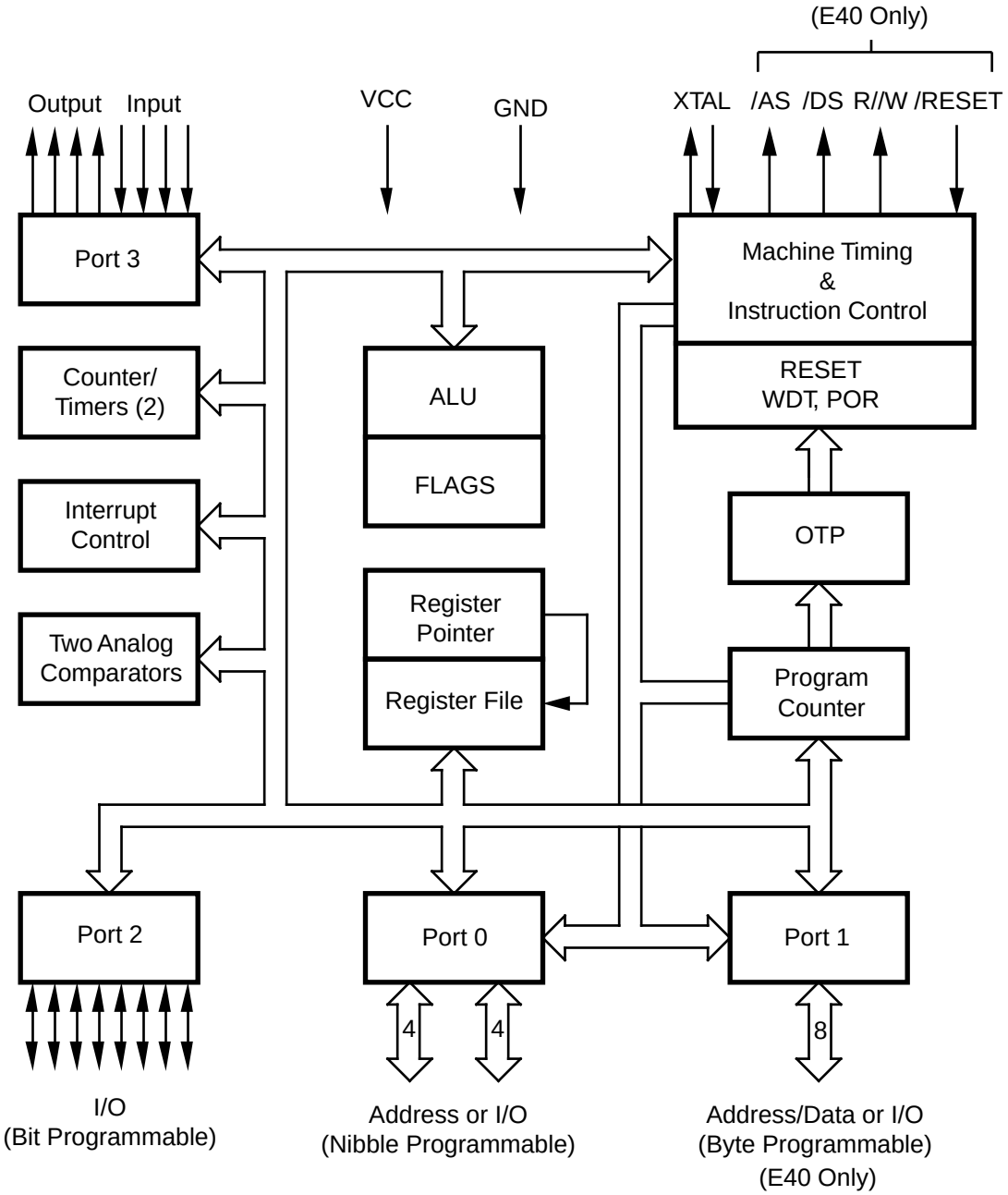

Figure 1. Z86E30/E31/E40 Functional Block Diagram

PIN IDENTIFICATION

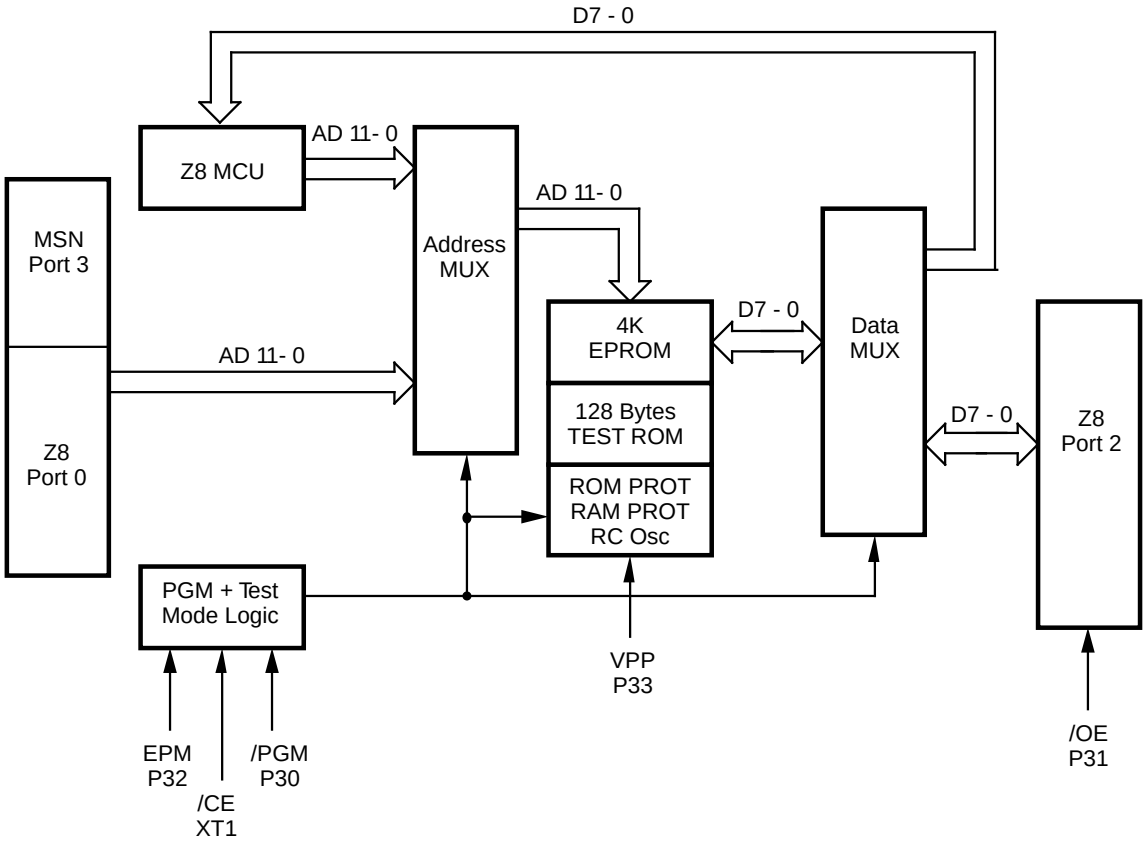

Figure 2. Z86E30/E31/E40 EPROM Programming Block Diagram

PIN IDENTIFICATION (Continued)

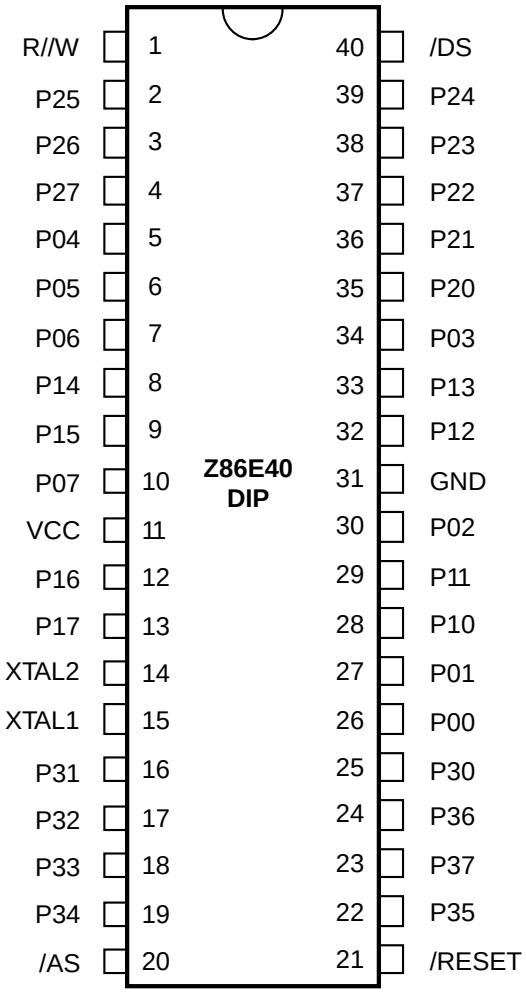

Figure 3. 40-Pin DIP Pin Configuration* (Standard Mode)

Table 1. 40-Pin DIP Pin Identification*

Standard Mode Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

Note:

* Pin Configuration and Identification identical on DIP and Cerdip Window Lid style packages.

PIN IDENTIFICATION (Continued)

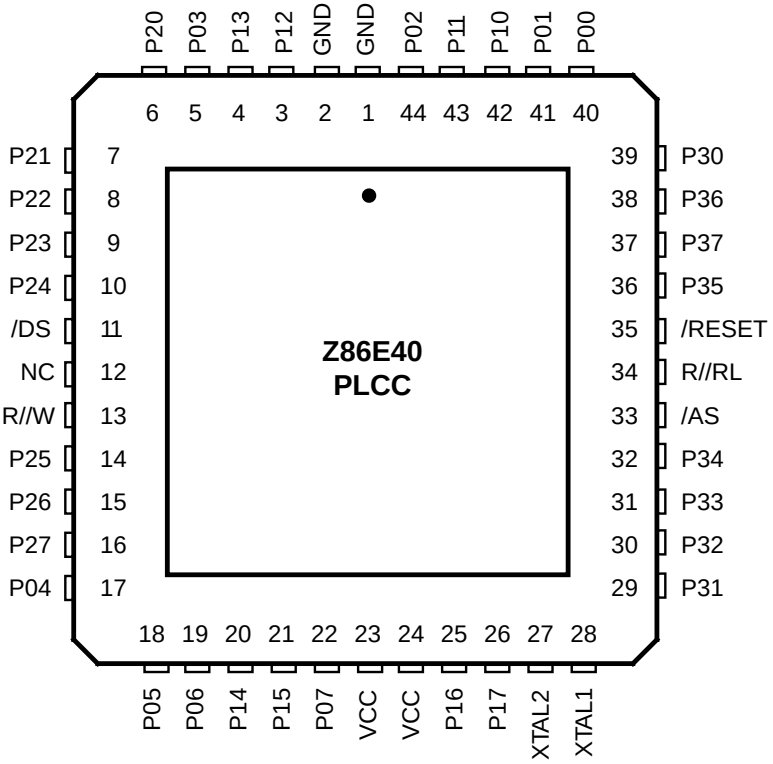

Figure 4. 44-Pin PLCC Pin Configuration (Standard Mode)

Table 2. 44-Pin PLCC Pin Identification

Standard Mode Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	No Connection	
13	R//W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23-24	V_{CC}	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output

Standard Mode Pin #	Symbol	Function	Direction
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

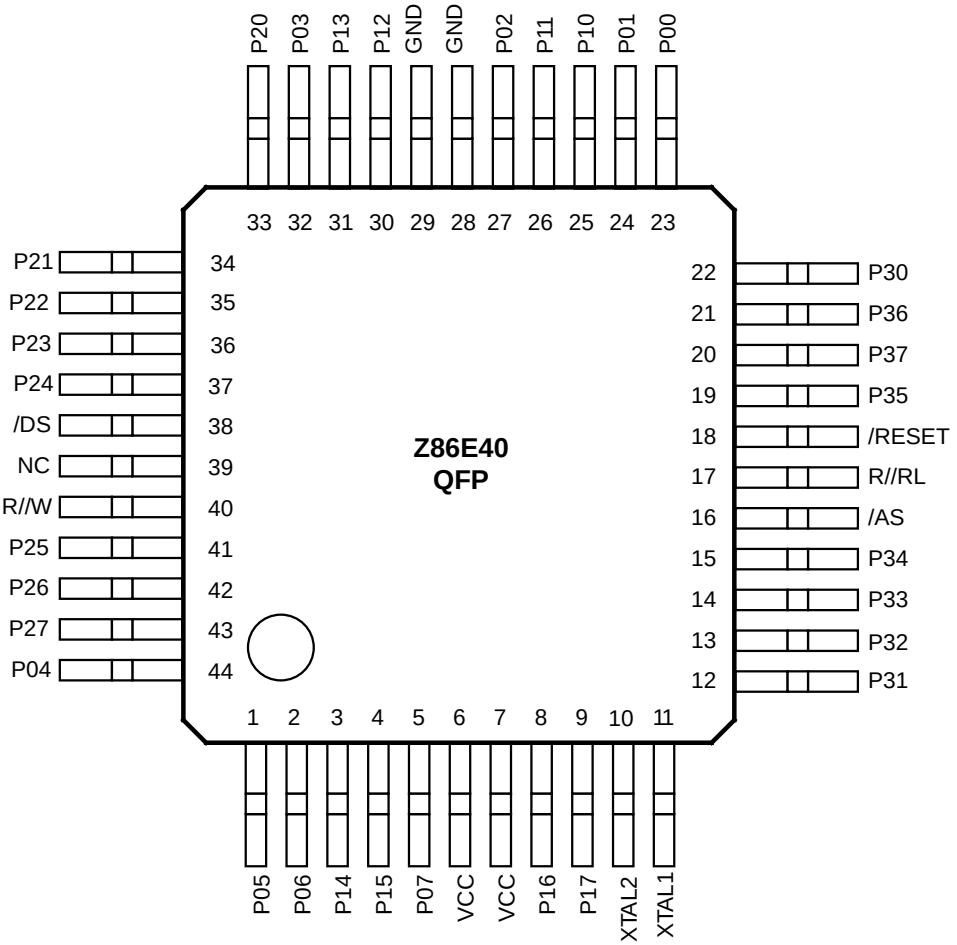

Figure 5. 44-Pin QFP Pin Configuration (Standard Mode)

Table 3. 44-Pin QFP Pin Identification

Standard Mode Pin #	Symbol	Function	Direction	Standard Mode Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-P01	Port 0, Pin 0,1	In/Output
6-7	V_{CC}	Power Supply		25-26	P10-P11	Port 1, Pins 0,1	In/Output
8-9	P16-P17	Port 1, Pins 6,7	In/Output	27	P02	Port 0, Pin 2	In/Output
10	XTAL2	Crystal Oscillator	Output	28-29	GND	Ground	
11	XTAL1	Crystal Oscillator	Input	30-31	P12-P13	Port 1, Pins 2,3	In/Output
12-14	P31-P13	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-4	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless select	Input	39	NC	No Connection	
18	/RESET	Reset	Input	40	R//W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output

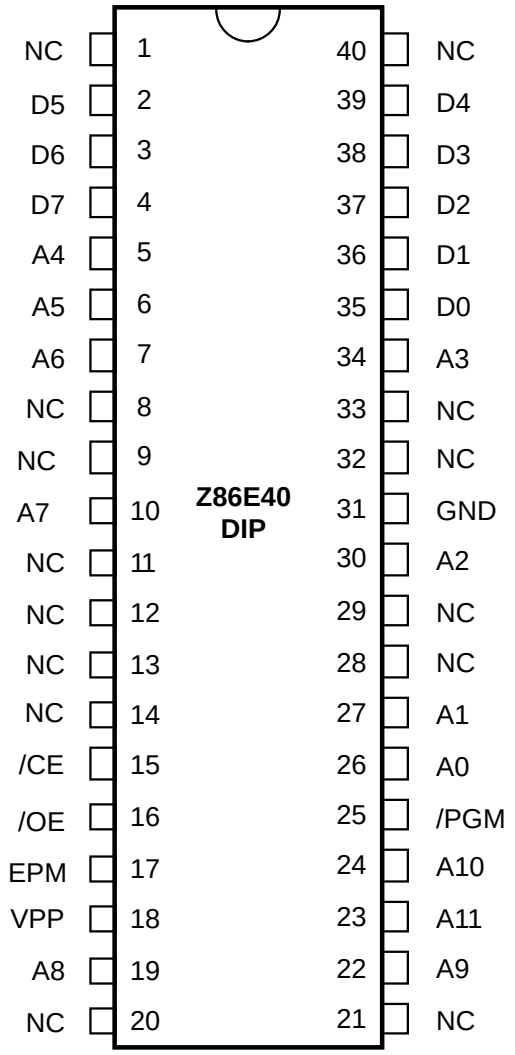

Figure 6. 40-Pin DIP Pin Configuration* (EPROM Mode)

Table 4. 40-Pin DIP Package Pin Identification*

EPROM Mode Pin #	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	In/Output
5-7	A4-A6	Address 4,5,6	Input
8-9	NC	No Connection	
10	A7	Address 7	Input
11	V_{CC}	Power Supply	
12-14	NC	No Connection	
15	/CE	Chip Select	Input
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19	A8	Address 8	Input
20-21	NC	No Connection	
22	A9	Address 9	Input
23	A11	Address 11	Input
24	A10	Address 10	Input
25	/PGM	Prog. Mode	Input
26-27	A0-A1	Address 0,1	Input
28-29	NC	No Connection	
30	A2	Address 2	Input
31	GND	Ground	
32-33	NC	No Connection	
34	A3	Address 3	Input
35-39	D0-D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

Note:

* Pin Configuration and Description identical on DIP and Cerdin Window Lid style packages.

PIN IDENTIFICATION (Continued)

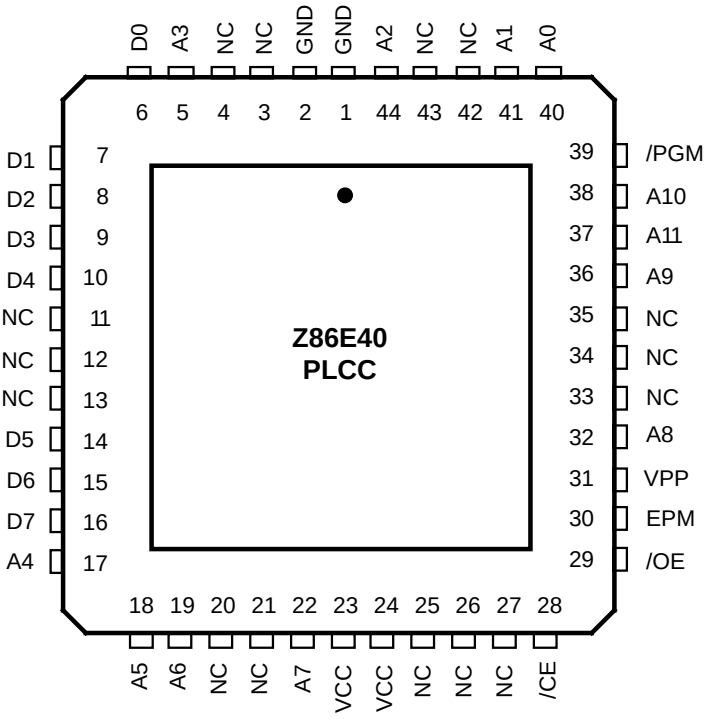

Figure 7. 44-Pin PLCC Pin Configuration (EPROM Programming Mode)

Table 5. 44-Pin PLCC Pin Identification

EPROM Programming Mode				EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**	**Pin #**	**Symbol**	**Function**	**Direction**
1-2	GND	Ground		29	/OE	Output Enable	Input
3-4	NC	No Connection		30	EPM	EPROM Prog. Mode	Input
5	A3	Address 3	Input	31	V_{PP}	Prog. Voltage	Input
6-10	D0-D4	Data 0,1,2,3,4	In/Output	32	A8	Address 8	Input
11-13	NC	No Connection		33-35	NC	No Connection	
14-16	D5-D7	Data 5,6,7	In/Output	36	A9	Address 9	Input
17-19	A4-A6	Address 4,5,6	Input	37	A11	Address 11	Input
20-21	NC	No Connection		38	A10	Address 10	Input
22	A7	Address 7	Input	39	/PGM	Prog. Mode	Input
23-24	V_{CC}	Power Supply		40-41	A0,A1	Address 0,1	Input
25-27	NC	No Connection		42-43	NC	No Connection	
28	/CE	Chip Select	Input	44	A2	Address 2	Input

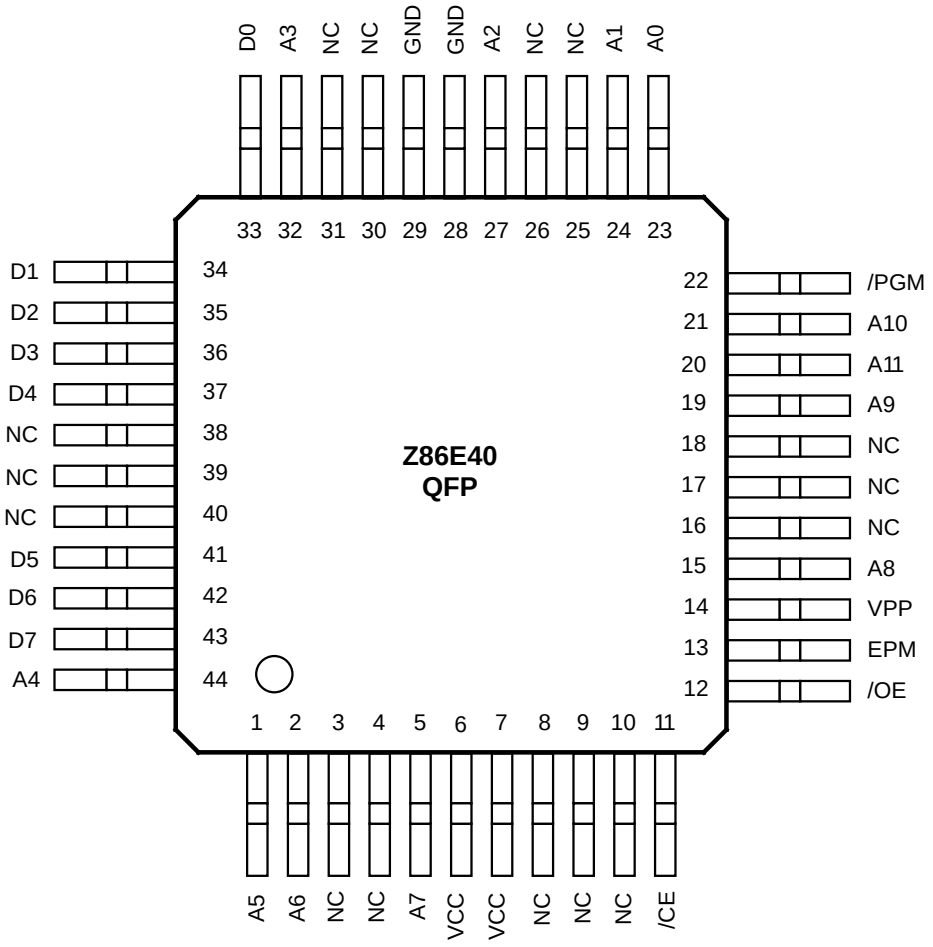

Figure 8. 44-Pin QFP Pin Configuration (EPROM Programming Mode)

Table 6. 44-pin QFP Pin Identification

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1-2	A5-A6	Address 5,6	Input
3-4	NC	No Connection	
5	A7	Address 7	Input
6-7	V_{CC}	Power Supply	
8-10	NC	No Connection	
11	/CE	Chip Select	Input
12	/OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15	A8	Address 8	Input
16-18	NC	No Connection	
19	A9	Address 9	Input
20	A11	Address 11	Input

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
21	A10	Address 10	Input
22	/PGM	Prog. Mode	Input
23-24	A0,A1	Address 0,1	Input
25-26	NC	No Connection	
27	A2	Address 2	Input
28-29	GND	Ground	
30-31	NC	No Connection	
32	A3	Address 3	Input
33-37	D0-D4	Data 0,1,2,3,4	In/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	In/Output
44	A4	Address 4	Input

PIN DESCRIPTION

Table 1. Z86E30/E31 28-Pin DIP Pin Identification*

Standard Mode Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

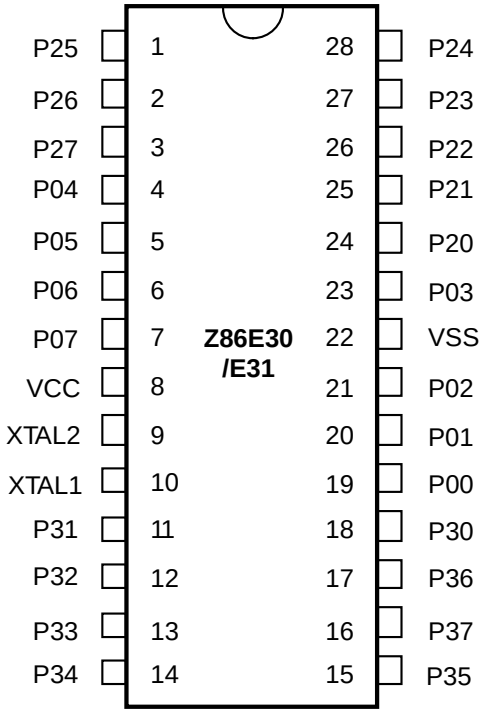

Figure 9. Z86E30/31 Standard Mode 28-Pin DIP Pin Configuration*

Table 2. Z86E30/E31 28-Pin DIP Pin Identification*

EPROM Programming Mode Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	In/Output
4-7	A4-A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	/CE	Chip Select	Input
11	/OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-15	A8-A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	/PGM	Prog. Mode	Input
19-21	A0-A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24-28	D0-D4	Data 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

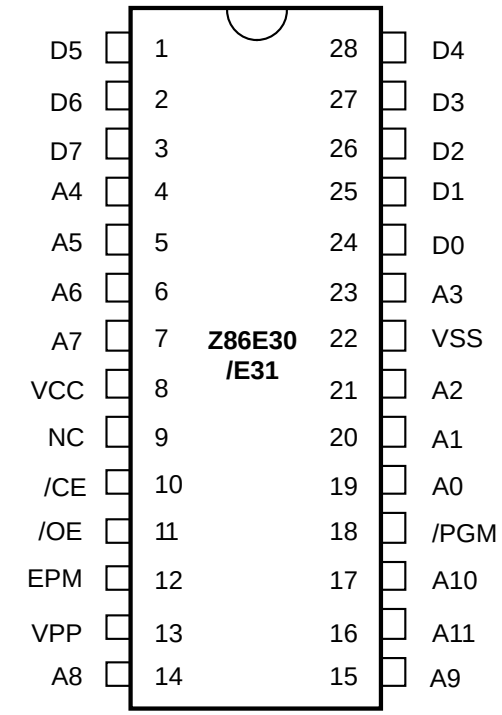

Figure 10. Z86E30/31 EPROM Programming Mode 28-Pin DIP Pin Configuration*

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		770	mW
Maximum Current out of V_{SS}		140	mA
Maximum Current into V_{DD}		125	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		25	mA
Maximum Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

Notice:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 770 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH} \,] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

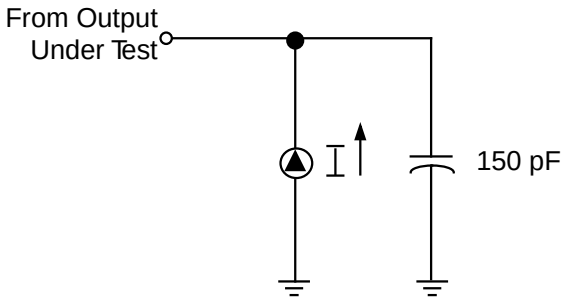

Figure 11. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	0.2V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	0.2V_{CC}	1.5	V		
		5.5V	GND-0.3	0.2V_{CC}	1.5	V		
V_{OH}	Output High Voltge	4.5V	V_{CC}–0.4		4.8	V	I_{OH}=–0.5mA	
	Low EMI Mode	5.5V	V_{CC}–0.4		4.8	V	I_{OH}=–0.5mA	
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[8]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[8]
V_{OL}	Output Low Voltage	4.5V		0.4	0.2	V	I_{OL}=1.0 mA	
	Low EMI Mode	5.5V		0.4	0.2	V	I_{OL}=1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL}=+4.0 mA	[8]
		5.0V		0.4	0.1	V	I_{OL}=+4.0 mA	[8]
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL}=+12mA	[8]
		5.5V		1.2	0.5	V	I_{OL}=+12mA	[8]
V_{RH}	Reset Input High Voltage	4.5V	.8V_{CC}	V_{CC}	2.1	V		[13]
		5.5V	.8V_{CC}	V_{CC}	2.1	V		[13]
V_{RL}	Reset Input Low Voltage	4.5V	GND–0.3	0.2V_{CC}	1.7			[13]
		5.5V	GND–0.3	0.2V_{CC}	1.7			[13]
V_{OFFSET}	Comparator Input Offset	4.5V		25	10	mV		
	Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	4.5V	0	V_{CC}–1.0V		V		[10]
	Voltage Range	5.5V	0	V_{CC}–1.0V		V		[10]
I_{IL}	Input Leakage	4.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
I_{IR}	Reset Input Current	4.5V		–180	–112	µA		
		5.5V		–180	–112	µA		
I_{CC}	Supply Current	4.5V		25	20	mA	@16MHz	[4,5]
		5.5V		25	20	mA	@16MHz	[4,5]
		4.5V		20	15	mA	@12MHz	[4,5]
		5.5V		20	15	mA	@12MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	4.5V		8	3.7	mA	HALT Mode V_{IN}=0V, V_{CC} @16MHz	[4,5]
		5.5V		8	3.7	mA	HALT Mode V_{IN}=0V, V_{CC} @16MHz	[4,5]
		4.5V		6	3.2	mA	HALT Mode V_{IN}=0V, V_{CC} @12MHz	[4,5]
		5.5V		6	3.2	mA	HALT Mode V_{IN}=0V, V_{CC} @12MHz	[4,5]
		4.5V		7.0	2.9	mA	Clock Divide by 16 @16MHz	[4,5]
		5.5V		7.0	2.9	mA	Clock Divide by 16 @16MHz	[4,5]
		4.5V		5	2.5	mA	Clock Divide by 16 @12MHz	[4,5]
		5.5V		5	2.5	mA	Clock Divide by 16 @12MHz	[4,5]
I_{CC2}	Standby Current	4.5V		10	2	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is not Running	[6,11]
		5.5V		10	2	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is not Running	[6,11]
		4.5V		800	600	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is Running	[6,11]
		5.5V		800	600	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	4.5V	1.4	15	4.7	µA	$OV<V_{IN}<V_{CC}$	[9]
		5.5V	1.4	15	4.7	µA	$OV<V_{IN}<V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	4.5V	–1	–8	–3.8	µA	$OV<V_{IN}<V_{CC}$	[9]
		5.5V	–1	–8	–3.8	µA	$OV<V_{IN}<V_{CC}$	[9]
T_{POR}	Power On Reset	4.5V	2.0	13	4	mS		
		5.5V	2.0	13	4	mS		
V_{LV}	Auto Reset Voltage		2.05	2.95	2.5	V		[1,7]

Note:

[1] Device does not function down to the Auto Reset voltage.
[2] GND = 0V.
[3] The V_{CC} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1= CL2 = 10 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Max. temperature is 70°C.
[8] STD Mode (not Low-EMI Mode).
[9] Auto Latch (mask option) selected.
[10] For analog comparator inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
[12] Typicals are at V_{CC} = 5.0V.
[13] Z86C40 only.

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note[3]	T_A=-40°C to 105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	0.2V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	0.2V_{CC}	1.5	V		
		5.5V	GND-0.3	0.2V_{CC}	1.5	V		
V_{OH}	Output High Voltge	4.5V	V_{CC}–0.4		4.8	V	I_{OH}=–0.5mA	
	Low EMI Mode	5.5V	V_{CC}–0.4		4.8	V	I_{OH}=–0.5mA	
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[8]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH}=–2.0mA	[8]
V_{OL}	Output Low Voltage	4.5V		0.4	0.2	V	I_{OL}=1.0 mA	
	Low EMI Mode	5.5V		0.4	0.2	V	I_{OL}=1.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL}=+4.0 mA	[8]
		5.0V		0.4	0.1	V	I_{OL}=+4.0 mA	[8]
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL}=+12mA	[8]
		5.5V		1.2	0.5	V	I_{OL}=+12mA	[8]
V_{RH}	Reset Input High Voltage	4.5V	.8V_{CC}	V_{CC}	2.1	V		[13]
		5.5V	.8V_{CC}	V_{CC}	2.1	V		[13]
V_{RL}	Reset Input Low Voltage	4.5V	GND–0.3	0.2V_{CC}	1.7			[13]
		5.5V	GND–0.3	0.2V_{CC}	1.7			[13]
V_{OFFSET}	Comparator Input Offset	4.5V		25	10	mV		
	Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	4.5V	0	V_{CC}–1.5V		V		[10]
	Voltage Range	5.5V	0	V_{CC}–1.5V		V		[10]
I_{IL}	Input Leakage	4.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN}=OV,V_{CC}	
I_{IR}	Reset Input Current	4.5V		–180	–112	µA		
		5.5V		–180	–112	µA		
I_{CC}	Supply Current	4.5V		25	20	mA	@16MHz	[4,5]
		5.5V		25	20	mA	@16MHz	[4,5]
		4.5V		20	15	mA	@12MHz	[4,5]
		5.5V		20	15	mA	@12MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note[3]	T_A = -40°C to 105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	4.5V		8	3.7	mA	HALT Mode V_{IN}=0V, V_{CC} @16MHz	[4,5]
		5.5V		8	3.7	mA	HALT Mode V_{IN}=0V, V_{CC} @16MHz	[4,5]
		4.5V		6	3.2	mA	HALT Mode V_{IN}=0V, V_{CC} @12MHz	[4,5]
		5.5V		6	3.2	mA	HALT Mode V_{IN}=0V, V_{CC} @12MHz	[4,5]
		4.5V		7.0	2.9	mA	Clock Divide by 16 @16MHz	[4,5]
		5.5V		7.0	2.9	mA	Clock Divide by 16 @16MHz	[4,5]
		4.5V		5	2.5	mA	Clock Divide by 16 @12MHz	[4,5]
		5.5V		5	2.5	mA	Clock Divide by 16 @12MHz	[4,5]
I_{CC2}	Standby Current	4.5V		10	2	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is not Running	[6,11]
		5.5V		10	2	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is not Running	[6,11]
		4.5V		1000	600	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is Running	[6,11]
		5.5V		1000	600	µA	STOP Mode V_{IN}=OV, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	µA	$OV<V_{IN}<V_{CC}$	[9]
		5.5V	1.4	20	4.7	µA	$OV<V_{IN}<V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	4.5V	–1.0	–10	–3.8	µA	$OV<V_{IN}<V_{CC}$	[9]
		5.5V	–1.0	–10	–3.8	µA	$OV<V_{IN}<V_{CC}$	[9]
T_{POR}	Power On Reset	4.5V	2.0	14	4	mS		
		5.5V	2.0	14	4	mS		
V_{LV}	Auto Reset Voltage		1.8	3.3	2.5	V		[1,7]

Note:

[1] Device does not function down to the Auto Reset voltage.
[2] GND=0V.
[3] The V_{CC} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1= CL2 = 100pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Max. temperature is 70°C.
[8] STD Mode (not Low EMI Mode).
[9] Auto Latch (mask option) selected.
[10] For analog comparator inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
[12] Typicals are at V_{CC} = 5.0V.
[13] Z86C40 only.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram (Z86C40 Only)

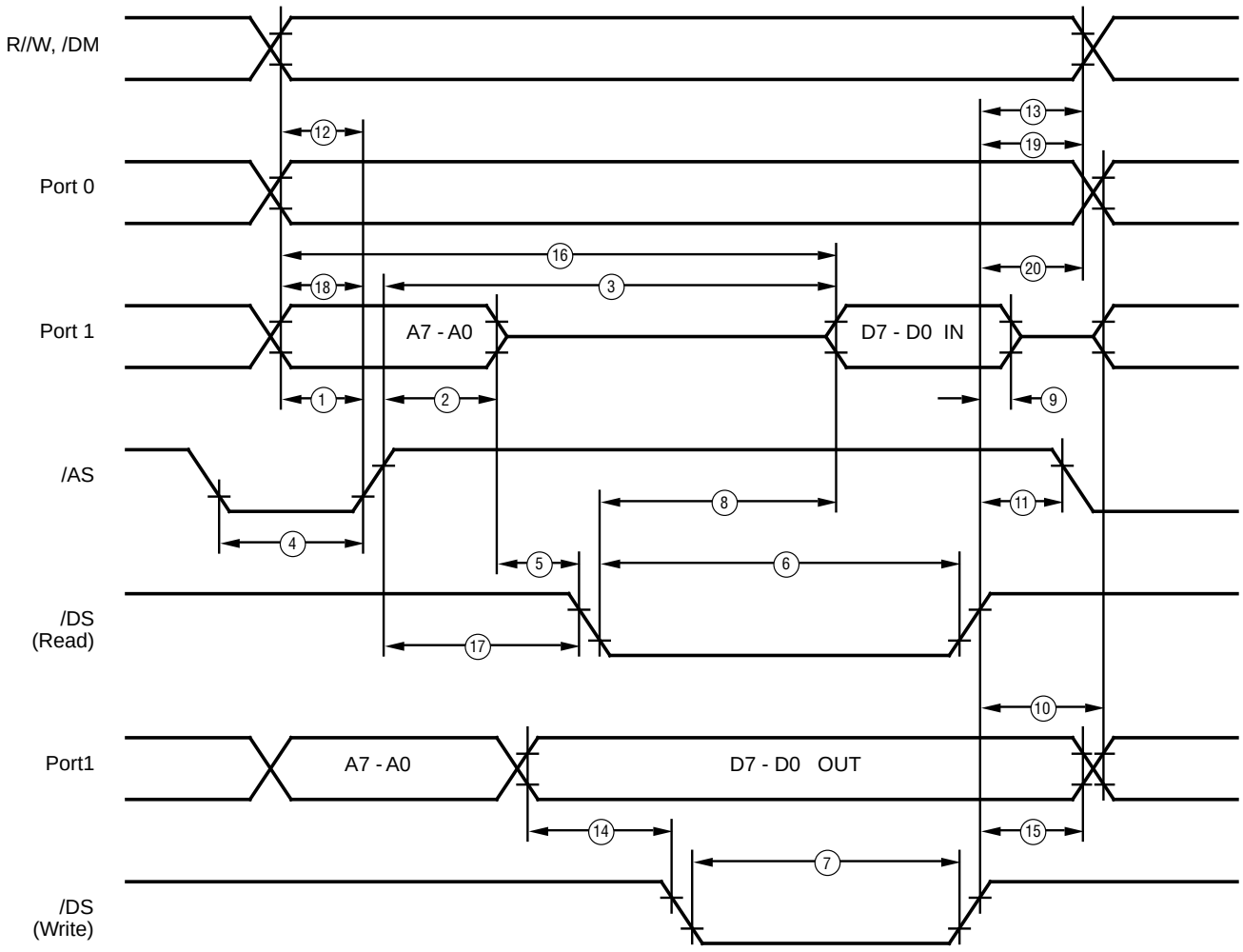

Figure 12. External I/O or Memory Read/Write Timing (Z86C40 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (Z86C40 Only)
(SCLK/TCLK = XTAL/2)

				T_A=-40°C to 105°C				T_A=-40°C to +105°C					
			Note[3]	12MHz		16MHz		12MHz		16MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	4.5V	35		25		35		25		ns	[2]
			5.5V	35		25		35		25		ns	
2	TdAS(A)	/AS Rise to Address Float Delay	4.5V	45		35		45		35		ns	[2]
			5.5V	45		35		45		35		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	4.5V		250		180		250		180	ns	[1,2]
			5.5V		250		180		250		180	ns	
4	TwAS	/AS Low Width	4.5V	55		40		55		40		ns	[2]
			5.5V	55		40		55		40		ns	
5	TdAS(DS)	Address Float to /DS Fall	4.5V	0		0		0		0		ns	
			5.5V	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	4.5V	200		135		200		135		ns	[1,2]
			5.5V	200		135		200		135		ns	
7	TwDSW	/DS (Write) Low Width	4.5V	110		80		110		80		ns	[1,2]
			5.5V	110		80		110		80		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	4.5V		150		75		150		75	ns	[1,2]
			5.5V		150		75		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	4.5V0	0		0		0		0		ns	[2]
			5.5V	0		0		0		0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	4.5V	45		50		45		50		ns	[2]
			5.5V	55		50		55		50		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	4.5V	30		35		30		35		ns	[2]
			5.5V	45		35		45		55		ns	
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	4.5V	45		25		45		25		ns	[2]
			5.5V	45		25		45		25		ns	
13	TdDS(R/W)	/DS Rise to R//W Not Valid	4.5V	45		35		45		35		ns	[2]
			5.5V	45		35		45		35		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	4.5V	55		25		55		25		ns	[2]
			5.5V	55		25		55		25		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	4.5V	45		35		45		35		ns	[2]
			5.5V	45		35		45		35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310		230		310		230	ns	[1,2]
			5.5V		310		230		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	4.5V	65		45		65		45		ns	[2]
			5.5V	65		45		65		45		ns	
18	TdDM(AS)	/DM Valid to /AS Fall Delay	4.5V	35		30		35		30		ns	[2]
			5.5V	35		30		35		30		ns	
19	TdDS(DM)	/DS Rise to DM Valid Delay	4.5V	45		35		45		35		ns	
			5.5V	45		35		45		35		ns	
20	ThDS(AS)	/DS Valid to Address Valid Hold Time	4.5V	45		35		45		35		ns	
			5.5V	45		35		45		35		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

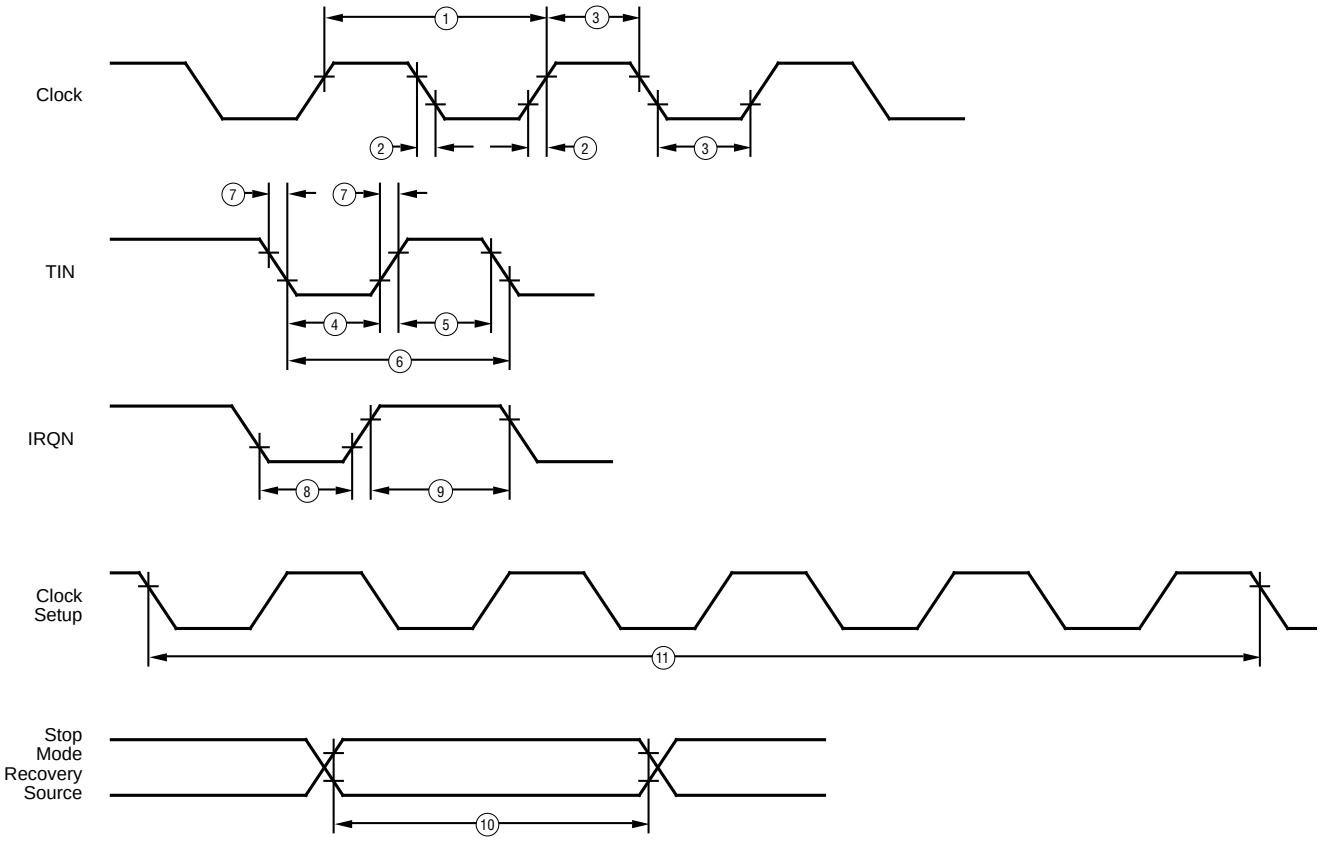

Figure 13. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode)

				T_A=0°C to +70°C 4MHz		T_A=-40°C to +105°C 4MHz			
No	Symbol	Parameter	V_{CC} Note[6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	4.5V	100		100		ns	[1,7,8]
			5.5V	100		100		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin,	Timer Input Rise & Fall Timer	4.5V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	4.5V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 1, POR STOP Mode Delay is on.

[5] Reg. WDTMR.

[6] The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

[7] SMR D1 = 0.

[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.

[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

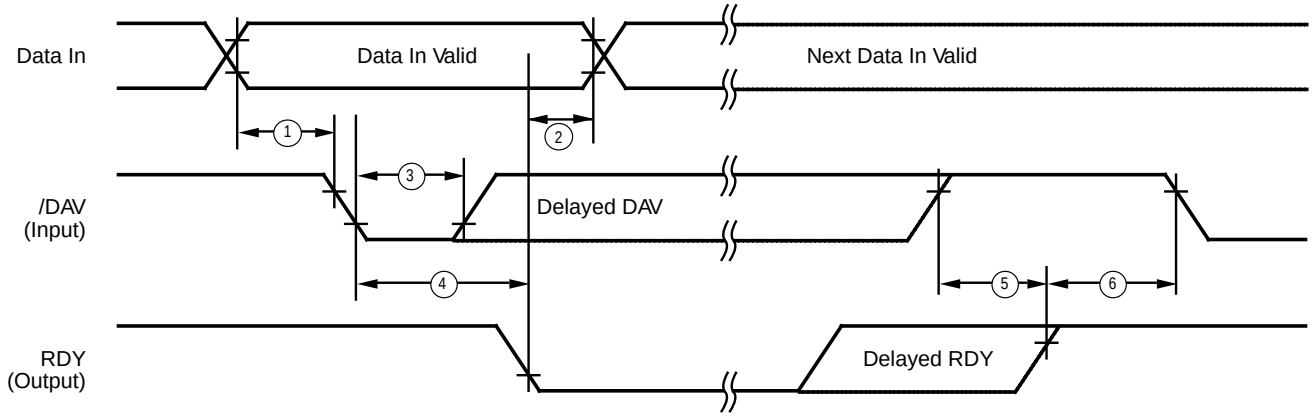

Figure 14. Input Handshake Timing

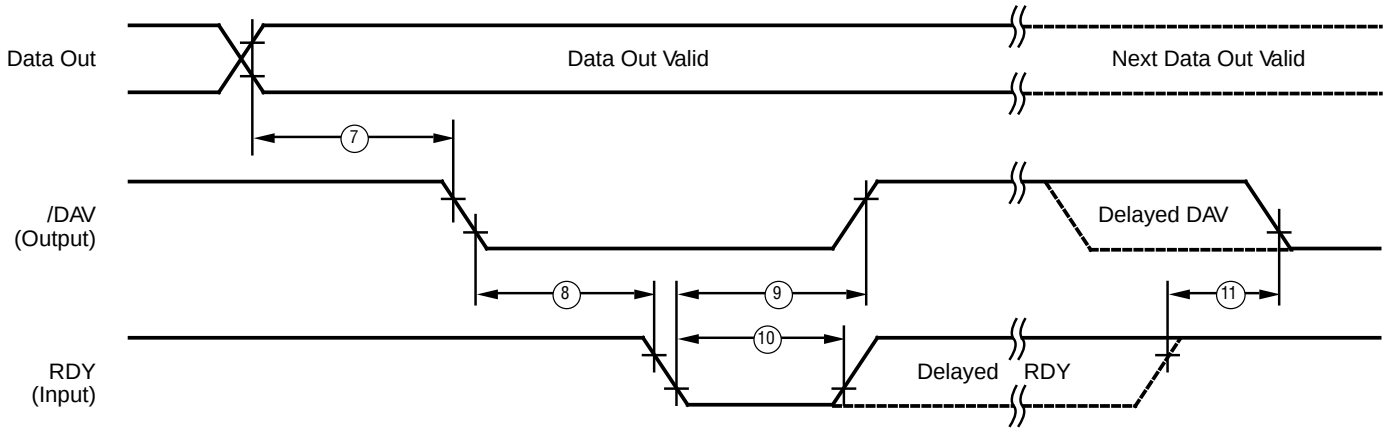

Figure 15. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

				T_A = -40°C to +105°C, T_A = 0°C to +70°C					
			V_{CC}	16MHz		12MHz			
No	Symbol	Parameter	Note[6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	62.5	DC	83	DC	ns	[1,7,8]
			5.5V	62.5	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	4.5V		15		15	ns	[1,7,8]
			5.5V		15		15	ns	[1,7,8]
3	TwC	Input Clock Width	4.5V	31		26		ns	[1,7,8]
			5.5V	31		26		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	4.5V	70		70		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin,	Timer Input Rise & Fall Timer	4.5V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	4.5V	70		70		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	4.5V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		[4,8]
			5.5V		5TpC		5TpC		[4,8]
12	Twdt	Watch-Dog Timer Delay Time	4.5V	5		5		ms	D0=0 [5,11]
		Before Refresh	5.5V	5		5.0		ms	D1=0 [5,11]
			4.5V	10		20		ms	D0=1 [5,11]
			5.5V	10		10		ms	D1=0 [5,11]
			4.5V	20		20		ms	D0=0 [5,11]
			5.5V	20		20		ms	D1=1 [5,11]
			4.5V	80		80		ms	D0=1 [5,11]
			5.5V	80		80		ms	D1=1 [5,11]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP Mode Delay is on.
[5] Reg. WDTMR.
[6] The V_{CC} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.
[10] Standard Mode (not Low EMI output ports).
[11] Using internal RC.

PRECAUTIONS

(1) When in ROM Protect Mode, and executing out of *External Program Memory*, instructions LDC, LDCI, LDE, and LDEI *cannot* read Internal Program Memory.

When in ROM Protect Mode, and executing out of *Internal Program Memory*, instructions LDC, LDCI, LDE, and LDEI *can* read Internal Program Memory.

(2) Low EMI is 25 percent of standard pull-down output driver and 25 percent of standard pull-up output driver.

(3) The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which time the outputs remain in the last state.

(4) Extended timing is operable.

(5) P0/P1/P2/P3 is Low-EMI software programmable.

(6) P0/P1/P2 is software programmable for open-drain.

(7) Expanded register PCON is Write Only.

(8) WDTMR is writable only within the first 64 system clocks after Reset. Afterward, the WDTMR is write protected.

(9) Device does not function down to the V_{LV} threshold. At temperatures less than 25°C, the V_{LV} threshold will rise to a maximum V_{DD} of 3.3V.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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