

### FEATURES

#### Ultralow Offset Voltage:

- $T_A = +25^\circ\text{C}$ : 10  $\mu\text{V}$  max
- $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ : 20  $\mu\text{V}$  max

#### Outstanding Offset Voltage Drift: 0.1 $\mu\text{V}/^\circ\text{C}$ max

#### Excellent Open-Loop Gain and Gain Linearity:

- 12  $\text{V}/\mu\text{V}$  typ

#### CMRR: 130 dB min

#### PSRR: 120 dB min

#### Low Supply Current: 2.0 mA max

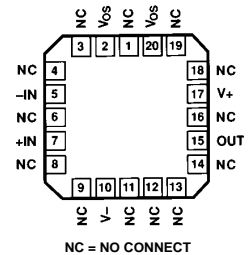
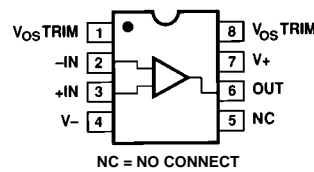
#### Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)

### PIN CONNECTIONS

Epoxy Mini-DIP  
(P Suffix)

OP177BRC/883  
LCC (RC Suffix)

8-Pin Hermetic DIP  
(Z-Suffix)  
8-Pin SO  
(S-Suffix)



### GENERAL DESCRIPTION

The OP177 features the highest precision performance of any op amp currently available. Offset voltage of the OP177 is only 10  $\mu\text{V}$  max at room temperature and 20  $\mu\text{V}$  max over the full military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . The ultralow  $V_{OS}$  of the OP177, combines with its exceptional offset voltage drift ( $TCV_{OS}$ ) of 0.1  $\mu\text{V}/^\circ\text{C}$  max, to eliminate the need for external  $V_{OS}$  adjustment and increases system accuracy over temperature.

The OP177's open-loop gain of 12  $\text{V}/\mu\text{V}$  is maintained over the full  $\pm 10 \text{ V}$  output range. CMRR of 130 dB min, PSRR of 120 dB min, and maximum supply current of 2 mA are just a few examples of the excellent performance of this operational amplifier. The OP177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The OP177 is offered in both the  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  military, and the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  extended industrial temperature ranges. This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

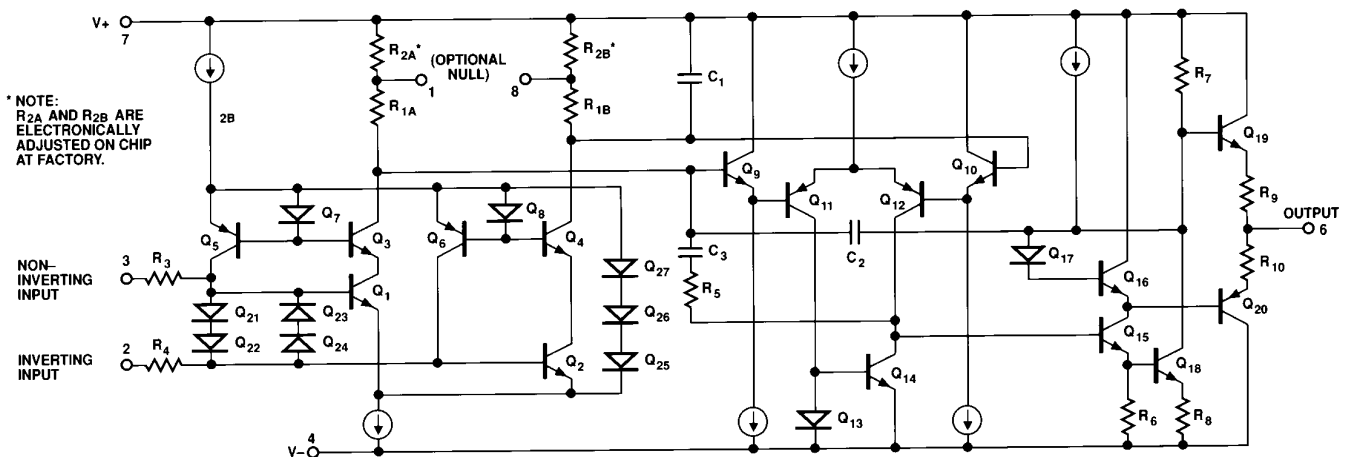


Figure 1. Simplified Schematic

REV. B

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# OP177—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$ , $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	OP177A			OP177B			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			4	10		10	25	$\mu\text{V}$
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)		0.2			0.2		$\mu\text{V}/\text{Mo}$
Input Offset Current	$I_{OS}$			0.3	1.0		0.3	1.5	nA
Input Bias Current	$I_B$		-0.2		1.5	-0.2		2.0	nA
Input Noise Voltage	$e_n$	$f_o = 1\text{ Hz to } 100\text{ Hz}^2$		118	150		118	150	nV rms
Input Noise Current	$i_n$	$f_o = 1\text{ Hz to } 100\text{ Hz}^2$		3	8		3	8	pA rms
Input Resistance Differential-Mode	$R_{IN}$	(Note 3)	26	45		26	45		M $\Omega$
Input Resistance Common-Mode	$R_{INCM}$			200			200		G $\Omega$
Input Voltage Range	IVR	(Note 4)	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	130	140		130	140		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	120	125		115	125		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}^5$	5000	12000		5000	12000		V/mV
Output Voltage Swing	$V_O$	$R_L \geq 10\text{ k}\Omega$	$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$		V
		$R_L \geq 2\text{ k}\Omega$	$\pm 12.5$	$\pm 13.0$		$\pm 12.5$	$\pm 13.0$		V
		$R_L \geq 1\text{ k}\Omega$	$\pm 12.0$	$\pm 12.5$		$\pm 12.0$	$\pm 12.5$		V
Slew Rate	SR	$R_L \geq 2\text{ k}\Omega^2$	0.1	0.3		0.1	0.3		V/ $\mu\text{s}$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1^2$	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	$R_O$			60			60		$\Omega$
Power Consumption	$P_D$	$V_S = \pm 15\text{ V}$ , No Load		50	60		50	60	mW
		$V_S = \pm 3\text{ V}$ , No Load		3.5	4.5		3.5	4.5	mW
Supply Current	$I_{SY}$	$V_S = \pm 15\text{ V}$ , No Load		1.6	2.0		1.6	2.0	mA
Offset Adjustment Range		$R_p = 20\text{ k}\Omega$		$\pm 3$			$\pm 3$		mV

### NOTES

<sup>1</sup>Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically less than 2.0  $\mu\text{V}$ .

<sup>2</sup>Sample tested.

<sup>3</sup>Guaranteed by design.

<sup>4</sup>Guaranteed by CMRR test condition.

<sup>5</sup>To insure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$ , $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	OP177A			OP177B			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			10	20		25	55	$\mu\text{V}$
Average Input Offset Voltage Drift	$\text{TCV}_{OS}$	(Note 1)		0.03	0.1		0.1	0.3	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$			0.5	1.5		0.5	2.0	nA
Average Input Offset Current Drift	$\text{TCI}_{OS}$	(Note 2)		1.5	25		1.5	25	pA/ $^\circ\text{C}$
Input Bias Current	$I_B$		-0.2	2.4	4	-0.2	2.4	4	nA
Average Input Bias Current Drift	$\text{TCI}_B$	(Note 2)		8	25		8	25	pA/ $^\circ\text{C}$
Input Voltage Range	IVR	(Note 3)	$\pm 13$	$\pm 13.5$		$\pm 13$	$\pm 13.5$		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	120	140		120	140		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	120	125		110	120		dB
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}^4$	2000	6000		2000	6000		V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2\text{ k}\Omega$	$\pm 12$	$\pm 13.0$		$\pm 12$	$\pm 13.0$		V
Power Consumption	$P_D$	$V_S = \pm 15\text{ V}$ , No Load		60	75		60	75	mW
Supply Current	$I_{SY}$	$V_S = \pm 15\text{ V}$ , No Load		2.0	2.5		2.0	2.5	mA

### NOTES

<sup>1</sup> $\text{TCV}_{OS}$  is 100% tested.

<sup>2</sup>Guaranteed by endpoint limits.

<sup>3</sup>Guaranteed by CMRR test condition.

<sup>4</sup>To insure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

Specifications subject to change without notice.

**ELECTRICAL CHARACTERISTICS** (@  $V_S = \pm 15\text{ V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	OP177E			OP177F			OP177G			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			4	10		10	25		20	60	$\mu\text{V}$
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)		0.2			0.3			0.4		$\mu\text{V}/\text{Mo}$
Input Offset Current	$I_{OS}$			0.3	1.0		0.3	1.5		0.3	2.8	nA
Input Bias Current	$I_B$		-0.2	1.0	1.5	-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	$e_n$	$f_o = 1\text{ Hz to } 100\text{ Hz}^2$		118	150		118	150		118	150	nV rms
Input Noise Current	$i_n$	$f_o = 1\text{ Hz to } 100\text{ Hz}^2$		3	8		3	8		3	8	pA rms
Input Resistance												
Differential-Mode	$R_{IN}$	(Note 3)	26	45		26	45		18.5	45		$\text{M}\Omega$
Input Resistance												
Common-Mode	$R_{INCM}$			200			200			200		$\text{G}\Omega$
Input Voltage Range	IVR	(Note 4)	$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		$\pm 13$	$\pm 14$		V
Common-Mode												
Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	130	140		130	140		115	140		dB
Power Supply												
Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	120	125		115	125		110	120		dB
Large Signal												
Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}^5$	5000	12000		5000	12000		2000	6000		V/mV
Output Voltage												
Swing	$V_O$	$R_L \geq 10\text{ k}\Omega$	$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$		$\pm 13.5$	$\pm 14.0$		V
		$R_L \geq 2\text{ k}\Omega$	$\pm 12.5$	$\pm 13.0$		$\pm 12.5$	$\pm 13.0$		$\pm 12.5$	$\pm 13.0$		V
		$R_L \geq 1\text{ k}\Omega$	$\pm 12.0$	$\pm 12.5$		$\pm 12.0$	$\pm 12.5$		$\pm 12.0$	$\pm 12.5$		V
		$R_L \geq 2\text{ k}\Omega^2$	0.1	0.3		0.1	0.3		0.1	0.3		V/ $\mu\text{s}$
Slew Rate	SR											
Closed-Loop												
Bandwidth	BW	$A_{VCL} = +1^2$	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output												
Resistance	$R_O$			60			60			60		$\Omega$
Power Consumption	$P_D$	$V_S = \pm 15\text{ V}$ , No Load		50	60		50	60		50	60	mW
		$V_S = \pm 3\text{ V}$ , No Load		3.5	4.5		3.5	4.5		3.5	4.5	mW
Supply Current	$I_{SY}$	$V_S = \pm 15\text{ V}$ , No Load		1.6	2.0		1.6	2.0		1.6	2.0	mA
Offset Adjustment												
Range		$R_p = 20\text{ k}\Omega$		$\pm 3$			$\pm 3$			$\pm 3$		mV

## NOTES

<sup>1</sup>Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically less than 2.0  $\mu\text{V}$ .

<sup>2</sup>Sample tested.

<sup>3</sup>Guaranteed by design.

<sup>4</sup>Guaranteed by CMRR test condition.

<sup>5</sup>To insure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

Specifications subject to change without notice.

# OP177—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	OP177E			OP177F			OP177G			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			10	20		15	40		20	100	$\mu\text{V}$
Average Input Offset Voltage Drift	$\text{TCV}_{OS}$	(Note 1)		0.03	0.1		0.1	0.3		0.7	1.2	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$			0.5	1.5		0.5	2.2		0.5	4.5	nA
Average Input Offset Current Drift	$\text{TCI}_{OS}$	(Note 2)		1.5	25		1.5	40		1.5	85	$\text{pA}/^\circ\text{C}$
Input Bias Current	$I_B$		-0.2	2.4	4	-0.2	2.4	4		2.4	$\pm 6.0$	nA
Average Input Bias Current Drift	$\text{TCI}_B$	(Note 2)		8	25		8	40		15	60	$\text{pA}/^\circ\text{C}$
Input Voltage Range Common-Mode	IVR	(Note 3)	$\pm 13$	$\pm 13.5$		$\pm 13$	$\pm 13.5$		$\pm 13.0$	$\pm 13.5$		V
Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{ V}$	120	140		120	140		110	140		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V to } \pm 18\text{ V}$	120	125		110	120		106	115		dB
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}^4$	2000	6000		2000	6000		1000	4000		V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2\text{ k}\Omega$	$\pm 12$	$\pm 13.0$		$\pm 12$	$\pm 13.0$		$\pm 12.0$	$\pm 13.0$		V
Power Consumption	$P_D$	$V_S = \pm 15\text{ V}$ , No Load		60	75		60	75		60	75	mW
Supply Current	$I_{SY}$	$V_S = \pm 15\text{ V}$ , No Load		2.0	2.5		2.0	2.5		2.0	2.5	mA

### NOTES

<sup>1</sup>OP177E:  $\text{TCV}_{OS}$  is 100% tested.

<sup>2</sup>Guaranteed by endpoint limits.

<sup>3</sup>Guaranteed by CMRR test condition.

<sup>4</sup>To insure high open-loop gain throughout the  $\pm 10\text{ V}$  output range,  $A_{VO}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

Specifications subject to change without notice.

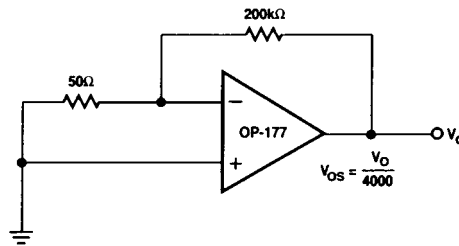


Figure 2. Typical Offset Voltage Test Circuit

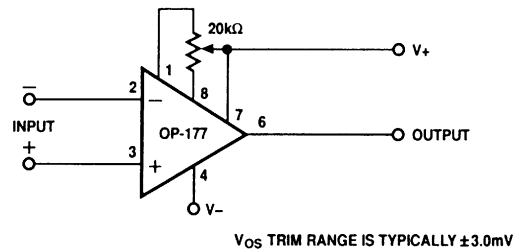
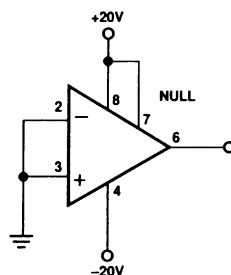


Figure 3. Optional Offset Nulling Circuit



PINOUTS SHOWN FOR P AND Z PACKAGES

Figure 4. Burn-In Circuit

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	±22 V
Internal Power Dissipation <sup>1</sup>	500 mW
Differential Input Voltage	±30 V
Input Voltage	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
Z and RC Packages	-65°C to +150°C
S, P Package	-65°C to +125°C
Operating Temperature Range	
OP177A, OP177B	-55°C to +125°C
OP177E, OP177F, OP177G	-40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	+300°C
DICE Junction Temperature (T <sub>J</sub> )	-65°C to +150°C

Package Type	$\theta_{JA}$ <sup>2</sup>	$\theta_{JC}$	Units
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES

<sup>1</sup>For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

<sup>2</sup> $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for cerdip, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
OP177AZ	-55°C to +125°C	8-Pin Cerdip	Q-8
OP177BZ	-55°C to +125°C	8-Pin Cerdip	Q-8
OP177EZ	-40°C to +85°C	8-Pin Cerdip	Q-8
OP177FZ	-40°C to +85°C	8-Pin Cerdip	Q-8
OP177GZ	-40°C to +85°C	8-Pin Cerdip	Q-8
OP177FP	-40°C to +85°C	8-Pin Plastic DIP	N-8
OP177GP	-40°C to +85°C	8-Pin Plastic DIP	N-8
OP177BRC/883	-55°C to +125°C	20-Pin LCC	E-20A
OP177FS	-40°C to +85°C	8-Pin SO	SO-8
OP177GS	-40°C to +85°C	8-Pin SO	SO-8

# OP177—Typical Performance Characteristics

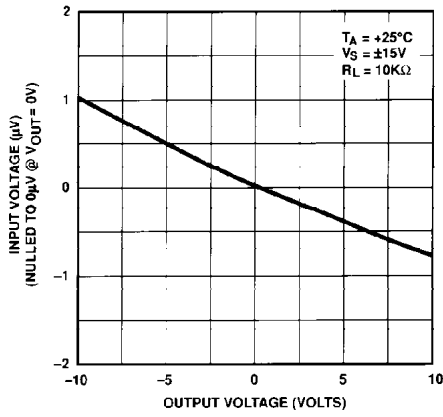


Figure 5. Gain Linearity (Input Voltage vs. Output Voltage)

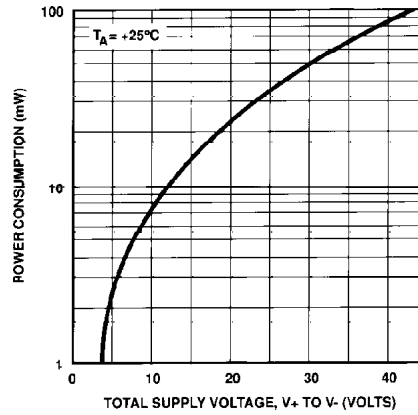


Figure 6. Power Consumption vs. Power Supply

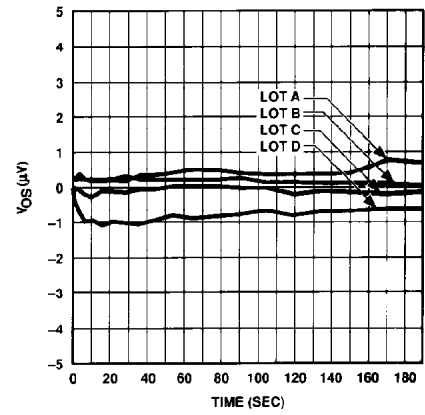


Figure 7. Warm-Up  $V_{OS}$  Drift (Normalized) Z Package

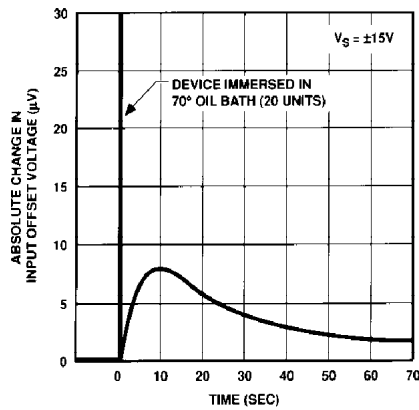


Figure 8. Offset Voltage Change Due to Thermal Shock

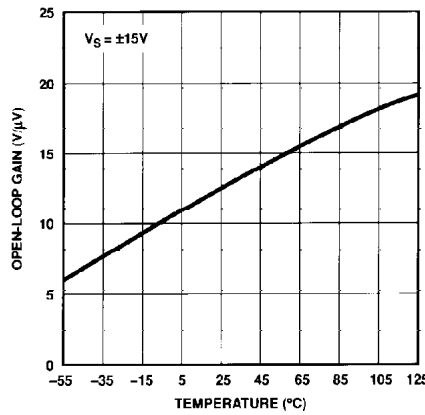


Figure 9. Open-Loop Gain vs. Temperature

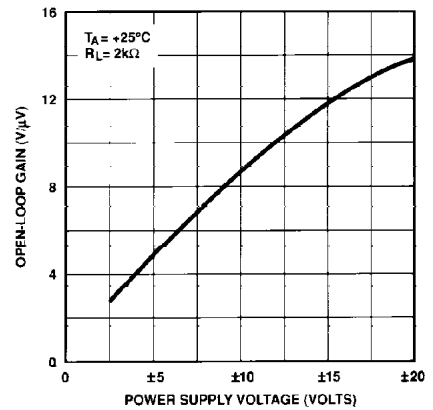


Figure 10. Open-Loop Gain vs. Power Supply Voltage

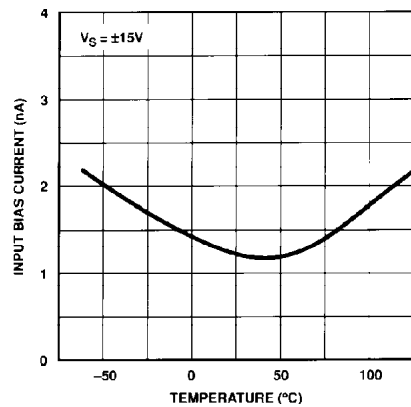


Figure 11. Input Bias Current vs. Temperature

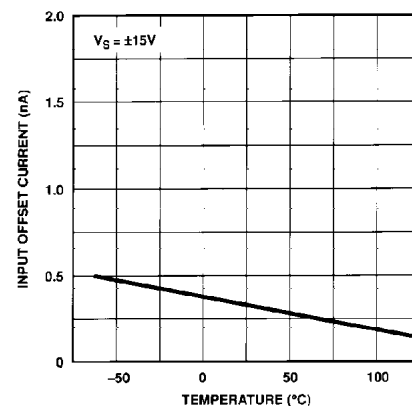


Figure 12. Input Offset Current vs. Temperature

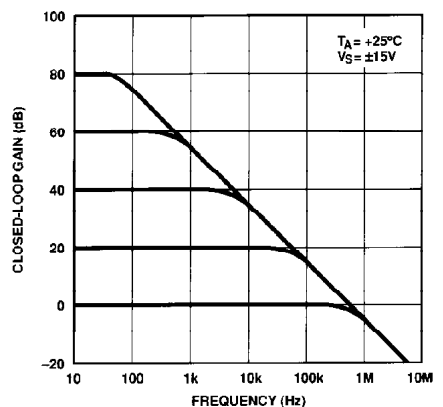


Figure 13. Closed-Loop Response for Various Gain Configurations

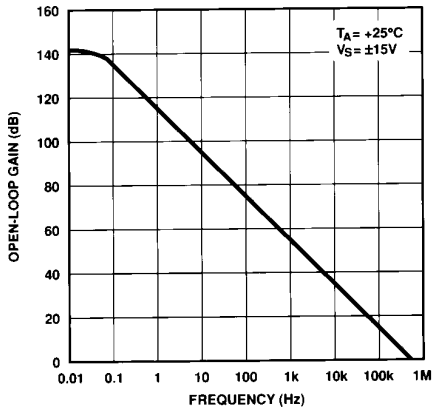


Figure 14. Open-Loop Frequency Response

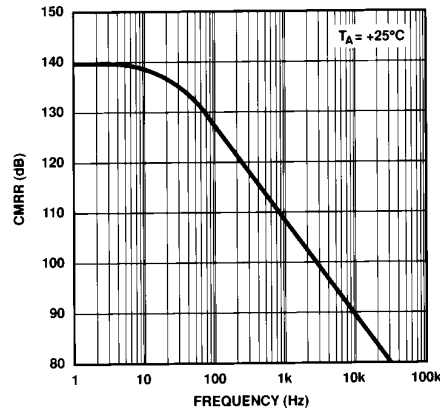


Figure 15. CMRR vs. Frequency

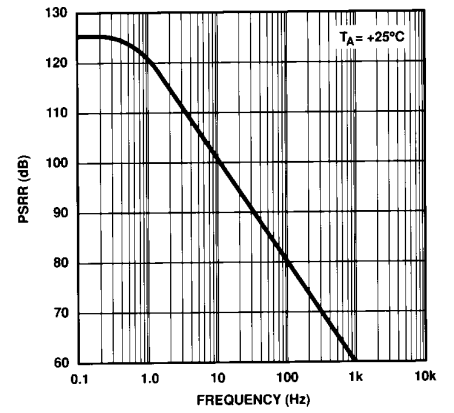


Figure 16. PSRR vs. Frequency

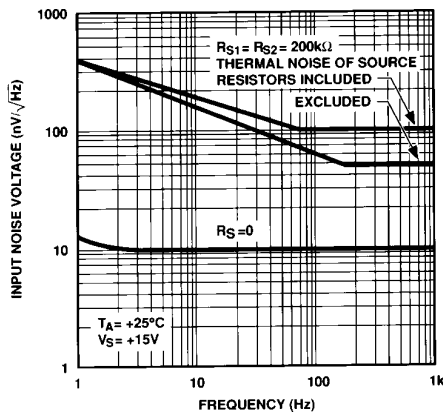


Figure 17. Total Input Noise Voltage vs. Frequency

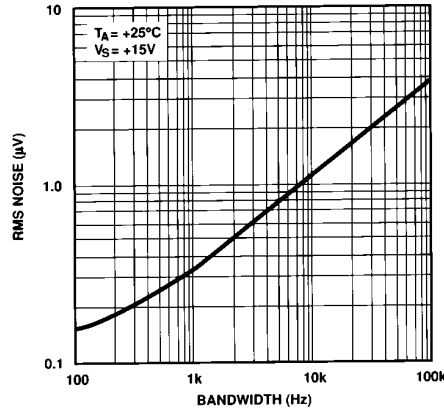


Figure 18. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

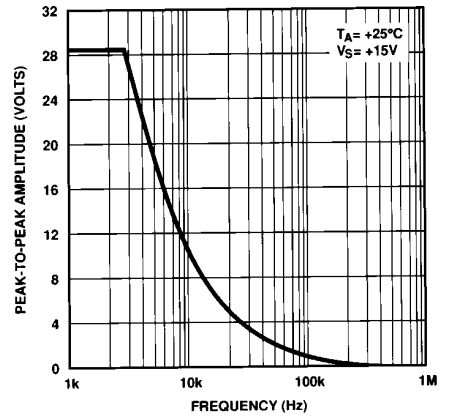


Figure 19. Maximum Output Swing vs. Frequency

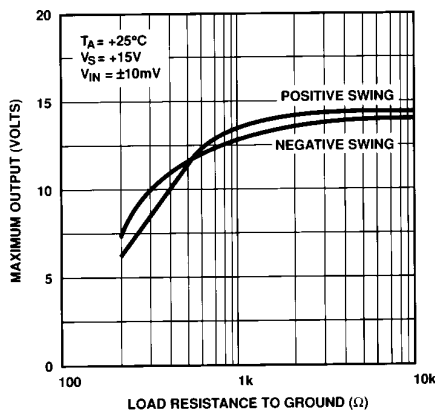


Figure 20. Maximum Output Voltage vs. Load Resistance

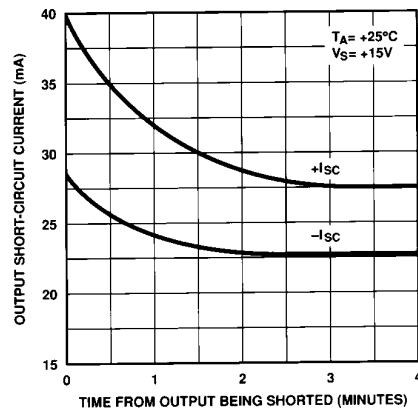


Figure 21. Output Short Circuit Current vs. Time

# OP177

## APPLICATIONS INFORMATION

### Gain Linearity

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's  $A_{VO}$  specification is only a part of the solution, since all automated testers use endpoint testing and, therefore, only show the average gain. For example, Figure 22 shows a typical precision op amp with a respectable open-loop gain of 650 V/mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal op amp would show a horizontal scope trace.

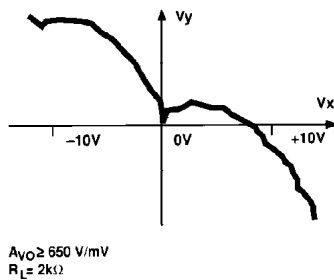


Figure 22. Typical Precision Op Amp

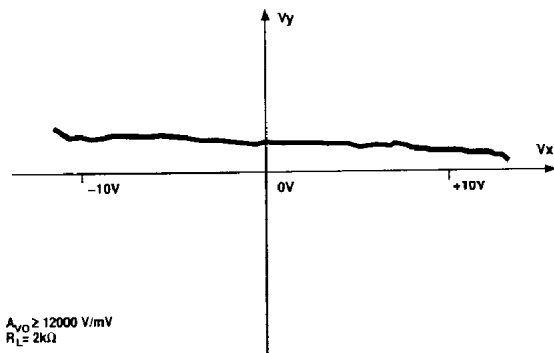


Figure 23. OP177's Output Gain Linearity Trace

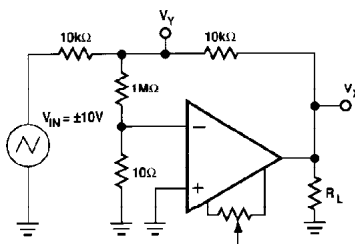


Figure 24. Open-Loop Gain Linearity Test Circuit

Figure 23 shows the OP177's output gain linearity trace with its truly impressive average  $A_{VO}$  of 12000 V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. PMI also performs additional testing to insure consistent high open-loop gain at various output voltages.

Figure 24 is a simple open-loop gain test circuit for your own evaluation.

## THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must amplify very low level signals accurately without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple, which has a Seebeck coefficient of  $10.3 \mu\text{V}/^\circ\text{C}$ , produces 10.3 mV of output voltage at a temperature of  $1,000^\circ\text{C}$ . The amplifier gain is set at 973.16. Thus, it will produce an output voltage of 10.024 V. Extended temperature ranges to beyond  $1,500^\circ\text{C}$  can be accomplished by reducing the amplifier gain. The circuit uses a low-cost diode to sense the temperature at the terminating junctions and in turn compensates for any ambient temperature change. The OP177, with its high open-loop gain, plus low offset voltage and drift combines to yield a very precision temperature sensing circuit. Circuit values for other thermocouple types are shown in Table I.

Table I.

Thermocouple Type	Seebeck Coefficient	R1	R2	R7	R9
K	$39.2 \mu\text{V}/^\circ\text{C}$	110 $\Omega$	5.76 k $\Omega$	102 k $\Omega$	269 k $\Omega$
J	$50.2 \mu\text{V}/^\circ\text{C}$	100 $\Omega$	4.02 k $\Omega$	80.6 k $\Omega$	200 k $\Omega$
S	$10.3 \mu\text{V}/^\circ\text{C}$	100 $\Omega$	20.5 k $\Omega$	392 k $\Omega$	1.07 M $\Omega$

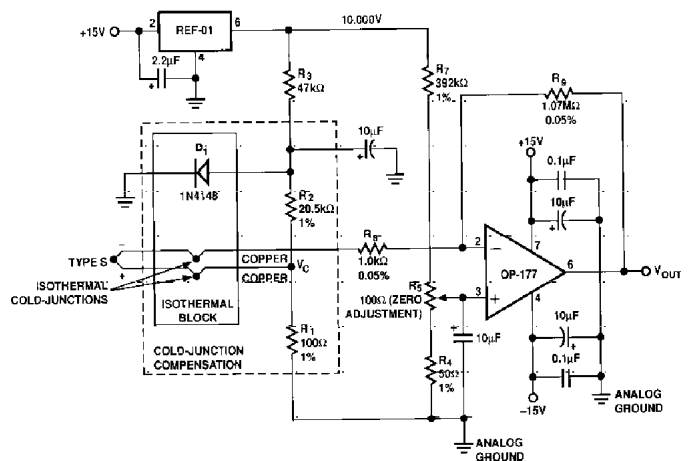


Figure 25. Thermocouple Amplifier with Cold Junction Compensation

## PRECISION HIGH GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low  $\text{TCV}_{OS}$  of the OP177 make it possible to obtain performance not previously available in single stage, very high-gain amplifier applications. See Figure 26.

For best CMR,  $\frac{R1}{R2}$  must equal  $\frac{R3}{R4}$ . In this example, with a 10 mV differential signal, the maximum errors are as listed in Table II.



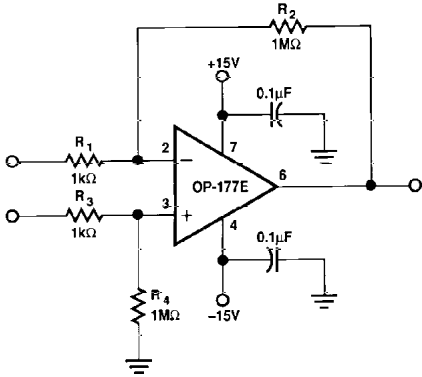


Figure 26. Precision High Gain Differential Amplifier

Table II. High Gain Differential Amp Performance

Type	Amount
Common-Mode Voltage	0.1%/V
Gain Linearity, Worst Case	0.02%
TCV <sub>OS</sub>	0.0003%/°C
TCI <sub>OS</sub>	0.008%/°C

**ISOLATING LARGE CAPACITIVE LOADS**

The circuit in Figure 27 reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100 Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP177.

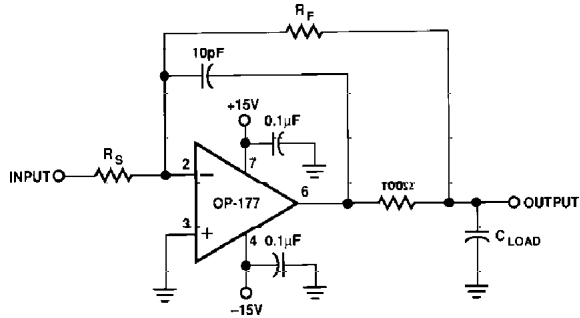
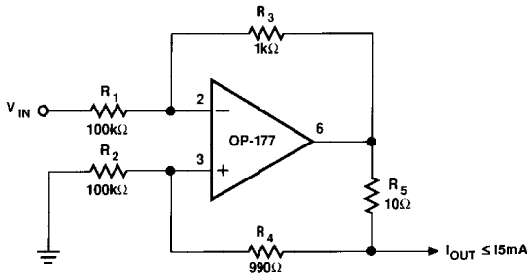
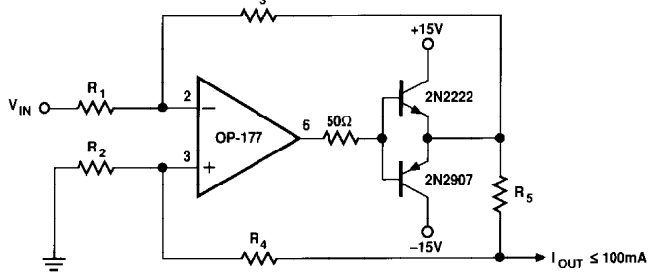


Figure 27. Isolating Capacitive Loads

**BASIC CURRENT SOURCE**



**100mA CURRENT SOURCE**



$$I_{OUT} = V_{IN} \frac{R_3}{R_1 \cdot R_5}$$

GIVEN  $R_3 = R_4 + R_5$ ,  $R_1 = R_2$

Figure 28. Bilateral Current Source

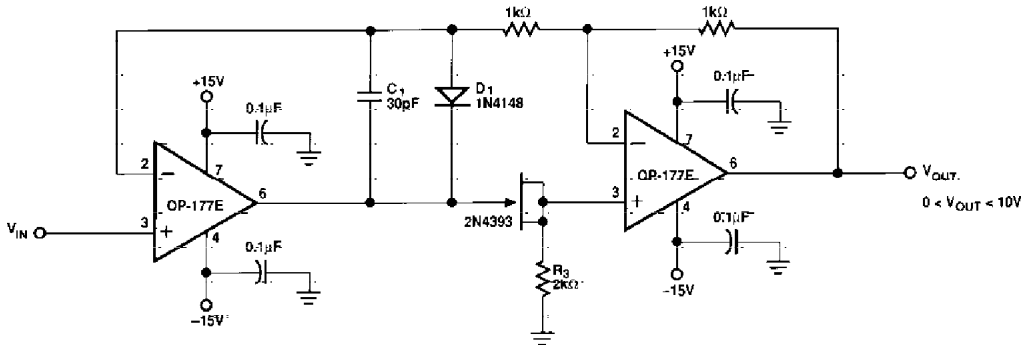


Figure 29. Precision Absolute Value Amplifier

# OP177

## BILATERAL CURRENT SOURCE

The current sources shown in Figure 28 will supply both positive and negative current into a grounded load.

$$\text{Note that } Z_O = \frac{R5 \left( \frac{R4}{R2} + 1 \right)}{\frac{R5 + R4}{R2} - \frac{R3}{R1}}$$

and that for  $Z_O$  to be infinite,

$$\frac{R5 + R4}{R2} \text{ must} = \frac{R3}{R1}$$

## PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low  $TCV_{OS}$  assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP177E CMRR of 140 dB assures errors of less than 1 ppm. See Figure 29.

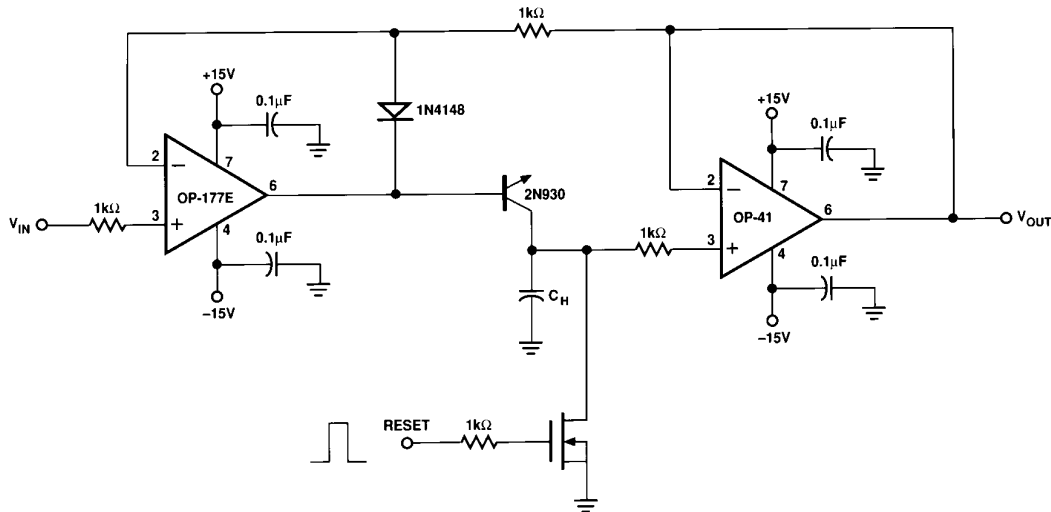


Figure 30. Precision Positive Peak Detector

## PRECISION POSITIVE PEAK DETECTOR

In Figure 30, the  $C_H$  must be of polystyrene, Teflon\*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of  $C_H$  and the bias current of the OP41.

## PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 32, when  $V_{IN} < V_{TH}$ , amplifier output swings negative, reverse biasing diode  $D_1$ .  $V_{OUT} = V_{TH}$  if  $R_L = \infty$ . When  $V_{IN} \geq V_{TH}$ , the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left( 1 + \frac{R_F}{R_S} \right)$$

$C_C$  is selected to smooth the response of the loop.

\*Teflon is a registered trademark of the Dupont Company.

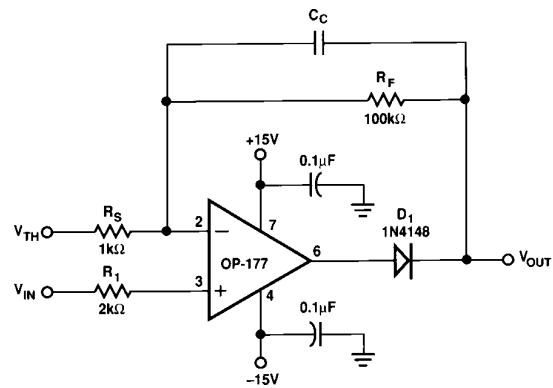
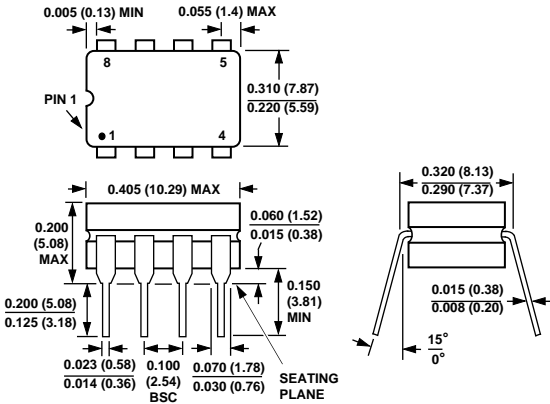


Figure 31. Precision Threshold Detector/Amplifier

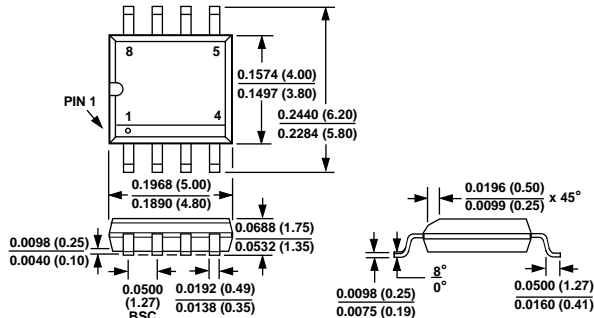
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

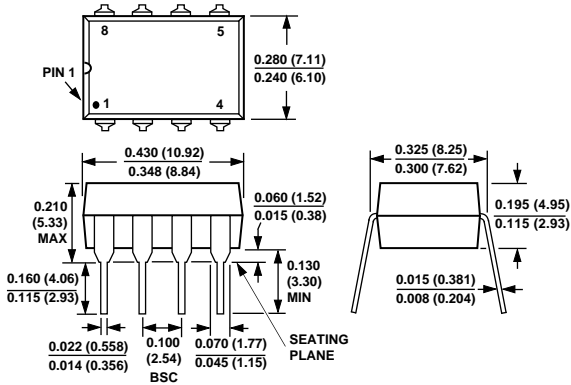
**8-Pin Cerdip  
(Q-8)**



**8-Pin SO  
(SO-08)**



**8-Pin Plastic DIP  
(N-8)**



**20-Pin LCC  
(E-20A)**

