19-4452; Rev 1; 5/92

MAXIM

Serially Interfaced, 8-Digit LED Display Driver

General Description

The MAX7219 is a compact, serial input/output common-cathode display driver that interfaces microprocessors (µPs) to 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. Only one external resistor is required to set the segment current for all LEDs.

A convenient 3-wire serial interface connects to all common µPs. Individual digits may be addressed and updated without rewriting the entire display. The MAX7219 also allows the user to select code-B decoding or no-decode for each digit.

The MAX7219 includes a 150µA low-power shutdown mode, analog and digital brightness control, a scan-limit register which allows the user to display from 1 to 8 digits, and a test mode which forces all LEDs on.

Applications

Bar-Graph Displays

7-Segment Displays

Industrial Controllers

Panel Meters

LED Matrix Displays

Features

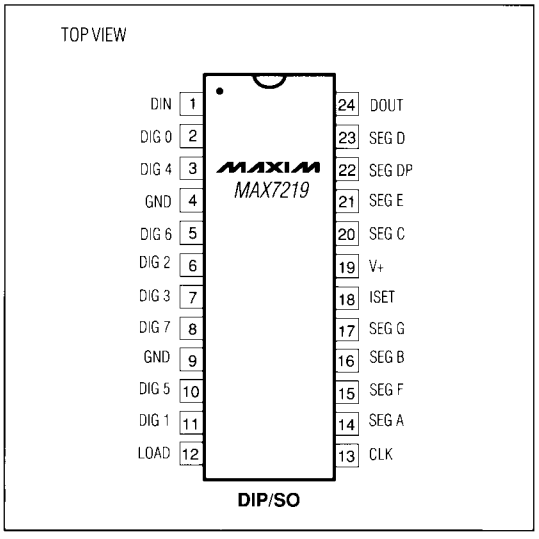
- ♦ **10MHz Serial Interface**
- ♦ **Individual LED Segment Control**
- ♦ **Decode/No-Decode Digit Selection**
- ♦ **150µA Low-Power Shutdown (Data Retained)**
- ♦ **Digital and Analog Brightness Control**
- ♦ **Display Blanked on Power-Up**
- ♦ **24-Pin DIP and SO Packages**
- ♦ **Drives Common-Cathode LED Display**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX7219CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX7219CWG	0°C to +70°C	24 Wide SO
MAX7219C/D	0°C to +70°C	Dice*
MAX7219ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX7219EWG	-40°C to +85°C	24 Wide SO
MAX7219ERG	-40°C to +85°C	24 Narrow CERDIP

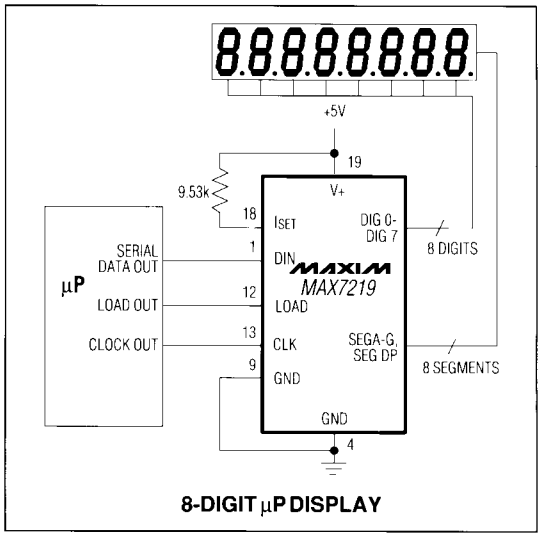
* *Contact factory for dice specifications.*

Pin Configuration



DIP/SO

Typical Application Circuit



8-DIGIT µP DISPLAY

Serially Interfaced, 8-Digit LED Display Driver

ABSOLUTE MAXIMUM RATINGS

V+ Voltage 7V
DIG0-DIG7 Sink Current 500mA
SEG A-G, DP Source Current 100mA
Input Voltage (any pin) ..... V+ + 0.3V to -0.3V
Continuous Power Dissipation (T_A = +85°C)
Narrow Plastic DIP 0.87W
Wide SO 0.76W
CERDIP 1.1W

Operating Temperature Ranges:
MAX7219C_G ..... 0°C to +70°C
MAX7219E_G ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V ±10%, R_{SET} = 9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

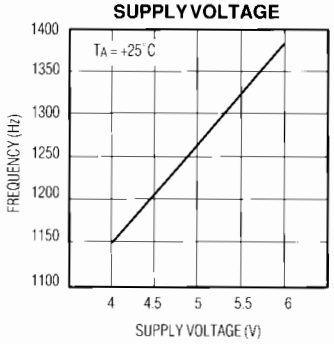
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		4.0		6.0	V
Shutdown Supply Current	I_Q	DIN,CLK and LOAD = GND or V+, shutdown register set to 0, T_A = +25°C			150	µA
Operating Supply Current	I_{OP}	R_{SET} = infinity			8	mA
		All segments and decimal points on, I_{SEGO} = -40mA		330		mA
Display Scan Rate	f_{OSC}	V+ = 5V, 8 digits scanned	500	1300	2000	Hz
Digit Drive Sink Current	I_{DIGI}	T_A = +25°C, V+ = 5V, V_{OUT} = 0.65V	320			mA
Segment Drive Current Source	I_{SEGO}	T_A = +25°C, V+ = 5V, V_{OUT} =V+ - 1V	-30	-37	-40	mA
Segment Drive Current Matching				3.0		%
Digit Drive Source Current	I_{DIGO}	Digit off, V_{OUT} = V+ - 0.3V	-2			mA
Segment Drive Current Sink	I_{SEGI}	Segment off, V_{OUT} = 0.3V	5			mA
LOGIC INPUTS						
Input Current	I	DIN, CLK and LOAD V_{IN} = 0V V_{IN} = V+			-1 1	µA
Logic 1 Input Voltage	V_{IH}		3.5			V
Logic 0 Input Voltage	V_{IL}				0.8	V
Hysteresis Voltage		DIN, CLK, and LOAD		1.0		V
Output High Voltage	V_{OH}	DOUT I_{OUT} = -1mA, I_{OUT} -1µA	V+-1.0	V+		V
Output Low Voltage	V_{OL}	DOUT, I_{OUT} = 1.6mA			0.4	V
Data-Hold Time DATAIN to Clock	t_{IDH}		0	-5		ns
Data-Setup Time DATAIN To Clock	t_{IDS}		25			ns
Clock-to-Serial Output Prop Delay	t_{OPD}	C_{LOAD} = 50pF			25	ns
Clock Low Time	t_{CKL}		50			ns
Clock High Time	t_{CKH}		50			ns
Data-to-Segment Prop Delay (Note 1)	t_{DSPD}	C_{LOAD} = 50pF	0		2.25	ms
Load-Rising Edge to Next Clock Rising Edge	t_{LDCK}		50			ns
Clock-to-Load Rising Edge Setup Time	t_{CKLD}		0			ns
Load Low Time	t_{LDL}		50			ns
Load High Time	t_{LDH}		50			ns

Note 1: Guaranteed by design.

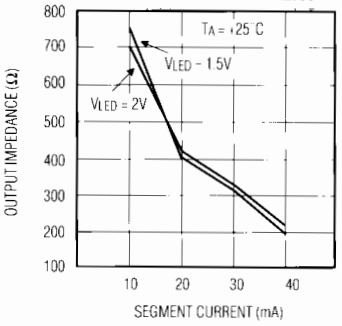
Serially Interfaced, 8-Digit LED Display Driver

Typical Operating Characteristics

SCAN FREQUENCY vs. SUPPLY VOLTAGE



SEGMENT DRIVER OUTPUT IMPEDANCE vs. SEGMENT CURRENT



Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input. Data is loaded into an internal 16-bit shift register on the rising edge of CLK.
2, 3, 5-8, 10, 11	DIG0-7	8 digit drive lines that sink current from the display.
4, 9	GND	Ground (both GND pins must be connected)
12	LOAD	Load Data Input. On LOAD's rising edge, the last 16 bits of serial input data are latched.
13	CLK	Clock Input. 10MHz maximum rate. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT.
14-17, 20-23	SEG A-G, DP	7-segment drive and decimal point lines that source current to the display.
18	ISET	Connect to V+ through a resistor (R_{SET}) to set the peak segment current (Refer to "*Selecting R_{SET} Resistor*" section).
19	V+	Supply Voltage
24	DOUT	Serial Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later.

Block Diagram

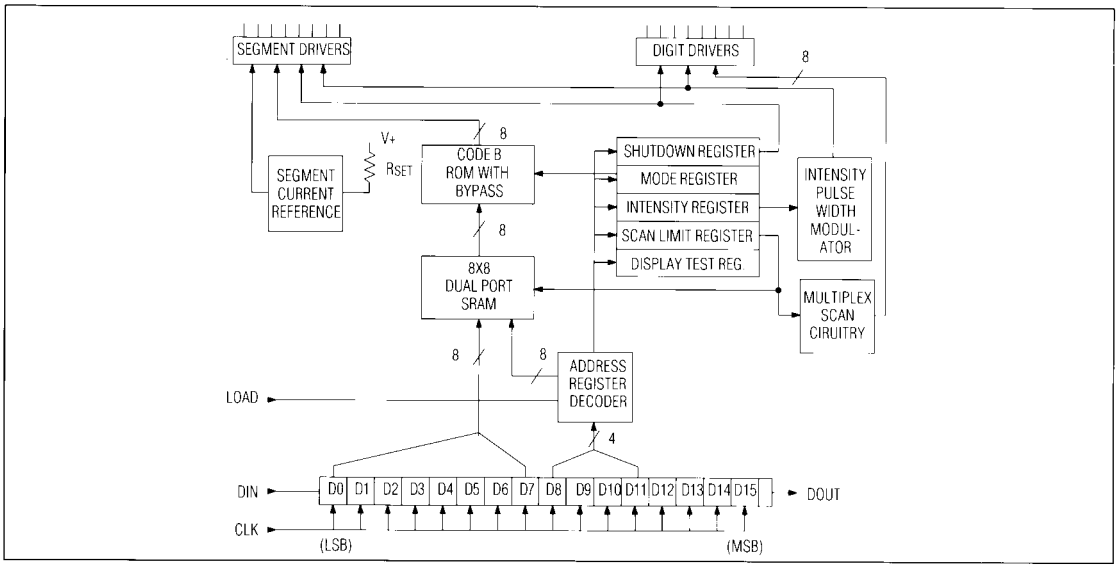


TABLE 1. SERIAL DATA FORMAT (16 BITS)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB	DATA						LSB

X = "don't care" bit

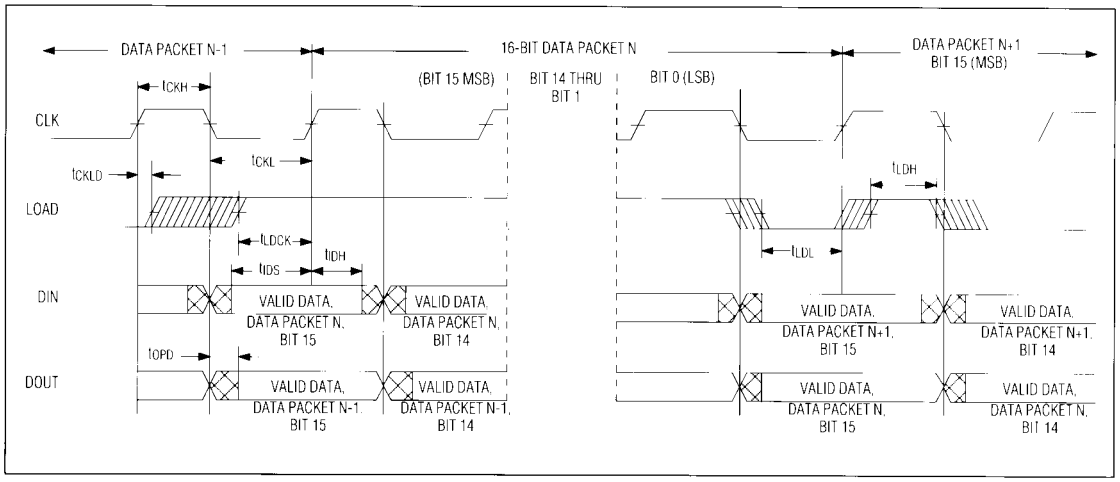


Figure 1. Timing Diagram

Detailed Description

Serial Addressing Modes

Serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK. The data is then latched into either the digit or control registers on the rising edge of LOAD. LOAD must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0-D15 (Table 1). D8-D11 contain the register address, D0-D7 contain the data, and D12-D15 are "don't care" bits. The first bit received is D15, the most significant bit (MSB).

Digit and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip, 8x8 dual-port SRAM. They are addressed directly so that individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of: decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on). A no-operation (no-op) register is also included, which allows data to be passed from DIN to DOUT when devices are cascaded without changing the display or affecting any control registers.

Shutdown Mode

When the MAX7219 is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving the shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS logic levels).

Typically, it takes less than 250µs for the MAX7219 to leave shutdown mode. Note that the display driver can still be programmed while in shutdown mode, and that shutdown mode can be overridden by the display-test function.

Table 2. Register Address Map

REGISTER	ADDRESS					HEX CODE
	D15-D12	D11	D10	D9	D8	
NO-OP	X	0	0	0	0	X0
DIGIT 0	X	0	0	0	1	X1
DIGIT 1	X	0	0	1	0	X2
DIGIT 2	X	0	0	1	1	X3
DIGIT 3	X	0	1	0	0	X4
DIGIT 4	X	0	1	0	1	X5
DIGIT 5	X	0	1	1	0	X6
DIGIT 6	X	0	1	1	1	X7
DIGIT 7	X	1	0	0	0	X8
DECODE MODE	X	1	0	0	1	X9
INTENSITY	X	1	0	1	0	XA
SCAN LIMIT	X	1	0	1	1	XB
SHUTDOWN	X	1	1	0	0	XC
DISPLAY TEST	X	1	1	1	1	XF

Table 3. Shutdown Register Format (Address (Hex) = XC)

	ADDR CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
SHUTDOWN MODE	XC	X	X	X	X	X	X	X	0
NORMAL OPERATION	XC	X	X	X	X	X	X	X	1

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX7219 enters shutdown mode. Therefore the user must program the display driver prior to display use since it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H, L, P, and -) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while a logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

Table 4. Decode-Mode Register Examples (Address (Hex) = X9)

	REGISTER DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
NO DECODE FOR DIGITS 7-0	0	0	0	0	0	0	0	0	00
CODE B DECODE FOR DIGIT 0 NO DECODE FOR DIGITS 7-1	0	0	0	0	0	0	0	1	01
CODE B DECODE FOR DIGITS 3-0 NO DECODE FOR DIGITS 7-4	0	0	0	0	1	1	1	1	0F
CODE B DECODE FOR DIGITS 7-0	1	1	1	1	1	1	1	1	FF

Serially Interfaced, 8-Digit LED Display Driver

Table 5. Code B Font

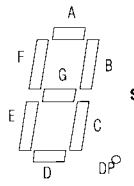
7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6-D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
-		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

* The decimal point is set by bit D7 = 1

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3-D0), disregarding bits D4-D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7=1 turns the decimal point on). The code-B font is listed in Table 5.

When no-decode is selected, data bits D7-D0 correspond to the segment lines of the MAX7219. Table 6 shows the one-to-one pairing of each data bit to the appropriate segment line.

Table 6. No-decode Mode Data Bits and Corresponding Segment Lines



STANDARD 7-SEGMENT LED

	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
CORRESPONDING SEGMENT LINE	DP	A	B	C	D	E	F	G

Intensity Control and Interdigit Blanking

The MAX7219 allows the display brightness to be controlled with an external resistor (R_{SET}) connected between V+ and ISET, and digitally using the intensity register. The peak current sourced from the segment drivers will nominally be 100 times the current entering ISET. This resistor can either be fixed, or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53kΩ, which typically sets the segment current at 37mA.

Digital control of segment current is provided by an internal pulse-width modulated DAC, which is loaded from the lower nibble of the intensity register. The DAC scales the average segment current in 16 steps from a maximum of 31/32, down to 1/32 of the peak current set by R_{SET}. The intensity register format is listed in Table 7. Maximum brightness occurs with a duty cycle of 31/32 because the interdigit blanking time is set to 1/32 of a cycle. Interdigit blanking time can be increased by decreasing the duty cycle.

Table 7. Intensity Register Format (Address (Hex) = XA)

DUTY CYCLE	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
1/32 (min on)	X	X	X	X	0	0	0	0	X0
3/32	X	X	X	X	0	0	0	1	X1
5/32	X	X	X	X	0	0	1	0	X2
7/32	X	X	X	X	0	0	1	1	X3
9/32	X	X	X	X	0	1	0	0	X4
11/32	X	X	X	X	0	1	0	1	X5
13/32	X	X	X	X	0	1	1	0	X6
15/32	X	X	X	X	0	1	1	1	X7
17/32	X	X	X	X	1	0	0	0	X8
19/32	X	X	X	X	1	0	0	1	X9
21/32	X	X	X	X	1	0	1	0	XA
23/32	X	X	X	X	1	0	1	1	XB
25/32	X	X	X	X	1	1	0	0	XC
27/32	X	X	X	X	1	1	0	1	XD
29/32	X	X	X	X	1	1	1	0	XE
31/32 (max on)	X	X	X	X	1	1	1	1	XF

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 1300Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is $8f_{OSC}/N$, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). The scan-limit register format is listed in Table 8.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the R_{SET} resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation. Table 9 lists the number of digits displayed and the corresponding maximum recommended segment current when the internal digit drivers are used.

Display-Test Register

The display-test register operates in two modes: normal and display test. Display-test mode turns all LEDs on by overriding - but not altering - all controls and digit registers (including the shutdown register). In display-test mode, 8 digits are scanned and the duty cycle is 31/32. Table 9 lists the display-test register format.

Table 8. Scan-Limit Register Format (Address (Hex) = XB)

	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0	(HEX CODE)
*DISPLAY DIGIT 0 ONLY	X	X	X	X	X	0	0	0	X0
*DISPLAY DIGITS 0 & 1	X	X	X	X	X	0	0	1	X1
*DISPLAY DIGITS 0 1 2	X	X	X	X	X	0	1	0	X2
DISPLAY DIGITS 0 1 2 3	X	X	X	X	X	0	1	1	X3
DISPLAY DIGITS 0 1 2 3 4	X	X	X	X	X	1	0	0	X4
DISPLAY DIGITS 0 1 2 3 4 5	X	X	X	X	X	1	0	1	X5
DISPLAY DIGITS 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	X6
DISPLAY DIGITS 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	X7

* See "*Scan-Limit Register*" text for application.

Table 9. Maximum Segment Current for 1, 2 or 3 Digit Displays

NUMBER OF DIGITS DISPLAYED	MAXIMUM SEGMENT CURRENT
1	10mA
2	20mA
3	30mA

Table 10. Display-Test Register Format (Address (Hex) = XF)

	REGISTER DATA D7	D6	D5	D4	D3	D2	D1	D0
NORMAL OPERATION	X	X	X	X	X	X	X	0
DISPLAY TEST MODE	X	X	X	X	X	X	X	1

Note: The MAX7219 remains in display-test mode (all LEDs on) until the display-test register is reconfigured for normal operation.

No-Op Register

The no-op register is used when cascading MAX7219s. Connect all devices' LOAD inputs together and connect DOUT to DIN on adjacent MAX7219s. DOUT is a CMOS logic level output that easily drives DIN of a successively cascaded MAX7219. Refer to the "*Serial Addressing Modes*" section for detailed information on serial input/output timing. For example, if four MAX7219s are cascaded, then to write to the fourth chip, send the desired 16-bit word, followed by three no-op codes (hex X0XX, see Table 2). When load goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

Serially Interfaced, 8-Digit LED Display Driver

Applications Information

Supply Bypassing and Wiring

To minimize power-supply ripple due to the peak digit driver currents, connect a 10µF electrolytic and a 0.1µF ceramic capacitor between V+ and GND as close to the device as possible. The MAX7219 should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electromagnetic interference. Also, both GND pins must be connected to ground.

Selecting R_{SET} Resistor and Using External Drivers

The current per segment is approximately 100 times the current in ISET. To select R_{SET}, see Table 11. The MAX7219's maximum allowable segment current is 40mA. For an LED forward voltage drop of 2.5V, R_{SET} must be greater than 9.53k. For segment current levels above the MAX7219 limits, external drivers will be needed. In this application, the MAX7219 serves as only a controller for other high-current drivers or transistors. Therefore, to conserve power in the MAX7219, use R_{SET} = 47k when using external current sources as segment drivers.

The example in Figure 2 uses the MAX7219's segment drivers, a MAX333 single-pole double-throw analog switch, and external transistors to drive 4.0" AND4107SCL common-cathode displays. The 5.6V zener diode has been added in series with the decimal point LED because the decimal point LED forward voltage is typically 4.2V, while for all other segments the LED forward voltage is typically 8V. Note that since external transistors are used to sink current (DIG 0 and DIG 1 are used as logic switches), peak segment currents of 40mA are allowed even though only two digits are displayed. In applications where the MAX7219's digit drivers are used to sink current and fewer than four digits are displayed, see Table 9 which specifies the maximum allowable segment current. R_{SET} must be selected accordingly (see Table 11).

Refer to the "Power Dissipation" section to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 11. RSET vs. Segment Current and LED Forward Voltage

	V_{LED} (V)				
I_{SEG} (mA)	1.5	2	2.5	3	3.5
40	11.3	10.4	9.8	8.9	7.8
30	16.3	15	14	12.9	11.4
20	26.2	24.6	22.8	20.9	18.6
10	60.1	56	51.7	47	41.9

Table 12. Package Thermal Resistance Data

PACKAGE	THERMAL RESISTANCE (θ_{JA})
24 Narrow DIP	+75°C/W
24 Wide SO	+85°C/W
24 CERDIP	+60°C/W
Maximum Junction Temperature (T_J) = +150°C	
Maximum Ambient Temperature (T_A) = +85°C	

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX7219 is determined from the following equation:

$$PD = (V+ \times 8mA) + (V+ - V_{LED})(DUTY \times I_{SEG} \times N)$$

where:

V+ = Supply Voltage

DUTY = Duty Cycle set by intensity register

N = number of segments driven (worst case is 8)

V_{LED} = LED forward voltage

I_{SEG} = Segment Current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V at 40mA, V+ = 5.25V

$$PD = 5.25V(8mA) + (5.25V - 1.8V)(31/32 \times 40mA \times 8)$$
$$= 1.11W$$

Thus, for a CERDIP package (θ_{JA} = +60C°/W from table 12), the maximum allowed ambient temperature T_A is given by:

$$T_{Jmax} = T_A + PD \times \theta_{JA}$$
$$+150°C = TA + 1.11W \times +60°C/W$$
$$T_A = +83.4°C$$

Cascading Drivers

The example in Figure 3 drives 16 digits using a 3-wire µP interface. If the number of digits is not a multiple of 8, set both drivers' scan-limit registers to the same number so one display will not appear brighter than the other. For example, if 12 digits are needed, use 6 digits per display

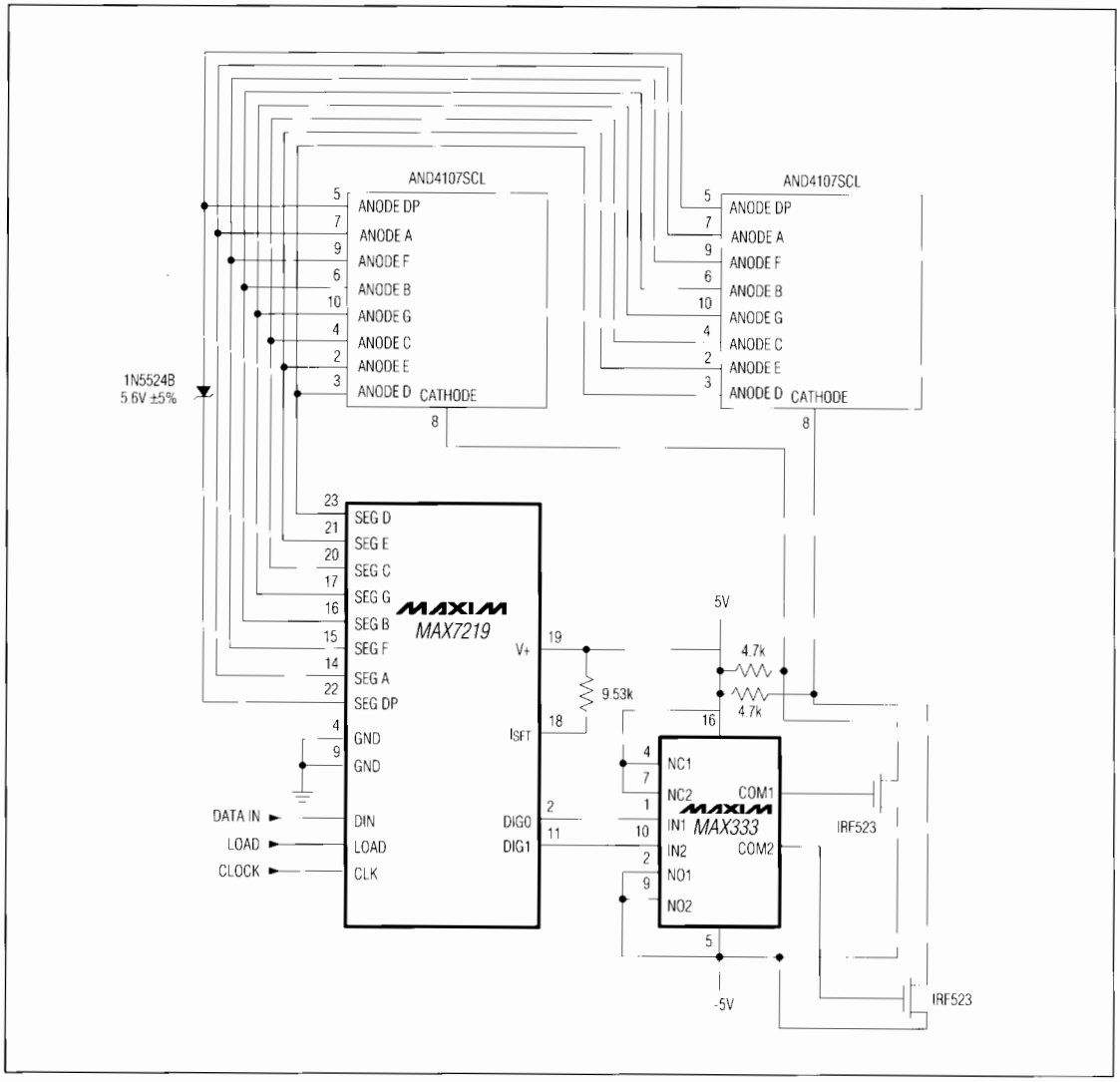


Figure 2. MAX7219 Driving 4 Inch Displays

Serially Interfaced, 8-Digit LED Display Driver

with both scan-limit registers set for 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both scan-limit registers for 6 digits and leave one digit driver unconnected. If one display is set for 6 digits and the other for 5 digits, the second display will appear brighter because its duty cycle per digit will be 1/5 while the first display's will be 1/6. Refer to the "No Op Register" section for additional information.

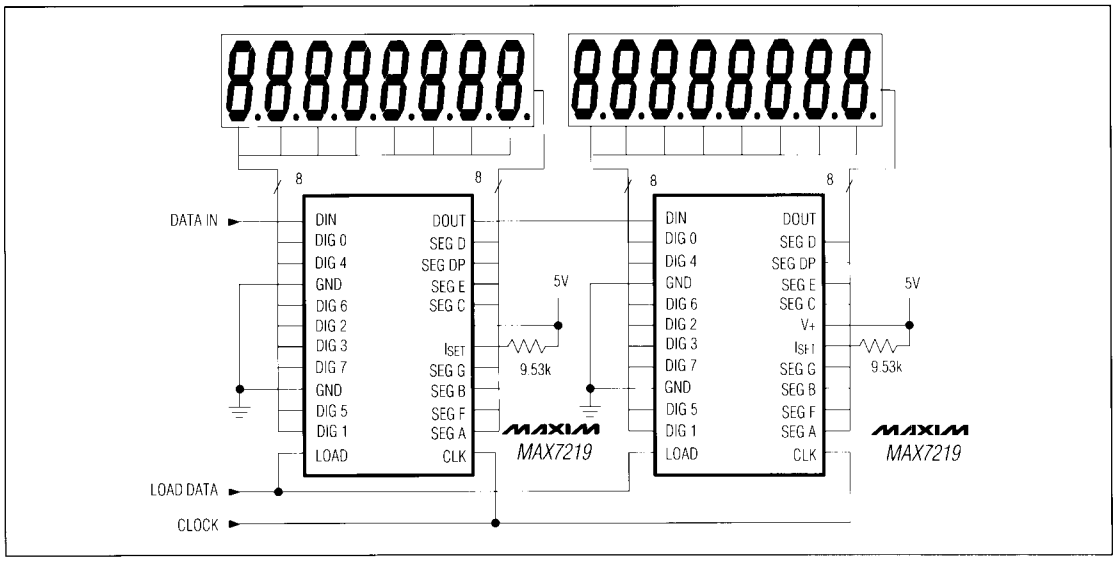


Figure 3. Cascading MAX7219s to drive 16 7-segment LED digits.

Chip Topography