PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

PE3503

3.5 GHz Low Power CMOS Divide-by-8 Prescaler

Features

- High-frequency operation: 1.5 GHz to 3.5 GHz
- Fixed divide ratio of 8
- Low-power operation: 12 mA typical @ 3 V across frequency
- Small package: 8-lead MSOP
- Low Cost

Product Description

The PE3503 is a high performance monolithic CMOS prescaler with a fixed divide ratio of 8. Its operating frequency range is 1.5 GHz to 3.5 GHz. The PE3503 operates on a nominal 3 V supply and draws only 12 mA. It is packaged in a small 8-lead MSOP and is ideal for microwave PLL synthesis solutions.

The PE3503 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi©) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

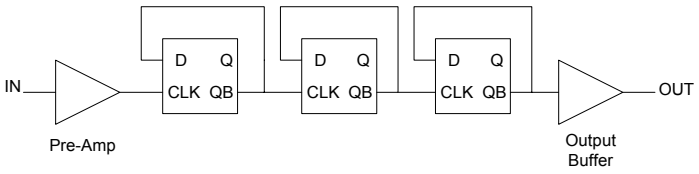


Figure 2. Package Drawing

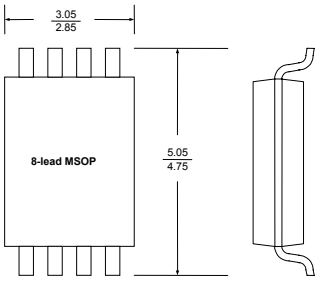


Table 1. Electrical Specifications ($Z_S = Z_L = 50\ \Omega$)

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			12	17	mA
Frequency Range (F_{IN})		1.5		3.5	GHz
Input Power (P_{IN})	1500 MHz ≤ F_{in} ≤ 3200 MHz	-10		+5	dBm
	3200 MHz < F_{in} ≤ 3500 MHz	0		+5	dBm
Output Power		-5			dBm

Figure 3. Pin Configuration

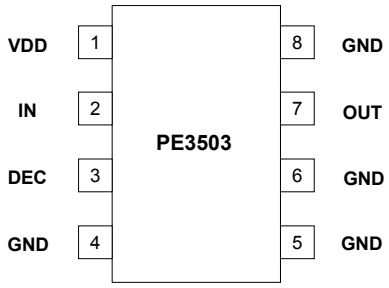


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	VDD	Power supply pin. Bypassing is required.
2	IN	Input signal pin. Should be coupled with a capacitor (eg 15pF)
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane (eg 10 nF and 10 pF).
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	GND	Ground pin.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 100 pF).
8	GND	Ground pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
VDD	Supply voltage		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
VESD	ESD voltage (Human Body Model)	250		V
P_{INMAX}	Maximum input power		10	dBm

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Functional Considerations

The PE3503 takes an input signal frequency from 1.5 GHz to 3.5 GHz and produces an output signal frequency one-eighth that of the supplied input. In order for the prescaler to work properly, several conditions need to be adhered to. It is crucial that pin 3 be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7, respectively) need to be AC coupled via an external capacitor as shown in the test circuit in Figure 7.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Typical Performance Data

Figure 4. Input Sensitivity

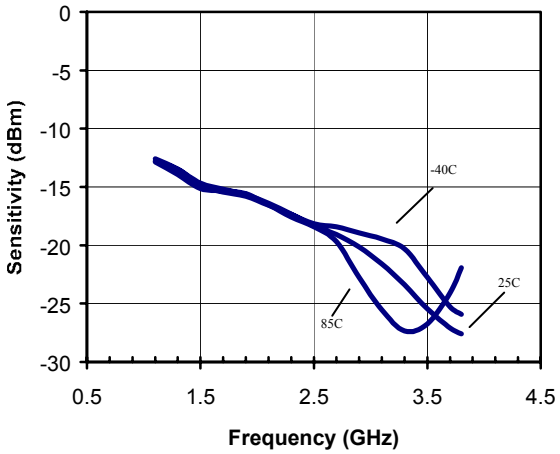


Figure 5. Device Current

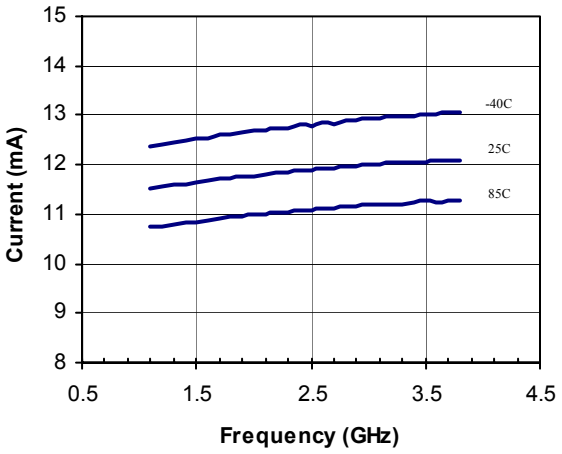


Figure 6. Output Power

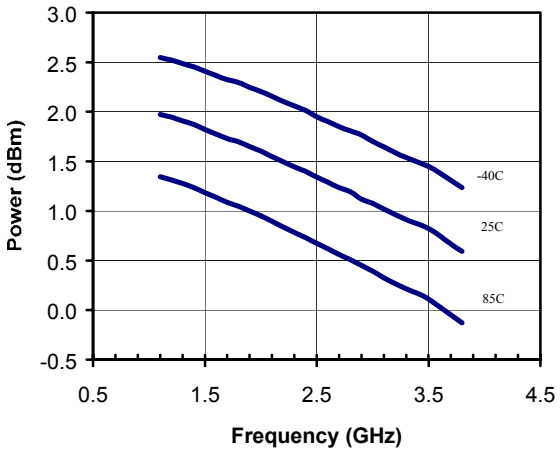


Figure 7. Test Circuit Block Diagram

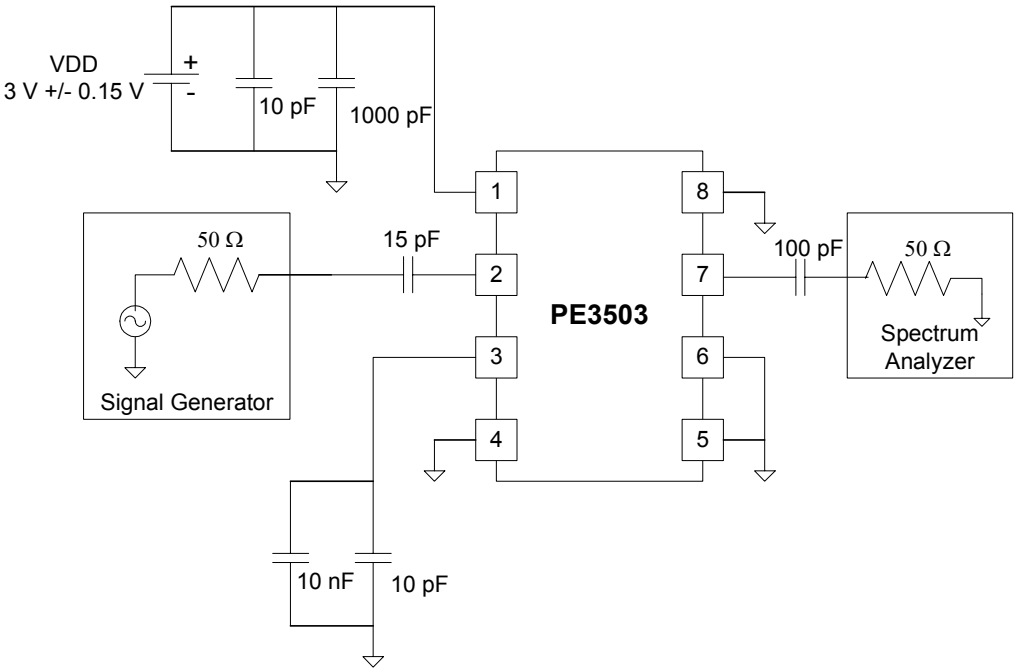


Figure 8. High Frequency System Application

The wideband frequency of operation of the PE3503 makes it an ideal part for use in a DBS downconverter system.

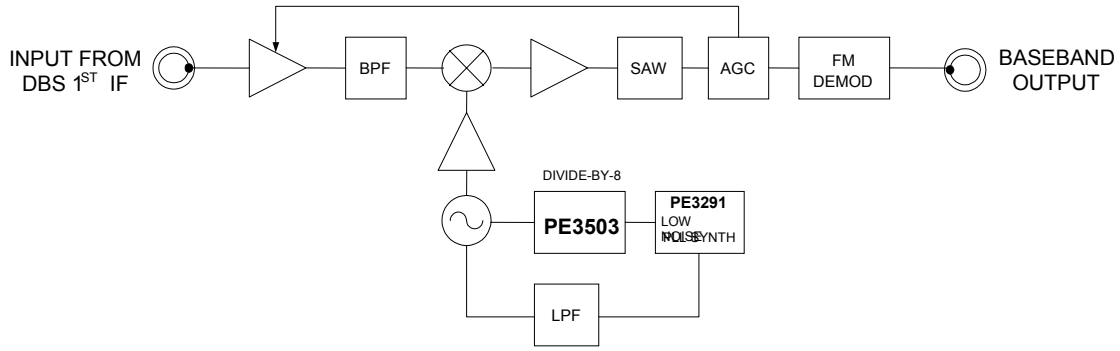


Figure 9. Evaluation Board Schematic Diagram

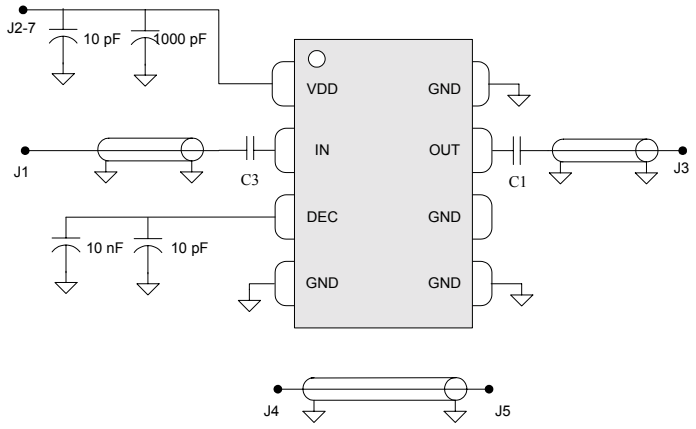
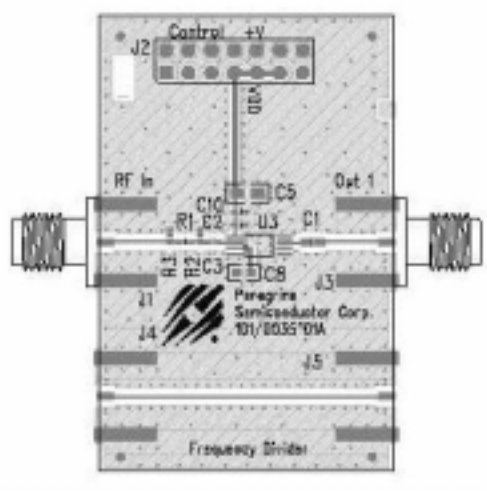


Figure 10. Evaluation Board Layout



Evaluation Kit Operation

The MSOP Prescaler Evaluation Board was designed to help customers evaluate the *PE3503* Divide-by-8 Prescaler. On this board, the device input (pin 2) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 15pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have a low impedance at the desired output frequency the device. The value of 100pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ε_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide.

J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device VDD pin (1). Two decoupling capacitors (10 pF, 1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

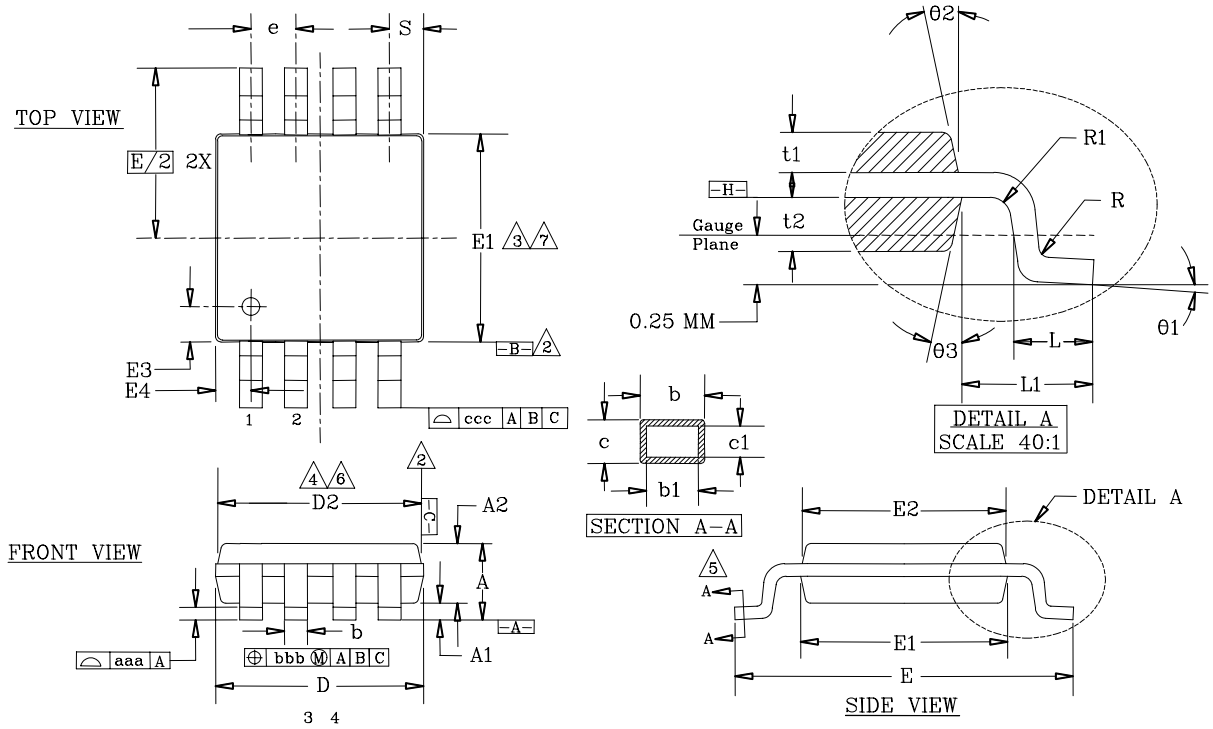
The DEC pin (3) must be connected to a low impedance AC ground for proper device operation. On the board, two decoupling capacitors (C6 = 10 nF, C4 = 10 pF), located on the back of the board, perform this function.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 455-0660 and ask for applications support. You may also contact us by fax or e-mail:

Fax: (858) 455-0770
E-Mail: help@peregrine-semi.com

Figure 11. Package Drawing



SYMBOL	MINI SOIC 8LD PACKAGE OUTLINE	
	(MILLIMETER)	±TOL
A	1.10	MAX
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	$^{+0.15}_{-0.08}$
R1	0.15	$^{+0.15}_{-0.08}$
t1	0.31	±0.08
t2	0.41	±0.08
b	0.33	$^{+0.07}_{-0.08}$
b1	0.30	±0.05
c	0.18	±0.05
c1	0.15	$^{+0.03}_{-0.02}$
θ1	3.0°	±3.0°
θ2	12.0°	±3.0°
θ3	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	———
aaa	0.10	———
bbb	0.08	———
ccc	0.25	———
e	0.65 BSC	———
S	0.525 BSC	———

Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3503-21	3503		8-lead MSOP	50 pcs. / Tube
3503-22	3503		8-lead MSOP	2000 pcs. / T&R
3503-00	PE3503-EK		Evaluation Board	1 / Box

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.