

# PE3513

## Product Description

The PE3513 is a high-performance static CMOS prescaler with a fixed divide ratio of 8. Its operating frequency range is DC to 1000 MHz. The PE3513 operates on a nominal 3 V supply and draws only 8 mA. It is packaged in a small 6-lead SC-70 and is ideal for frequency scaling solutions.

The PE3513 is manufactured in Peregrine's patented Ultra-Thin Silicon (UTSi<sup>®</sup>) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

## 1000 MHz Low Power CMOS Divide-by-8 Prescaler

### Features

- DC to 1000 MHz operation
- Fixed divide ratio of 8
- Low-power operation: 8 mA typical @ 3 V
- Ultra small package: 6-lead SC-70

Figure 1. Functional Schematic Diagram

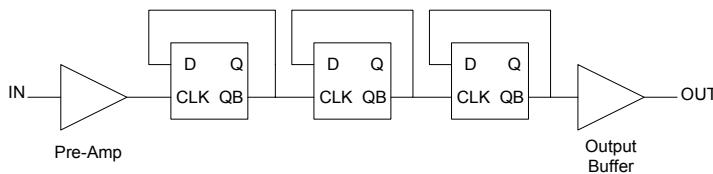


Figure 2. Package Type

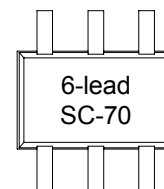


Table 1. Electrical Specifications ( $Z_S = Z_L = 50 \Omega$ )

$V_{DD} = 3.0 \text{ V}$ ,  $-40^\circ \text{ C} \leq T_A \leq 85^\circ \text{ C}$ , unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			8	12	mA
Input Frequency ( $F_{in}$ )		DC		1000	MHz
Input Power ( $P_{in}$ )	$DC \leq F_{in} \leq 1000\text{MHz}$	-10		+10	dBm
Output Power ( $P_{out}$ )	$DC \leq F_{in} \leq 1000\text{MHz}$	0			dBm

**Table 2. DC Electrical Characteristics (-40° C ≤ T<sub>A</sub> ≤ 85° C)**

Symbol	Parameter	Condition	Typical	Unit
V <sub>IH</sub>	High Level Input Voltage	2.7 V ≤ VDD ≤ 3.3 V	2.0	V
V <sub>IL</sub>	High Level Input Voltage	2.7 V ≤ VDD ≤ 3.3 V	0.8	V
V <sub>OH</sub>	High Level Output Voltage	VDD = 2.7 V; I <sub>OH</sub> = 2.9 mA	2.2	V
V <sub>OL</sub>	Low Level Output Voltage	VDD = 2.7 V; I <sub>OL</sub> = 2.6 mA	0.4	V

**Table 3. AC Characteristics (-40° C ≤ T<sub>A</sub> ≤ 85° C)**

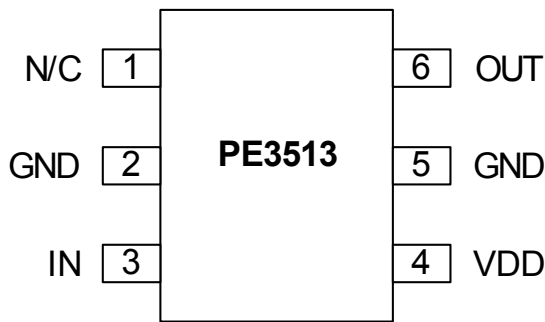
Symbol	Parameter	Condition*	Typical	Unit
t <sub>PHL</sub>	Propagation Delay (High to Low)	50 MHz Pulse Train Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	4.1	ns
t <sub>PLH</sub>	Propagation Delay (Low to High)	50 MHz Pulse Train Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	3.9	ns
t <sub>r</sub>	Output Rise Time (10% to 90%)	50 MHz Pulse Train Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	2.0	ns
t <sub>f</sub>	Output Fall Time (90% to 10%)	50 MHz Pulse Train Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	2.0	ns

\* See figure 5 for AC test circuit

**Table 4. Typical Output Swing (VDD = 2.7 V)**

Frequency	Condition	Typical	Unit
50 MHz	200 mVp-p Sinusoidal Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	2.3	Vp-p
500 MHz	200 mVp-p Sinusoidal Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	2.3	Vp-p
1000 MHz	200 mVp-p Sinusoidal Input; C <sub>L</sub> = 10 pF, R <sub>L</sub> = 500 Ω	2.2	Vp-p

**Figure 3. Pin Configuration**



**Electrostatic Discharge (ESD) Precautions**

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 5.

**Latch-Up Avoidance**

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

**Device Functional Considerations**

The PE3513 divides an input signal, up to a frequency of 1000 MHz, by a factor of eight thereby producing an output frequency at one-eighth the input frequency. To work properly, the input and output signals (pins 3 & 6) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 7 for a layout example.

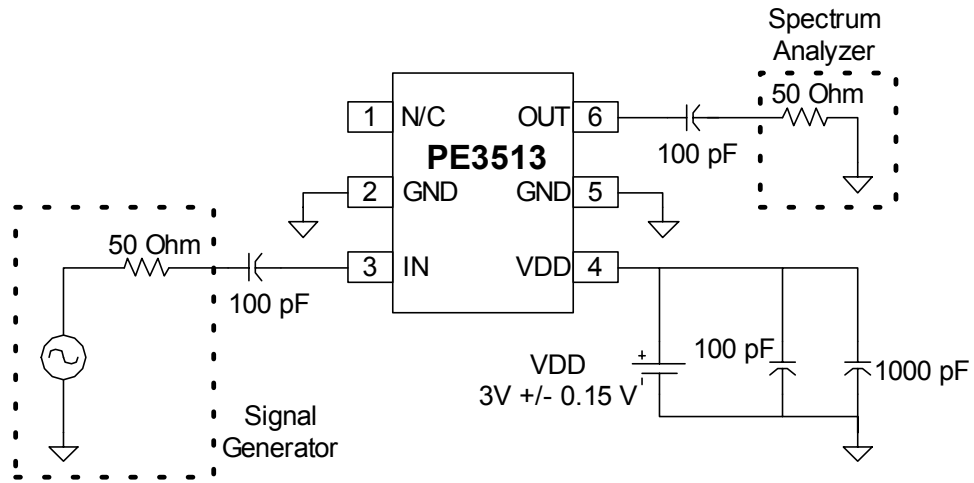
**Table 5. Pin Descriptions**

Pin No.	Pin Name	Description
1	N/C	No Connect. This pin should be left open.
2	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
3	IN	Input signal pin. DC blocking capacitor required (100 pF typical).
4	VDD	Power supply pin. Bypassing is required.
5	GND	Ground pin.
6	OUT	Divided frequency output pin. DC blocking capacitor required (100 pF typical).

**Table 6. Absolute Maximum Ratings**

Symbol	Parameter/Conditions	Min	Max	Units
VDD	Supply voltage		4.0	V
P <sub>in</sub>	Input Power		10	dBm
T <sub>ST</sub>	Storage temperature range	-65	150	°C
T <sub>OP</sub>	Operating temperature range	-40	85	°C
VESD	ESD voltage (Human Body Model)	250		V

**Figure 4. Test Circuit Block Diagram**



**Figure 5. AC Test Circuit**

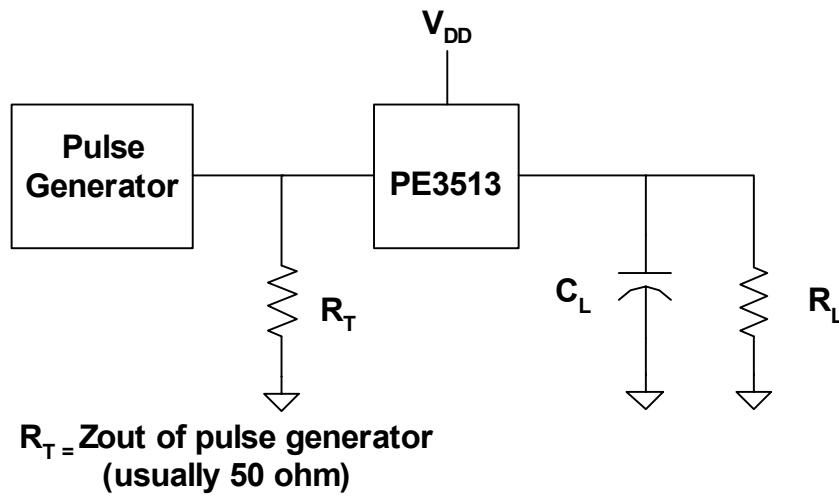


Figure 6. Evaluation Board Schematic Diagram

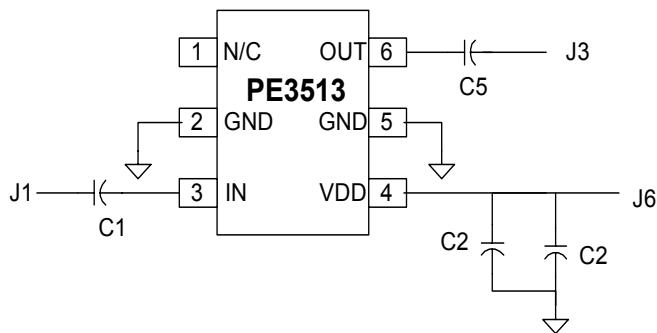
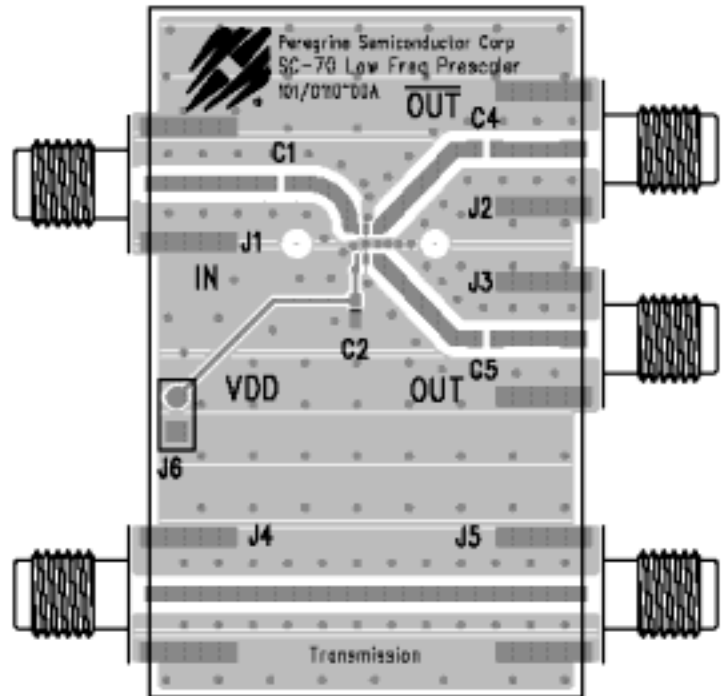


Figure 7. Evaluation Board Layout



### Evaluation Kit Operation

The SC-70 Prescaler Evaluation Board was designed to help customers evaluate the PE3513 divide-by-8 prescaler. On this board, the device input (pin 3) is connected to connector J1 through a 50  $\Omega$  transmission line. A series capacitor (C1) provides the necessary DC block for the device input. A value of 100 pF was used for this board layout; other applications may require a different value.

The device output (pin 6) is connected to connector J3 through a 50  $\Omega$  transmission line. A series capacitor (C5) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 100 pF was chosen for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were

designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014", and  $\epsilon_r$  of 4.4. Note that the predominate mode of these transmission lines is coplanar waveguide.

J6 provides DC power to the device via pin 4. Two decoupling capacitors (100 pF, 1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

### Applications Support

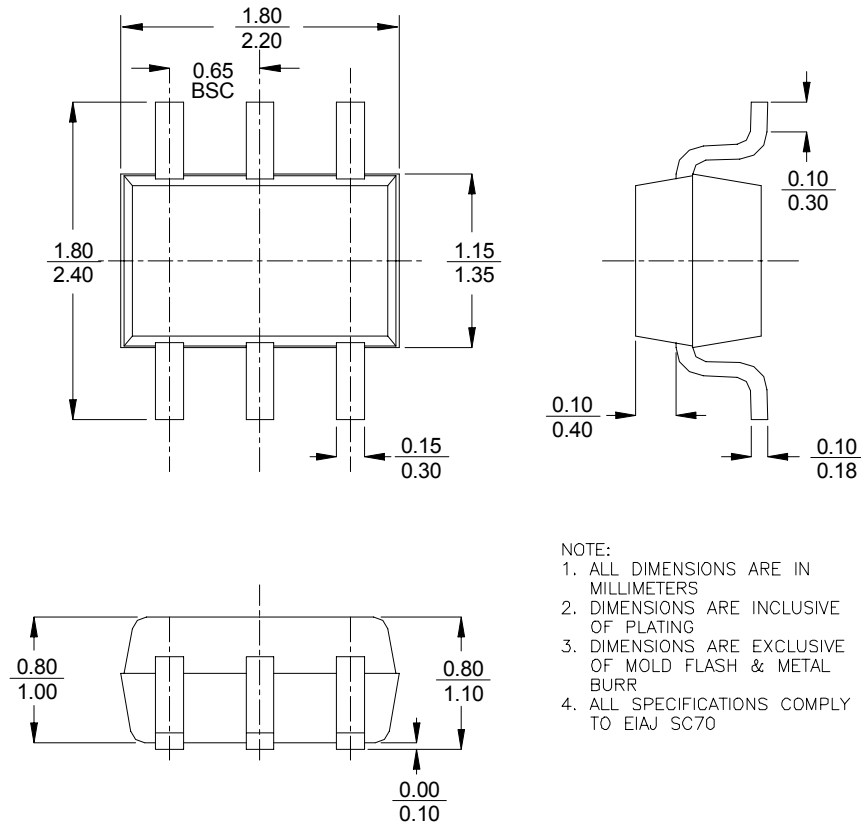
If you have a problem with your evaluation kit or if you have applications questions call (858) 455-0660 and ask for applications support. You may also contact us by fax or e-mail:

**Fax:** (858) 455-0770

**E-Mail:** [help@peregrine-semi.com](mailto:help@peregrine-semi.com)

**Figure 8. Package Drawing**

6-lead SC-70



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
  2. DIMENSIONS ARE INCLUSIVE OF PLATING
  3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
  4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70

**Table 7. Ordering Information**

Order Code	Part Marking	Description	Package	Shipping Method
3513-01	513	PE3513-06SC70-7680F	6-lead SC-70	7680 units / Canister
3513-02	513	PE3513-06SC70-3000C	6-lead SC-70	3000 units / T&R
3513-00	PE3513-EK	PE3513-06SC70-EK	Evaluation Kit	1 / Box

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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

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