CHERRY SEMICONDUCTOR

CS-212

SECURITY DETECTOR
DATA RECEIVER/TRANSMITTER

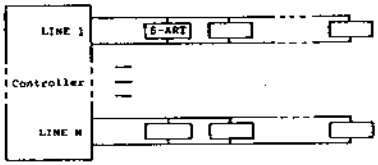
SERIAL-ADDRESSABLE RECEIVER/TRANSMITTER

INTRODUCTION

The S-ART is a 16 pin circuit designed for data transmission on a two-lead cable. The circuit is specially developed for alarm systems where it is desired to identify each detector individually. There can be up to 30 S-ART circuits/detectors on the same 2-lead cable. This cable transmits both DC supply to the S-ART and information to/from the S-ART.

SYSTEM BLOCK DIAGRAM

A method by which, in principle, the system can be extended to an infinite number of S-ART is shown on the block diagram. The controller scans the in/outputs of a number of lines, each with a maximum of 30 S-ARTs.



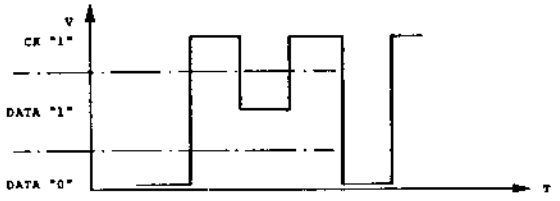
DESCRIPTION

The S-ART works on the principle by which an address is sent on the line cable and the S-ART which recognizes the address then carries out the order which can, in principle, be two things:

1. Transmit data from the line cable to the S-ART's two outputs OUT 0 and OUT 1.
2. Answer the S-ART controller with the condition of the 2 inputs IN 0 and IN 1/IN 2-3.

The line signal is divided into 3 levels in order to give a time signal for synchronizing and a data signal containing addresses, orders etc.

Typical signal levels for the three levels would be 15V, 7.5V and 0V.



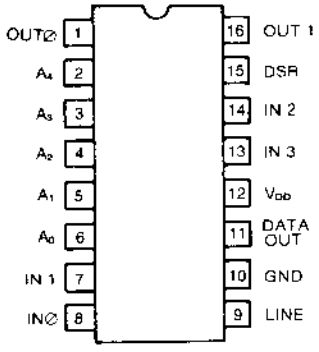
FEATURES:

- Receives/transmits data on only two leads
- Low current consumption
- High noise immunity
- Sabotage surveilled loop input

APPLICATIONS:

- Security systems
- Fire detection
- Surveillance
- Building automation
- Local data transmission

PIN CONNECTIONS



(Top View)

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SPECIFICATIONS

ADDRESS CODING

The circuit is coded on address inputs A0-A4.

In order to reduce the power consumption to the circuits they are in power down mode for most of the time. Only when a circuit is addressed is the amount to that particular circuit increased.

READ

When a S-ART has recognized an address with the correct parity and then received a READ-order the controller becomes passive. The S-ART in question will then send data bits to the controller. These bits are the condition on the IN 0 and IN 1/IN 2-3 and a parity bit derived from them.

The current in inputs IN 0 and IN 1 only flows when the S-ART is addressed.

If the sabotage surveilled loop IN 2-3 is used IN 1 should be open. IN 2-3 is then read instead of IN 1.

The loop IN 2-3 is checked for both shorting and breaking.

WRITE

When a S-ART has recognized an address with correct parity and a write order, the S-ART in question transmits data to the utputs OUT 0 and OUT 1. This data transmission takes place after a check of the parity bit. It the parity bit is wrong, data transmission to OUT 0 and OUT 1 is blocked and new data transmission can only take place after a read order which resets the parity fault.

The DSR signal can be used to strobe OUT 0 and OUT 1 further on in the following logic.

CHARACTERISTICS	CONDITIONS	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	UNITS
Device Current I_{dd} Not Addressed	Outputs unloaded Line Voltage=0-15V V_{dd}=15V		.47	0.80	mA
Device Current I_{dd} Power-Up Mode (5 corr. addr. bits) C_p4-C_p5	IN0, IN1 are open IN2, IN3 are active V_{dd}=15V		3.55	5.50	mA
Device Current I_{dd} Addressed, Line Output Transistor Active	IN2, IN3 not active IN0, IN1 are open V_{dd}=15V		6.24	9.64	mA
Device Current I_{dd} Addressed (4 corr. addr. bits) Line Output Transistor Not Active	IN2, IN3 not active IN0, IN1 are open V_{dd}=15V		1.84	2.86	mA
Output Voltage Low Level Out 0, Out 1, DSR	Vdd=10-15V I_{sink}=1mA			1.2	V
Output sink Current Out 0, Out 1, DSR		1.0			mA
Output Voltage High Level Out 0, Out 1, DSR				14	V
Leakage Current Out 0, Out 1, DSR	V_{out}=14V			30	μA
Input Voltage Level Low	V_{dd}=10-15V			30%V_{dd}	V
A0-A4, IN0, IN1 High	V_{dd}=10-15V	70%V_{dd}			V
Input Current IN0, IN1=GND Power-Up Mode (4 corr. addr. bits)	V_{dd}=18V	150		850	μA
Input Current A0-A4, IN0, IN1 Not Addressed	V_{dd}=18V			20	μA
Positive Trigger Threshold V_p, C	Clock Comparator	11.0	11.7	12.4	V
Voltage V_{dd}=15V V_p, D	Data Comparator	4.6	5.7	6.6	V
Negative Trigger V_{nc}	V_{dd}=15V Clock Comparator	10.2	10.9	11.6	V
Threshold Voltage V_{nc}	V_{dd}=15V Data Comparator	3.4	4.3	5.2	V
Hysteresis Voltage Clock/Data Comp.	V_{dd}=15V	0.7	0.8		V
Saturation Voltage For Line Output Driver	V_{dd}=15V I_c=50 mA			1	V
Saturation Voltage For Line Output Driver	V_{dd}=15V I_c=10 mA			0.4	V
Leakage Current For the Line Output	V_{line}=0-18V V_{dd}=18V			±16	μA
Line Signal Freq.	V_{dd}=15V±1V	0		20	kHz
Rise/Fall-Time Line Signal		0.250		250	μS
Turn-On Time for Line Output Driver			1.0		μS
Turn-Off Time for Line Output Driver			1.0		μS
•Line Voltage VL		0		28	V
Loop Current IN2, IN3		0.1		0.5	mA
Alarm Condition IN2-IN3 Loop Open		1		5	kΩ
Alarm Condition IN2-IN3 Loop Shorted		5		30	kΩ
Temperature T_A	Operating	-40		85	°C
Range T_{stg}	Storage	-65		150	°C

•The circuit shall function in the correct way only between 0-18V. Data driver must not turn on when line voltage is above 18V.

SERIAL-ADDRESSABLE RECEIVER TRANSMITTER S-ART continued

DATA FORMAT

The signals are sent out on the line in words organized as shown in the figure.

The S-ART information consists of two parity bits - an address parity bit and a data parity bit. Both the address and data are checked for even parity. The address parity bit must always be generated by the controller. The data parity bit during the READ-mode is generated by the S-ART. During the WRITE-mode the data parity bit is generated by the controller.

A0-A4:
Address inputs. Must be connected to V_{DD} or GND according to the relevant address code.

LINE:
Signal lead in the line cable.

GND:
Zero lead in the line cable.

V_{DD}:
Supply voltage to the S-ART. The voltage is derived from the line signal.

IN 0:
Input to S-ART.

IN 1:
Input to S-ART.

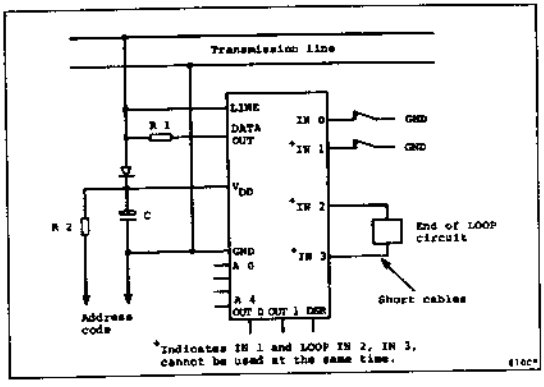
IN 2—IN 3:
Sabotage surveilled loop (shorting and breaking).

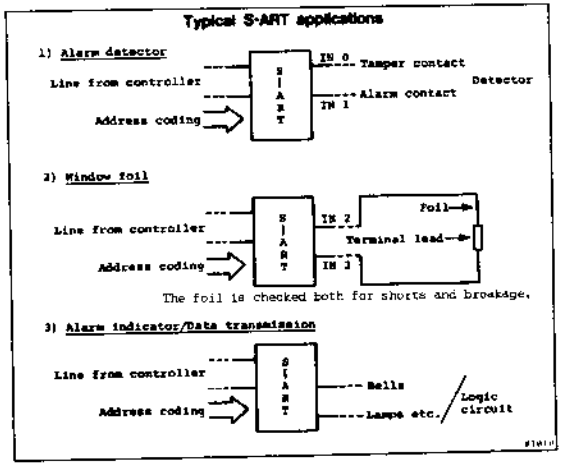
OUT 0:
Output (open collector) from S-ART.

OUT 1:
Output (open collector) from S-ART.

DSR:
Data set ready. Output (open collector) from the S-ART, which is active during WRITE-mode, when OUT 0 and OUT 1 change.

DATA OUT:
Output from the S-ART, which is active in the READ-mode. Transmits data from S-ART to line.





CS-212 FUNCTIONAL DESCRIPTION

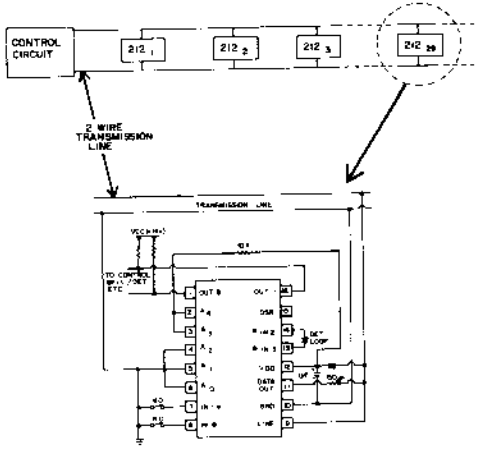
GENERAL

The CS-212 is a peripheral addressable circuit which is used as a communication link between Dectectors/Sensors and a Central Control Unit.

The communication between the CS-212 and a control unit takes place via a simple 2-wire cable which also provides power to the IC

On each 2-wire cable, a maximum of 30 CS-212's can be controlled or interrogated with the address binary 0-29. This permits surveillance of up to 30 window protections, door contacts, movement detectors, etc., within the same 2-wire group. Each 212 can monitor the status of two external surveillance devices and communicate the status back to the control unit. Two outputs are also available for controlling bells, lights, Led's, door locks, etc. These outputs are controlled from the control unit via the 2-wire cable.

The CS-212 is a 14,000 squaremill I^2L/Linear IC consisting of approximately 275 I^2L Gates, 100 BiPolar Transistors and 40 Resistors.



NOTES.
1 * indicates, IN 1 & loop IN 2, IN 3 cannot be used at the same time
2 This diagram shown CS-212 circuit coded to #24

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CS-212 FUNCTIONAL DESCRIPTION continued

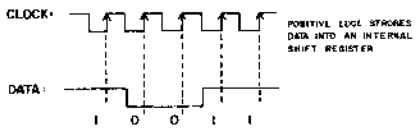
2-WIRE TRANSMISSION CABLE (The Line)

The 2-wire bidirectional transmission cable called "The Line" provides power and data to the CS-212 and also provides data back to the control circuit.

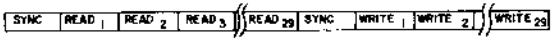
The line signal is rectified and filtered at each CS-212 and is used for the power supply to the chip. The CS-212 also decodes the line signal into clock and data signals used inside the IC.

A typical line signal from the control unit would look like the following:

The CS-212 would decode this into clock and data.

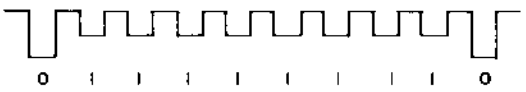


The CS-212 accepts addresses and commands in 10-bit word formats Three types of words must be generated: Sync. Read and Write.



SYNC WORD

Synchronization is obtained by providing the CS-212 with 8 or more 1's followed by a "0". To prevent a false sync, it is best to send 0 before the 8 1's. This word insures all circuits on the same line see the commands at the proper time

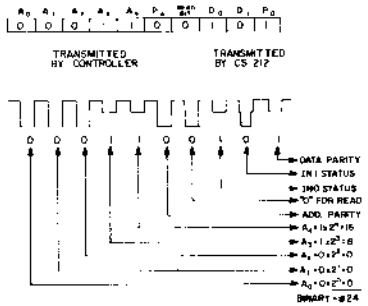


READ WORD

To check the status of a CS-212's inputs; i.e., IN0 and IN1 or IN2/IN3, a read word must be sent. The first 5 bits must correspond to the address of the CS-212 to be interrogated. Bit #6 is the address parity bit. It must insure that the first 6 bits are an even number of "1" 's. If the parity is even and the CS-212 to be interrogated has not previously received a parity error (odd parity), it will transmit its status, along with an internally generated parity bit. D_0 corresponds to IN_0, D1 corresponds to IN1 or IN2/IN3. After the address parity has been transmitted, the controller must allow the CS-212 to transmit. The controller must pull the line down to approximately 7.5V, then the CS-212 will transmit. If a "1" is to be transmitted, no change will occur on the line. If a "0" is to be transmitted, the CS-212 will then pull the line down. In either case, the controller must pull the line back up to 15V in order to continue. If the CS-212 has received a parity fault, it will transmit 3 one's (D0=D1=pD=1). This will allow the controller to detect a parity error. If a parity error is detected by the controller, the read word must be repeated.

TYPICAL READ WORD

Assume that Device #24 is to be interrogated and the status of IN0=1 and IN1=0.

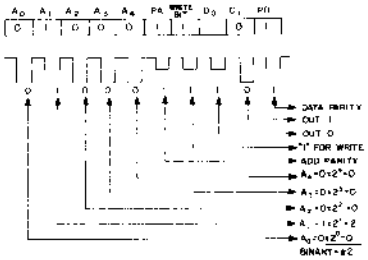


WRITE WORD

In order to update Out 0 and Out 1, a write word must be sent to the CS-212. The first 5 bits must correspond to the 212 you wish to update. Bit #6 is and address parity bit. It must insure even parity. D0 corresponds to Out 0 and D1 corresponds to Out 1. An even data parity bit must be received by the CS-212. If the address and data parity are even and the CS-212 has not previously received a parity error, it will update Out 0 and Out 1. If a parity error was received, the 212 will not be updated. In this case, a read word must be sent to clear the parity fault.

TYPICAL WRITE WORD

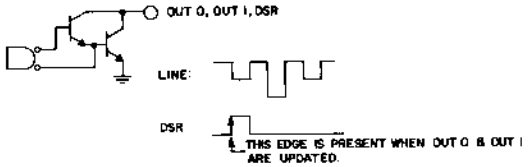
Assume CS-212 #2 is to be updated so that Out 0=1 and Out 1=0.



OUTPUTS

1. Out 0 and Out 1: Pin #'s 1, 16:
   These outputs are updated according to the information present during the write word.
2. DSR: Pin #15:
   The DSR pin is a monitor of the clock signal for the On Chip D type Flip Flops, corresponding to Out 0 and Out 1. It can be used to strobe data from Out 0 and Out 1 into external circuitry connected to the CS-212.

   These three outputs can sink up to 1mA at 1.2V. They are Darlington type open collector outputs.

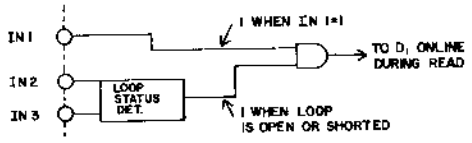


3. Data Out: Pin #11:
   The Data Out is used to transmit the status of In 0 and In 1 to the line. For Data=1, the line driver is off. For Data=0, the line driver is turned on. This output is a saturated switch capable of sinking 10mA DC at .4V and 50mA at 1V on a transients basis. The 50mA is needed to discharge the line capacitance. A 150 Resistor from the line to Pin 11 limits the current into Pin 11 when the line driver is on.

INPUTS

1. Address Inputs: Pin #'s 2, 3, 4, 5, 6.
   The 212 has 5 address inputs which decide what address code it will respond to. Their thresholds are approximately 1/2 V_{DD} and draw less than 20uA. The inputs should be grounded for Logic 0 and tied to V_{DD} (Pin 12) through a 10K Resistor. The resistor is necessary for non-destruction of the IC with 28V applied to the line.
2. Data Inputs: Pin #'s 7, 8.
   IN0 and IN1 (Pins 8 and 7) are digital inputs and are similar to the address inputs in that they have a threshold of approximately 1/2 V_{DD}. When the CS-212 is unaddressed, these inputs draw less than 20uA. When the circuit powers up, IN0 and IN1 source typically 400uA.
3. Detector Loop: Pin #'s 13, 14.
   IN2 and IN3 can be used together to form a detector loop. When used, the outputs are connected together through a window foil and a diode. These inputs will generate a 1 at D1 on the line when the pins are shorted or opened.

   When using IN2 and IN3, IN1 must be terminated to V_{DD} through the 10K Resistor used for the address inputs. When using IN1, IN2 and IN3 must be shorted or opened.



4. Line Input: Pin #9
   The line input is internally connected to two comparators. These comparators separate the line signal into clock and data. The line input will draw less than 16uA of input current.
5. V_{DD}: Pin #12
   The V_{DD} Pin provides power to the CS-212 circuitry. The line signal is externally rectified and filtered, then applied to V_{DD}. The V_{DD} pin draws varying amounts of current, depending upon the state of the 212. (See specification). The unaddressed current in less than .8mA.

   The operating voltage range is 10V to 18V on Pin 12 of the IC. This wide range is necessary because of losses in the line and ripple on V_{DD}.

   The circuit is designed to withstand 28V applied to the line. This is to prevent the destruction of the IC and its external components if the 2-wire cable is miswired.

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ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-212N	16 Lead PDIP

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Our Sales Representative in Your Area is: