FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27220-3E

ASSP For Power Supply Applications

6-ch DC/DC Converter IC With Synchronous Rectifier

MB3825A

■ DESCRIPTION

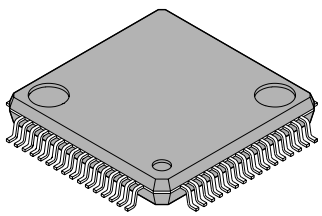
The MB3825A is a pulse width modulation (PWM) type 6-channel DC/DC converter IC with synchronous rectification (2-channels) designed for low voltage, high efficiency operation in high precision and high frequency applications, ideal for down conversion.
The MB3825A is an ideal device offering low power consumption, compact size and light weight for products such as self-contained camcorders and digital still cameras.

■ FEATURES

- Synchronous rectification (channels 1 and 4)
- High efficiency drive with power-on output enhanced by built-in speed-up circuit
- Wide range of operating power supply voltage : 2.5 V to 12 V
- Built-in high-precision reference voltage generator : 1.5 V ± 1%
- Wide operating oscillator frequency range, high frequency capability : 50 kHz to 800 kHz
- Wide input voltage range (all channels) : 0 V to Vcc – 0.9 V
- Error amplifier output for soft start (channels 1, 2, 4) (All channels may be set for same soft start time regardless of duty factor setting.)

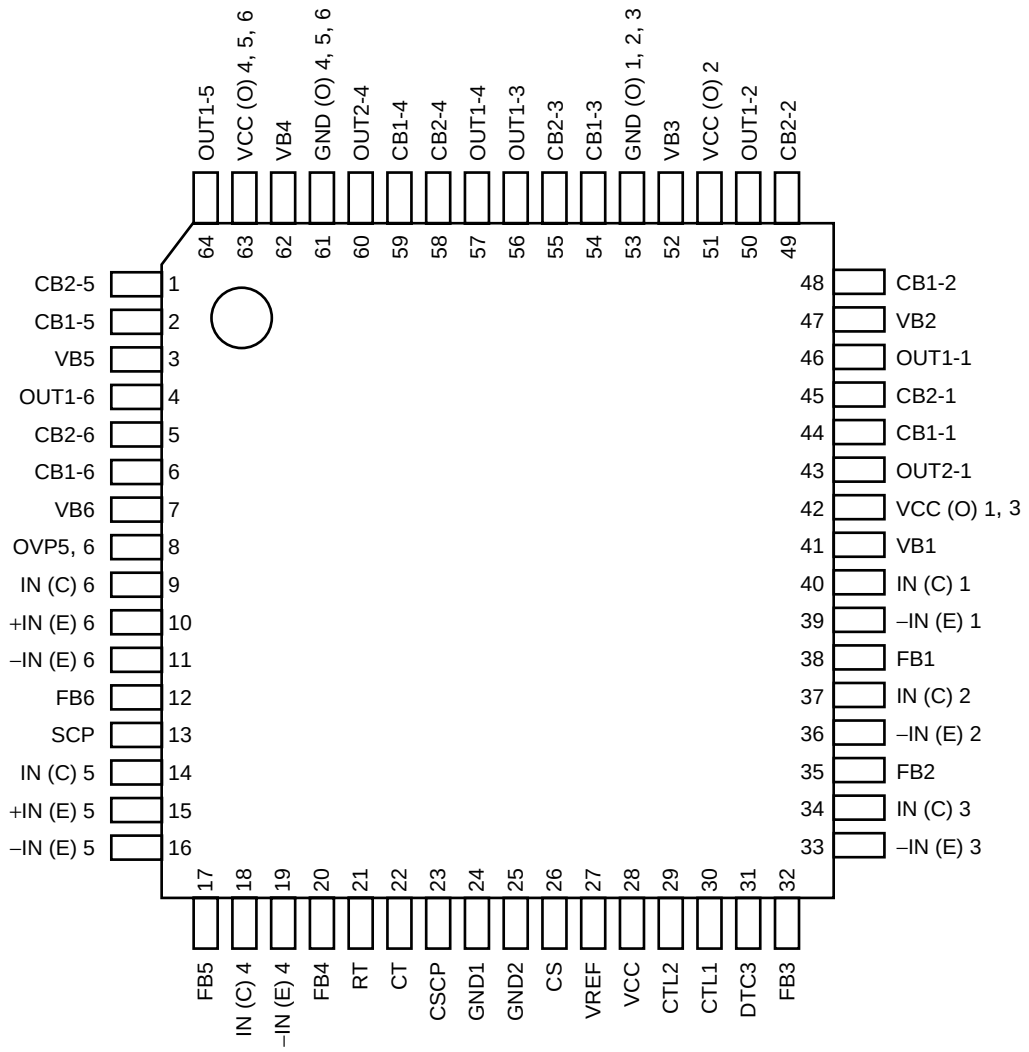
■ PACKAGE

64-pin, Plastic LQFP



(FPT-64P-M03)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.		Symbol	I/O	Descriptions
CH 1	38	FB1	O	Channel 1 error amplifier output terminal.
	39	–IN (E) 1	I	Channel 1 error amplifier inverted input terminal.
	40	IN (C) 1	I	Channel 1 short detection comparator input terminal.
	46	OUT1-1	O	Channel 1 main side output terminal.
	43	OUT2-1	O	Channel 1 synchronous rectifier side output terminal.
	44	CB1-1	—	Channel 1 boot capacitor connection terminal.
	45	CB2-1	—	
	41	VB1	—	Channel 1 output sink current setting terminal.
CH 2	35	FB2	O	Channel 2 error amplifier output terminal.
	36	–IN (E) 2	I	Channel 2 error amplifier inverted input terminal.
	37	IN (C) 2	I	Channel 2 short detection comparator input terminal.
	50	OUT1-2	O	Channel 2 output terminal.
	48	CB1-2	—	Channel 2 boot capacitor connection terminal.
	49	CB2-2	—	
	47	VB2	—	Channel 2 output sink current setting terminal.
CH 3	32	FB3	O	Channel 3 error amplifier output terminal.
	33	–IN (E) 3	I	Channel 3 error amplifier inverted input terminal.
	34	IN (C) 3	I	Channel 3 short detection comparator input terminal.
	56	OUT1-3	O	Channel 3 output terminal.
	54	CB1-3	—	Channel 3 boot capacitor connection terminal.
	55	CB2-3	—	
	52	VB3	—	Channel 3 output sink current setting terminal.
	31	DTC3	I	Channel 3 dead time control terminal.
CH 4	20	FB4	O	Channel 4 error amplifier output terminal.
	19	–IN (E) 4	I	Channel 4 error amplifier inverted input terminal.
	18	IN (C) 4	I	Channel 4 short detection comparator input terminal.
	57	OUT1-4	O	Channel 4 main side output terminal.
	60	OUT2-4	O	Channel 4 synchronous rectifier side output terminal.
	59	CB1-4	—	Channel 4 boot capacitor connection terminal.
	58	CB2-4	—	
	62	VB4	—	Channel 4 output sink current setting terminal.

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Pin No.		Symbol	I/O	Descriptions
CH 5	17	FB5	O	Channel 5 error amplifier output terminal.
	16	–IN (E) 5	I	Channel 5 error amplifier inverted input terminal.
	15	+IN (E) 5	I	Channel 5 error amplifier non-inverted input terminal.
	14	IN (C) 5	I	Channel 5 short detection comparator input terminal.
	64	OUT1-5	O	Channel 5 output terminal.
	2	CB1-5	—	Channel 5 boot capacitor connection terminal.
	1	CB2-5	—	
	3	VB5	—	Channel 5 output sink current setting terminal.
	8	OVP5, 6	I	Channel 5, 6 output maximum voltage setting terminal.
CH 6	12	FB6	O	Channel 6 error amplifier output terminal.
	11	–IN (E) 6	I	Channel 6 error amplifier inverted input terminal.
	10	+IN (E) 6	I	Channel 6 error amplifier non-inverted input terminal.
	9	IN (C) 6	I	Channel 6 short detection comparator input terminal.
	4	OUT1-6	O	Channel 6 output terminal.
	6	CB1-6	—	Channel 6 boot capacitor connection terminal.
	5	CB2-6	—	
	7	VB6	—	Channel 6 output sink current setting terminal.
	8	OVP5, 6	I	Channel 5, 6 output maximum voltage setting terminal.
Triangular-Wave Oscillator Circuit	21	RT	—	Triangular wave frequency setting resistor connection terminal.
	22	CT	—	Triangular wave frequency setting capacitor connection terminal.
Control Circuit	30	CTL1	I	Power supply control circuit. “H” level : Power supply operating mode “L” level : Standby mode
	29	CTL2	I	Channel 3 control circuit. When CTL1 terminal is “H” level “H” level : Channel 3 in operating mode “L” level : Channel 3 in OFF mode
	13	SCP	I	Short detection comparator input terminal.
	23	CSCP	—	Short protection circuit capacitor connection terminal.
	26	CS	—	Soft start circuit capacitor connection terminal.

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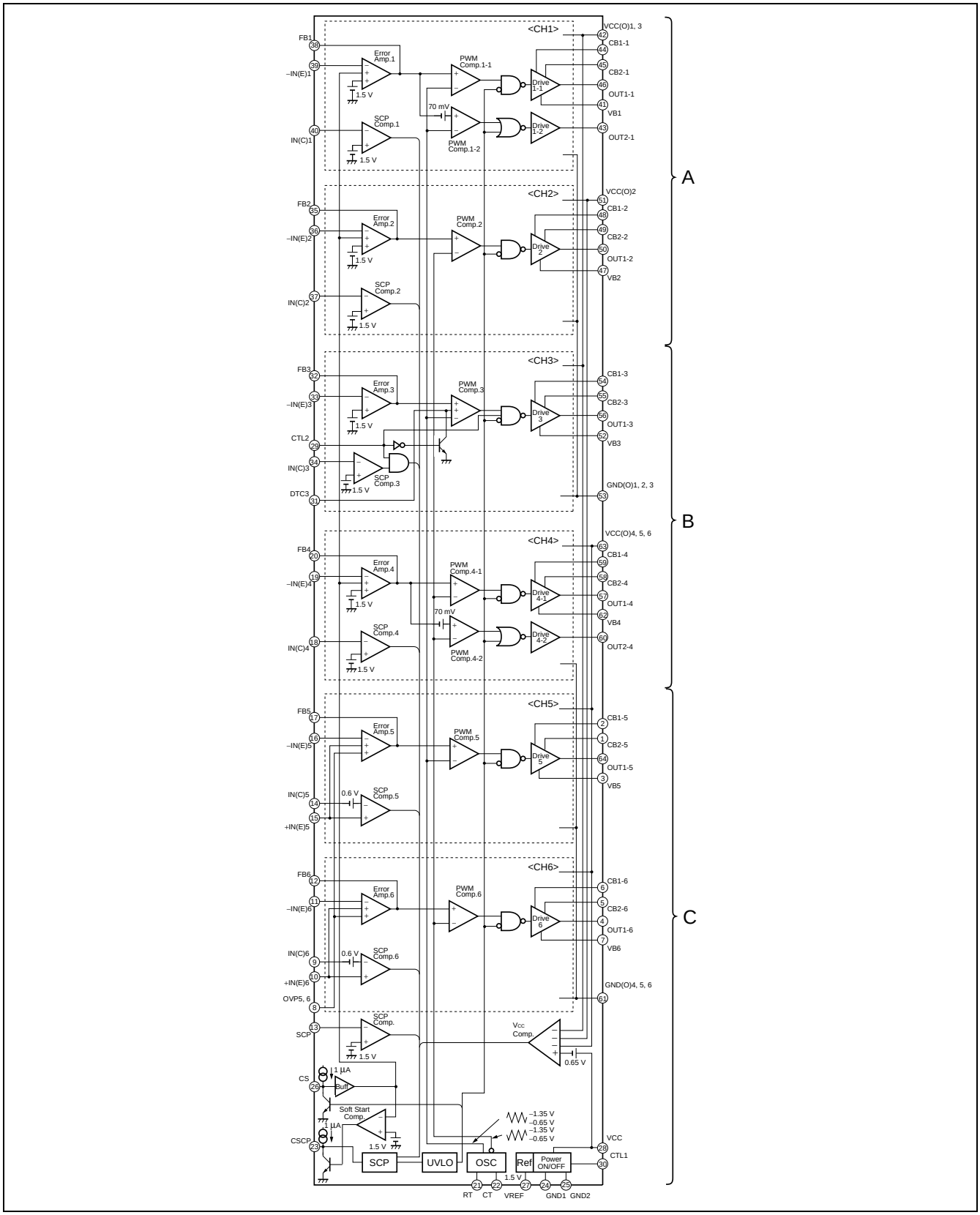
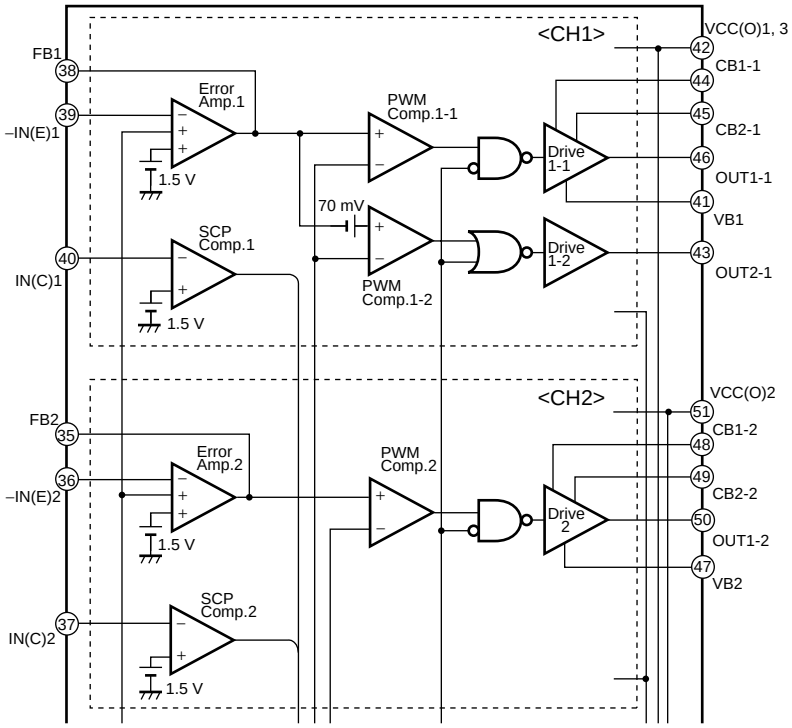
Pin No.		Symbol	I/O	Descriptions
Power Supply Circuit	28	VCC	—	Reference voltage and control circuit power supply terminal.
	42	VCC (O) 1, 3	—	Output circuit power supply terminal (Channel 1, 3) .
	51	VCC (O) 2	—	Output circuit power supply terminal (Channel 2) .
	63	VCC (O) 4, 5, 6	—	Output circuit power supply terminal (Channel 4, 5, 6) .
	27	VREF	O	Reference voltage output terminal.
	24	GND1	—	Ground terminal.
	25	GND2	—	Ground terminal.
	53	GND (O) 1, 2, 3	—	Output circuit ground terminal (Channel 1, 2, 3) .
	61	GND (O) 4, 5, 6	—	Output circuit ground terminal (Channel 4, 5, 6) .

■ BLOCK DIAGRAM

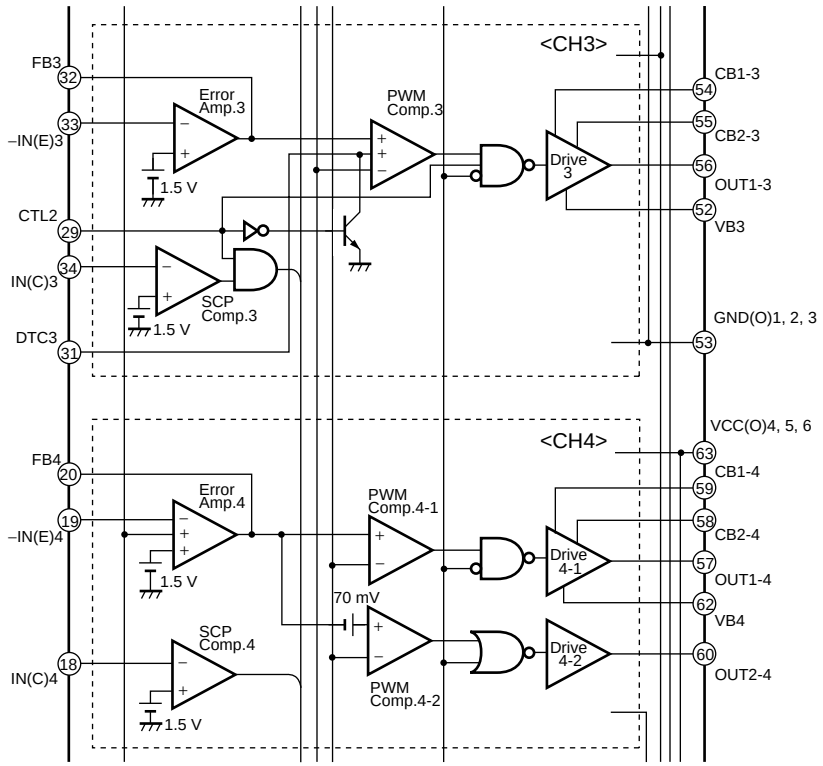
- **General view**



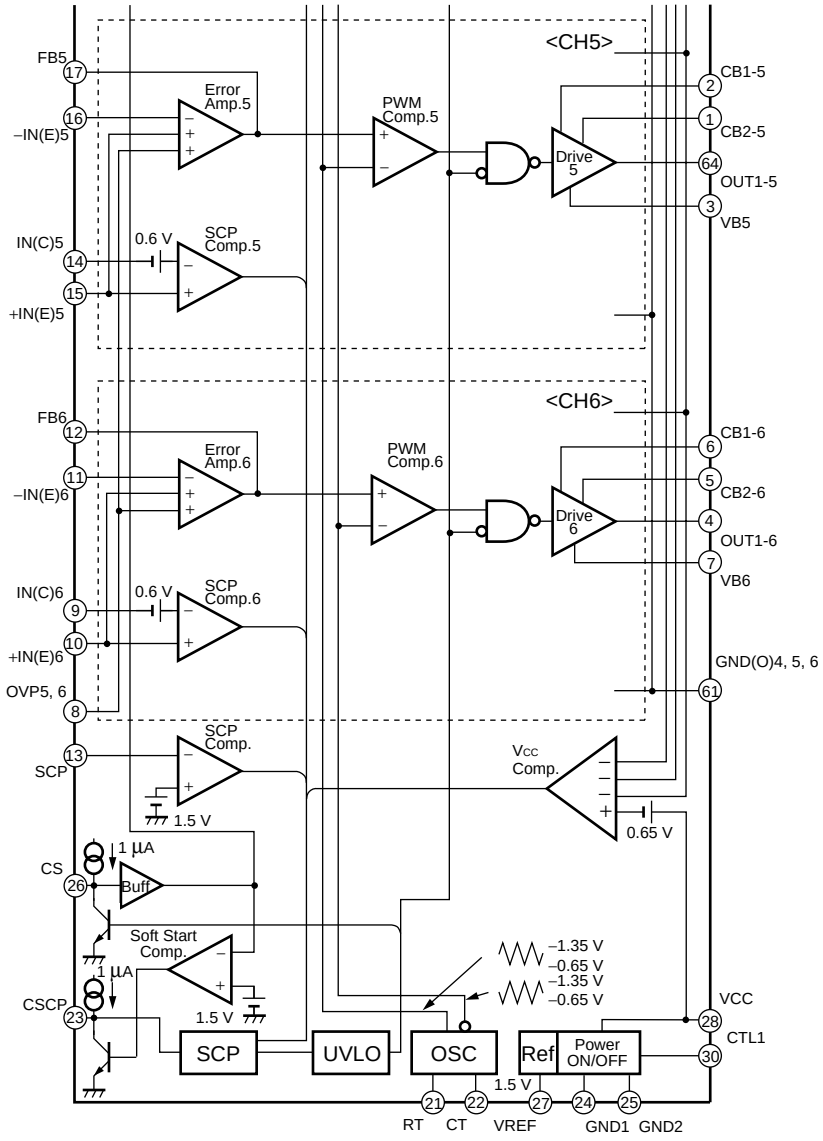
- **Enlarged view of A**



- **Enlarged view of B**



- **Enlarged view of C**



■ ABSOLUTE MAXIMUM RAGINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	—	—	17	V
Output current	Io	OUT terminal	—	50	mA
Output peak current	Io	OUT terminal, Duty ≤ 5%	—	200	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	800*	mW
Storage temperature	T_{stg}	—	–55	+125	°C

* : The packages are mounted on the epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{CC}	—	2.5	6.0	12	V
Reference voltage output current	I_{OR}	—	–1	—	0	mA
Input voltage	V_{IN}	–IN (E) , IN (C) , OVP terminal	0	—	V_{CC} – 0.9	V
Control input voltage	V_{CTL}	CTL terminal	0	—	12	V
Output current	I_O	Main side OUT terminal	2	—	20	mA
Output current setting resistor	R_B	—	2.7	5.6	30	kΩ
Oscillator frequency	f_{OSC}	—	50	500	800	kHz
Timing capacitor	C_T	—	50	100	1500	pF
Timing resistor	R_T	—	20	39	82	kΩ
Soft-start capacitor	C_S	—	—	0.1	1.0	µF
Short detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CC} (O) = +6 V, Ta = +25°C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Reference voltage block	Reference voltage	V_{REF}	27	—	1.485	1.500	1.515	V
	Output voltage temperature stability	ΔV_{REF} /V_{REF}	27	Ta = –30 °C to +85 °C	—	0.5*	—	%
	Input stability	Line	27	V_{CC} = 2.5 V to 12 V	—	2	10	mV
	Load stability	Load	27	VREF = 0 mA to –1 mA	—	2	10	mV
	Short-circuit output current	I_{OS}	27	VREF = 2 V	–10	–6	–1	mA
Under voltage lockout protection circuit block (U.V.L.O)	Threshold voltage	V_{TH}	46	V_{CC} = ↓	—	2.1	—	V
	Hysteresis width	V_H	46	—	—	0.1	—	V
	Reset voltage	V_{RST}	46	—	1.8	2.0	—	V
Soft-start block	Input standby voltage	V_{STB}	26	—	—	50	100	mV
	Charge current	I_{CS}	26	—	–1.4	–1.0	–0.6	µA
Short circuit detection block	Threshold voltage	V_{TH}	23	—	0.65	0.70	0.75	V
	Input standby voltage	V_{STB}	23	—	—	50	100	mV
	Input latch voltage	V_I	23	—	—	50	100	mV
	Input source current	I_{CSCP}	23	—	–1.4	–1.0	–0.6	µA
Triangular wave oscillator block	Oscillator frequency	f_{OSC}	46, 50, 56, 57, 64, 4	C_T = 100 pF, R_T = 39 kΩ	450	500	550	kHz
	Frequency stability for voltage	$\Delta f/fdv$	46, 50, 56, 57, 64, 4	V_{CC} = 2.5 V to 12 V	—	1	10	%
	Frequency stability for temperature	$\Delta f/fdt$	46, 50, 56, 57, 64, 4	Ta = –30 °C to +85 °C	—	1*	—	%

* : Standard design value.

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(V_{CC} = V_{CC} (O) = +6 V, Ta = +25°C)

Parameter		Symbol	Pin No	Conditions	Value			Unit
					Min.	Typ.	Max.	
Error amplifier block (CH1 to CH4)	Threshold voltage	V_{TH}	38, 35, 32, 20	FB = 1.0 V	1.45	1.50	1.55	V
	V_T temperature stability	$\Delta V_T/V_T$	38, 35, 32, 20	Ta = –30 °C to +85 °C	—	0.5*	—	%
	Input bias current	I_B	39, 36, 33, 19	–IN = 0 V	–200	–20	—	nA
	Voltage gain	A_V	38, 35, 32, 20	DC	60	75	—	dB
	Frequency bandwidth	BW	38, 35, 32, 20	A_V = 0 dB	—	1.0*	—	MHz
	Maximum output voltage width	V_{OM}^+	38, 35, 32, 20	—	1.45	1.55	—	V
		V_{OM}^-	38, 35, 32, 20	—	—	20	200	mV
	Output source current	I_O^-	38, 35, 32, 20	FB = 1.0 V	—	–2.0	–0.6	mA
	Output sink current	I_O^+	38, 20	FB = 1.0 V (CH1, CH4)	60	120	—	µA
			35, 32	FB = 1.0 V (CH2, CH3)	60	130	—	µA
Error amplifier bolck (CH5, CH6)	Input offset voltage	V_{IO}	17, 12	FB = 1.0 V	–1	9	19	mV
	Input bias current	I_B	15, 10	+IN = 0 V, +IN (E) terminal	–400	–40	—	nA
			16, 11	–IN = 0 V, –IN (E) terminal	–200	–20	—	nA
			8	OVP = 0 V, OVP terminal	–400	–40	—	nA
	Common mode input voltage range	V_{CM}	17, 12	—	0	—	V_{CC} – 0.9	V
	Voltage gain	A_V	17, 12	DC	60	75	—	dB
	Frequency bandwidth	BW	17, 12	A_V = 0 dB	—	1.0*	—	MHz
	Maximum output voltage width	V_{OM}^+	17, 12	—	1.45	1.55	—	V
		V_{OM}^-	17, 12	—	—	20	200	mV
	Output source current	I_O^-	17, 12	FB = 1.0 V	—	–2.0	–0.6	mA
	Output sink current	I_O^+	17, 12	FB = 1.0 V	60	130	—	µA
SCP Comp. block (CH1 to CH4, SCP)	Threshold voltage	V_{TH}	46, 50, 56, 57	—	1.45	1.50	1.55	V
	Input bias current	I_B	40, 37, 34, 18, 13	IN (C) = SCP = 0 V	–200	–20	—	nA

* : Standard design value.

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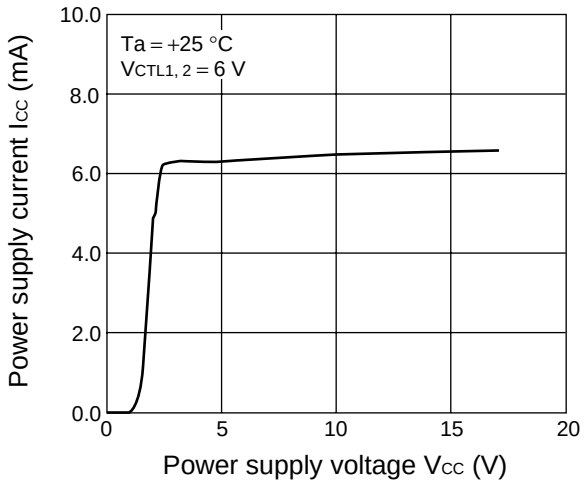
(V_{CC} = V_{CC} (O) = +6 V, Ta = +25°C)

Parameter		Symbol	Pin No	Conditions	Value			Unit
					Min.	Typ.	Max.	
SCP Comp. block (CH5, CH6)	Input offset voltage	V_{IO}	64, 4	—	0.55	0.60	0.65	V
	Input bias current	I_{IN^+}	14, 9	IN (C) = 0 V	–400	–40	—	nA
	Common mode input voltage range	V_{CM}	64, 4	—	0	—	V_{CC} – 0.9	V
PWM Comp. block (CH1 to CH6)	Threshold voltage	V_{T0}	46, 50, 56, 57, 64, 4	Duty cycle = 0%	0.55	0.65	—	V
		V_{T100}	46, 50, 56, 57, 64, 4	Duty cycle = 100%	—	1.35	1.45	V
Dead time control block (CH3) (DTC terminal)	Input bias current	I_B	31	DTC = 0.4 V	–1.0	–0.2	—	µA
	Sink current at CTL2 = "L"	I_{IDTC}	31	DTC = 1.5 V CTL2 = 0 V	80	500	—	µA
	Input voltage at CTL2 = "L"	V_{IDTC}	31	IDTC = 40 µA CTL2 = 0 V	—	0.2	0.3	V
Main side output block (CH1 to CH6) (Drive-1)	Output source current	I_{O^-}	46, 50, 56, 57, 64, 4	Duty cycle ≤ 5%	—	–100	—	mA
	Output sink current	I_{O^+}	46, 50, 56, 57, 64, 4	R_B = 5.6 kΩ	7	10	13	mA
Synchro-nous rectifier side output block (CH1, CH4) (Drive-2)	Output source current	I_{O^-}	43, 60	Duty cycle ≤ 5%, V_O = 2 V	—	–70	—	mA
	Output sink current	I_{O^+}	43, 60	Duty cycle ≤ 5%, V_O = 1 V	—	70	—	mA
	Output voltage	V_{OH}	43, 60	—	3.5	4.0	—	V
		V_{OL}	43, 60	—	—	0	0.1	V
Control block	CTL input condition	V_{ON}	27	IC active mode	2.1	—	12	V
		V_{OFF}	27	IC standby mode	0	—	0.7	V
	Input current	I_{CTL}	30	CTL = 5 V	—	100	200	µA
V_{CC} Comp. block	Threshold voltage	V_{TH}	46, 50, 56	—	V_{CC} – 0.70	V_{CC} – 0.65	V_{CC} – 0.60	V
General	Standby current	I_{CCS}	28	VCC terminal, CTL = 0 V	—	—	10	µA
		$I_{CCS\ (O)}$	42, 51, 63	VCC (O) terminal, CTL = 0 V	—	—	10	µA
	Power supply current	I_{CC}	28, 42, 51, 63	—	—	6.3	9.0	mA

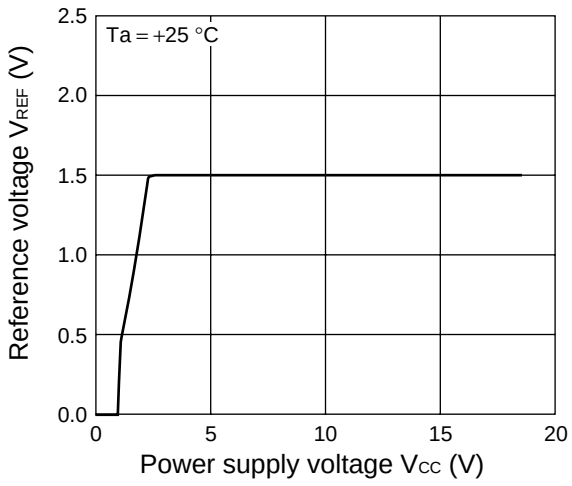
* : Standard design value.

■ TYPICAL CHARACTERISTICS

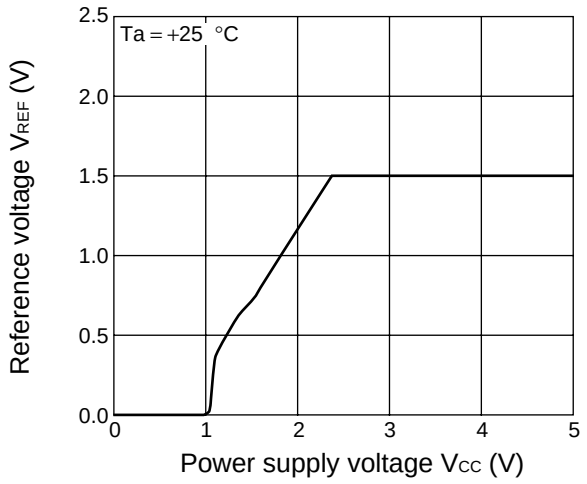
Power supply current vs. power supply voltage



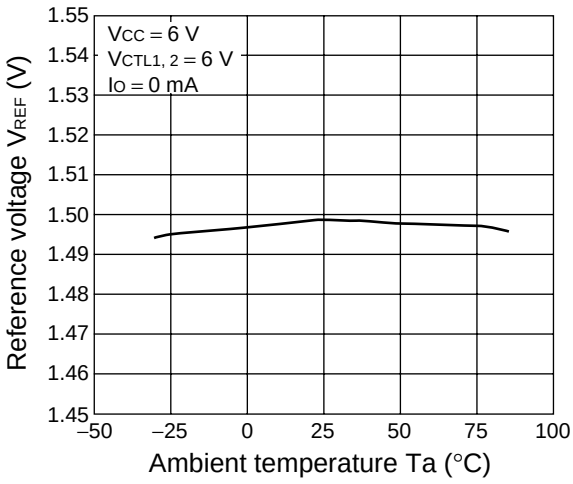
Reference voltage vs. power supply voltage



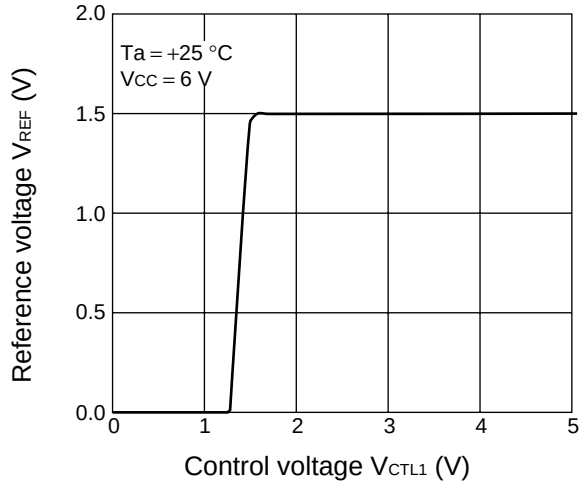
Reference voltage vs. power supply voltage



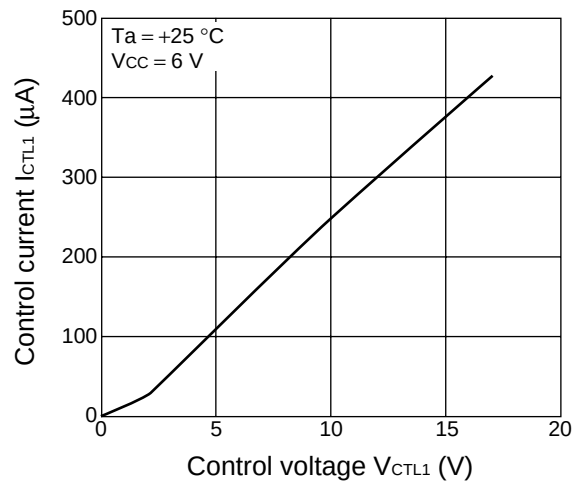
Reference voltage vs. ambient temperature



Reference voltage vs. control voltage



Control current vs. control voltage



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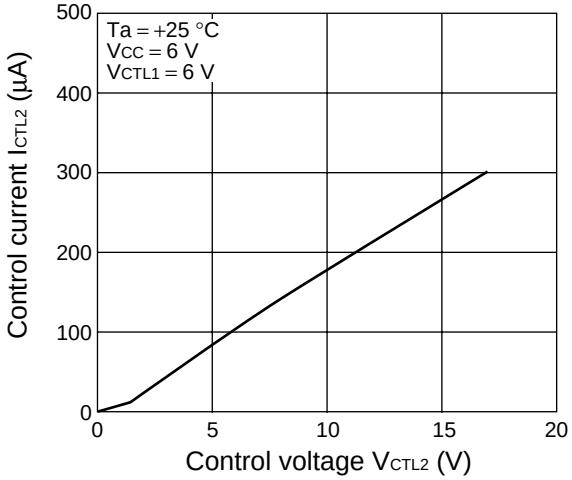
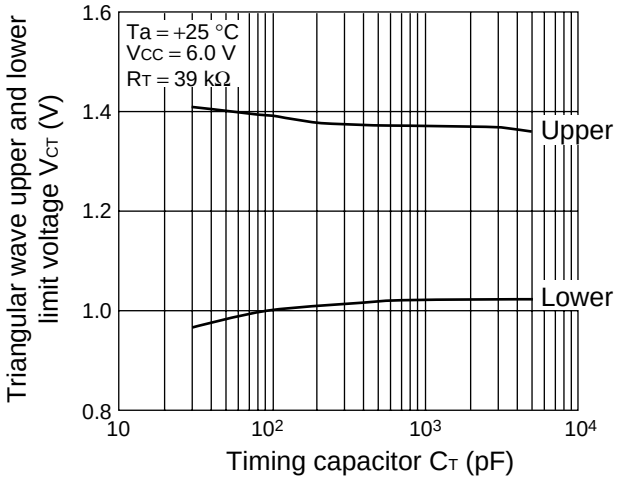
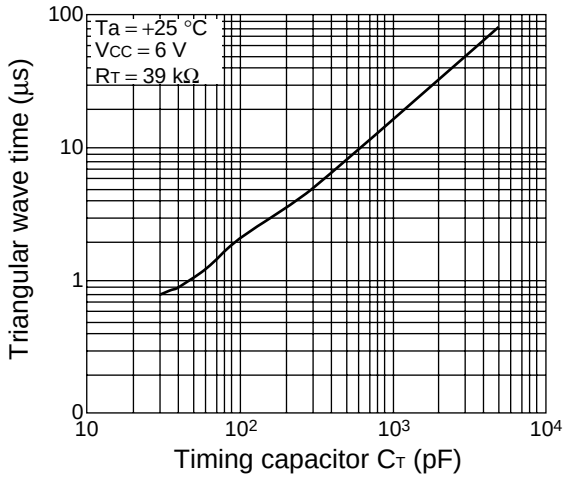
Control current vs. control voltage



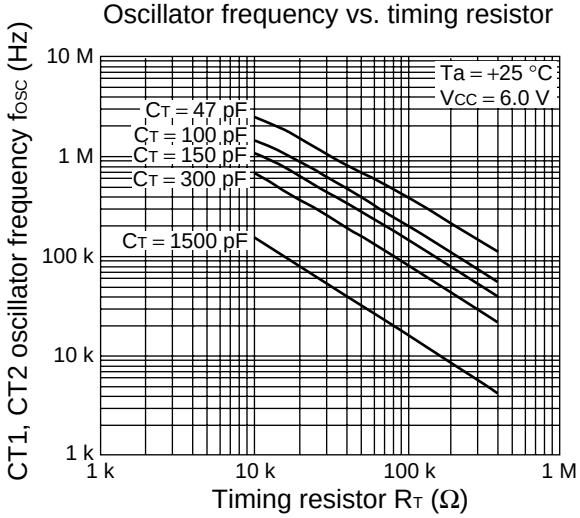
Triangular wave upper and lower limit voltage vs. timing capacitor



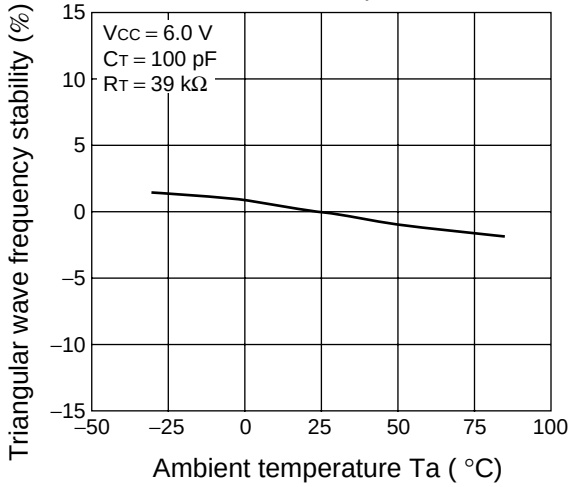
Triangular wave time vs. timing capacitor



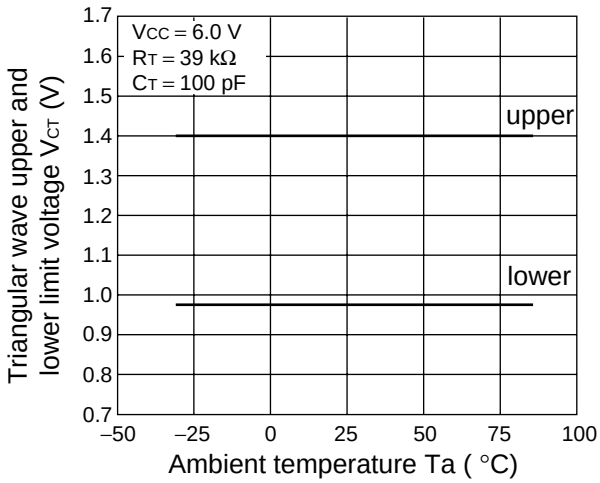
Oscillator frequency vs. timing resistor



Triangular wave frequency stability vs. ambient temperature



Triangular wave upper and lower limit voltage vs. ambient temperature



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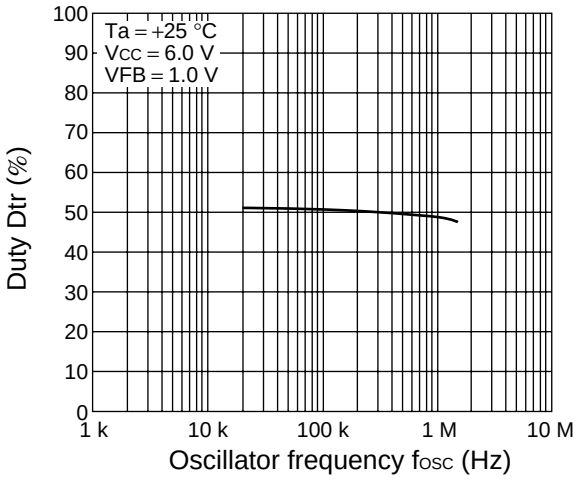
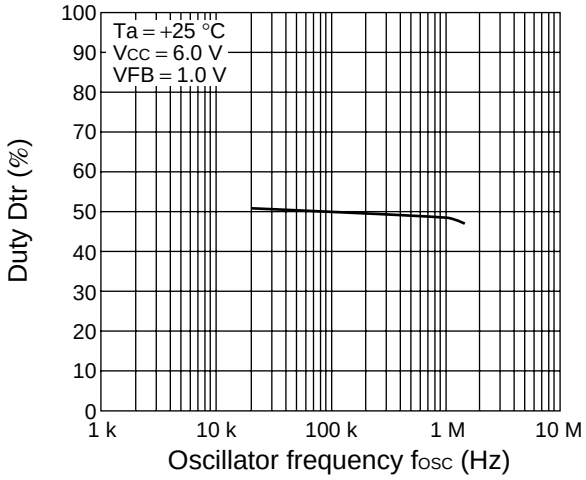
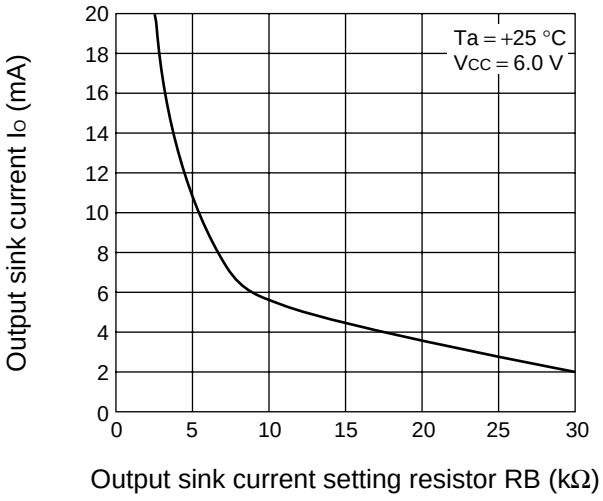
Duty vs. oscillator frequency (ch1)



Duty vs. oscillator frequency (ch4)



Output sink current vs.
output sink current setting resistor



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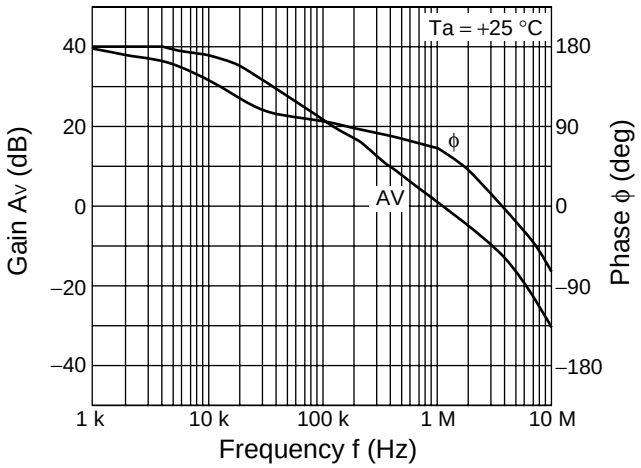
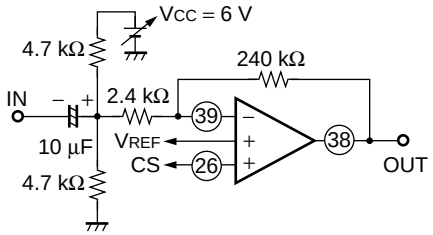
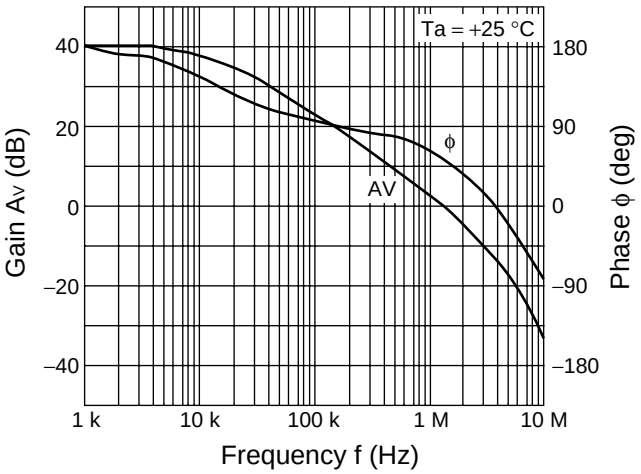
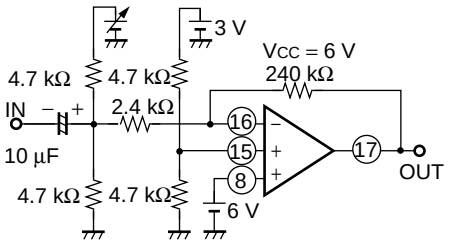
Error amplifier gain and phase vs. frequency (ch1)



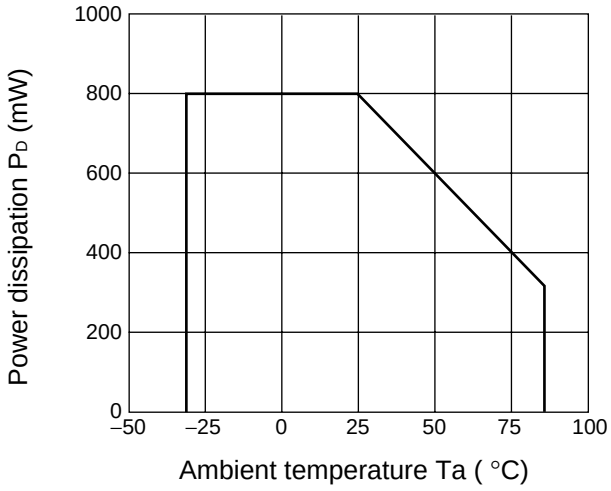


Error amplifier gain and phase vs. frequency (ch5)





Power dissipation vs. ambient temperature



■ FUNCTIONAL DESCRIPTION

1. Switching Regulator Function

(1) Reference voltage circuit

The reference voltage circuit generates a temperature-compensated reference voltage (≒1.500 V) using the voltage supplied from the power supply terminal (pin 28) . This voltage is used as the reference voltage for the internal circuits of the IC. The reference voltage of up to 1 mA can also be supplied to an external device from the VREF terminal (pin 27) .

(2) Triangular-wave oscillator circuit

By connecting a timing capacitor and a resistor to the C_T (pin 22) and the R_T (pin 21) terminals, it is possible to generate any desired triangular oscillator waveform (CT : amplitude 1.0 V to 1.4 V, CT1 : amplitude 0.65 V to 1.35 V in phase with CT1, and CT2 : amplitude 0.65 V to 1.35 V in inverse phase with CT) . The triangular wave is input to CT1, CT2 and the PWM comparator within the IC.

(3) Error amplifier

This amplifier detects the output voltage of the switching regulator and outputs a PWM control signal accordingly. It has a wide common-mode input voltage range from 0 V to V_{CC} – 0.9 V on channels 5 and 6 allows easy setting from an external power supply, making the system suitable for DC motor speed control.
By connecting a feedback resistor and capacitor from the error amplifier output terminal to the inverted input terminal, you can form any desired loop gain, for stable phase compensation.

(4) PWM comparator

The PWM comparators in these channels are a voltage comparator with one inverted input and one non-inverted input (channels 1, 2, 4, 5, 6) as well as one inverted input and two non-inverted inputs (channel 3) , and voltage pulse width modifier to control output duty according to input voltage.
In the interval when the error amplifier output voltage is higher than the triangular waveform, the output transistor is turned on (channels 1, 2, 4, 5, 6) .
In the interval when the error amplifier output voltage is lower than the triangular waveform, the output transistor is turned on (channel 1, 4 synchronous rectifier side) .
In the interval when the error amplifier output voltage and DTC3 voltage are higher than the triangular waveform, the output transistor is switched on (channel 3) .

(5) Output circuit

The output circuits is comprised of a totem-pole configuration on both the main side and synchronous rectifier side, and can drive an external PNP transistor (main side) or N-ch MOSFET (synchronous rectifier side) .
Sink current (on the main side) can be set up to 20 mA depending on the resistance of the VB terminal.

2. Channel Control Function

Channel on and off levels are dependent on the voltage levels of the CTL1 terminal (pin 30) and CTL 2 terminal (pin 29) .

Table 1 Channel by Channel On/Off Setting Conditions.

CTL terminal voltage level		On/Off state of channel						
CTL1	CTL2	Power supply circuit	Channel 1	Channel 2	Channel 4	Channel 5	Channel 6	Channel 3
L	X	OFF (standby mode) *						
H	L	ON						OFF
	H							ON

* : The power supply current in standby mode is 10 μA or less.

3. Protective Functions

(1) Timer-latch short-circuit protection circuit

The short detection comparator in each channel detects the output voltage level, and when any channel output voltage falls below the short detection voltage, or the SCP terminal (pin 13) voltage falls below the reference voltage, the timer circuit starts operating and the capacitor C_{SCP} connected to the CSCP terminal (pin 23) starts charging.

When the capacitor charge reaches approximately 0.7 V, the output transistor is turned off and the idle interval becomes 100%.

When actuated, this protection circuit can be reset by turning on the power supply again. (See “METHOD OF SETTING TIME CONSTANT FOR TIMER-LATCH SHORT PROTECTION CIRCUIT”.)

(2) Under voltage lockout protection circuit

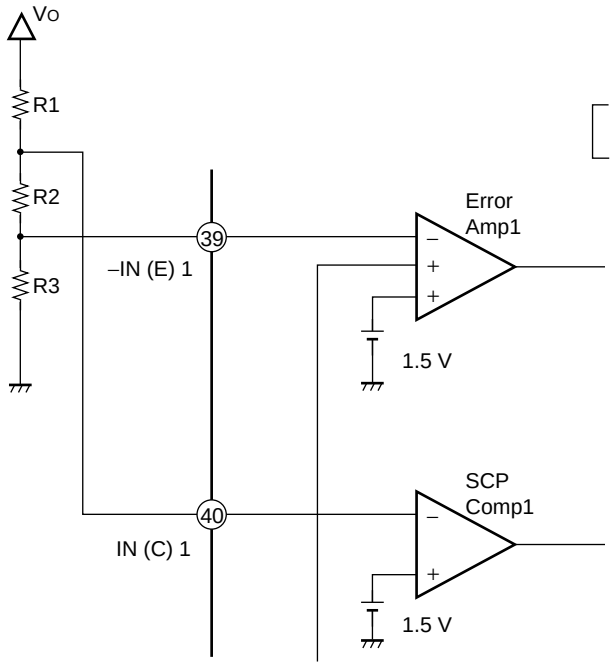
A transient state at power-on or a momentary drop of the power supply voltage causes the control IC to malfunction, resulting in system breakdown or system deterioration. By detecting the internal reference voltage with respect to the power supply voltage, this protection circuit resets the latch circuit to turn off the output transistor and set the duty (OFF) = 100%, while at the same time holding the CSCP terminal (pin 23) at the “L”. The reset is cleared when the power supply voltage becomes greater than or equal to the threshold voltage level of this protection circuit.

(3) Output Supply Monitor Comparator (Vcc Comp.)

The output supply monitor comparator compares the output circuit power supply (VCC (O) 1, 3, VCC (O) 2, VCC (O) 4, 5, 6) to the VCC level, and operates the timer-latch short protection circuit if any of the output circuit power supplies fall below Vcc – 0.65 V.

■ METHODS OF SETTING THE OUTPUT VOLTAGE

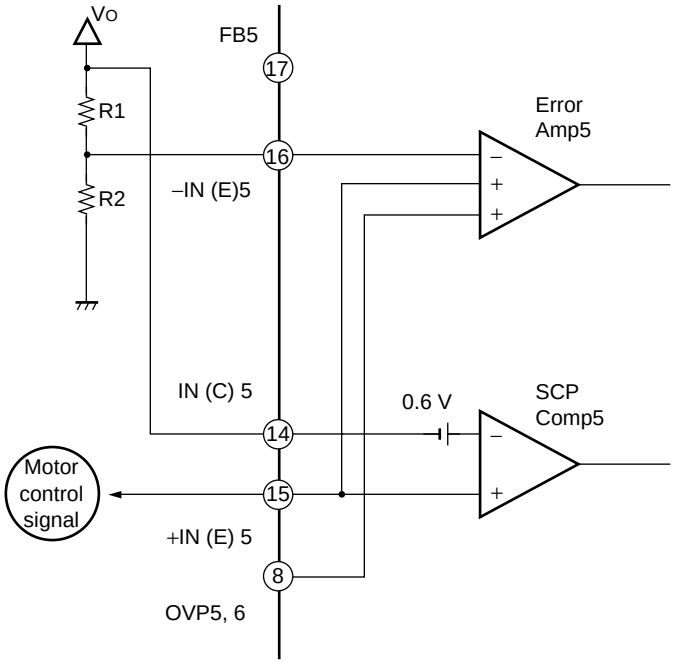
Figure 1. CH1 to CH4



$$V_O = \frac{1.5\ V}{R3}\ (R1 + R2 + R3)$$

$$\left[\ V_O > \frac{1.5\ V}{R2 + R3}\ (R1 + R2 + R3)\ \right]$$

Figure 2. CH5 and CH6



$$V_O = \frac{V_{+IN\ (E)\ 5}}{R2}\ (R1 + R2)$$

$$\left[\ V_{OVP5,\ 6} > V_{+IN\ (E)\ 5}\ \right]$$

$$V_O = \frac{V_{OVP5,\ 6}}{R2}\ (R1 + R2)$$

$$\left[\ V_{OVP5,\ 6} < V_{+IN\ (E)\ 5}\ \right]$$

■ METHOD OF SETTING THE OUTPUT CURRENT

Figure 3 shows the configuration of the output circuits, and Figure 4 illustrates how the sink current value of the output current waveform has a constant current setting. Note that the sink current is set by the following formula

- Sink current = $(V_B/R_B) \times 60 \div 56/R_B$ [A]

Figure 3. Output circuit (main side)

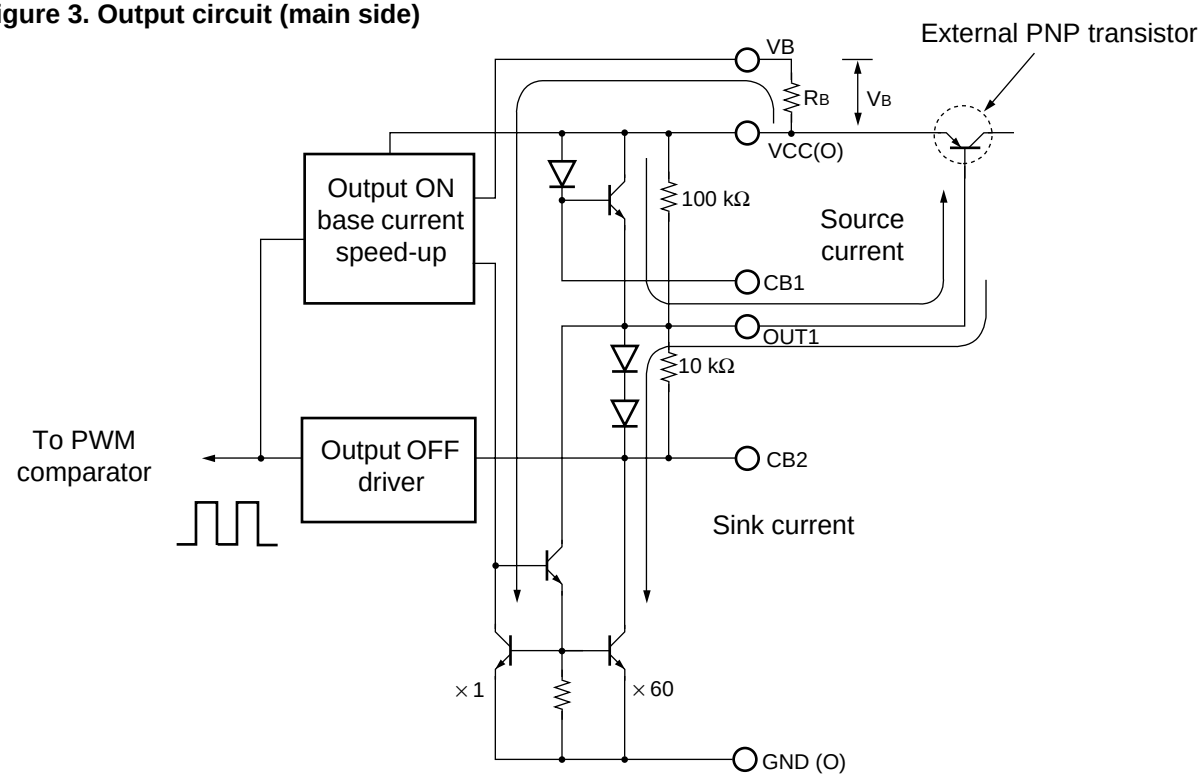
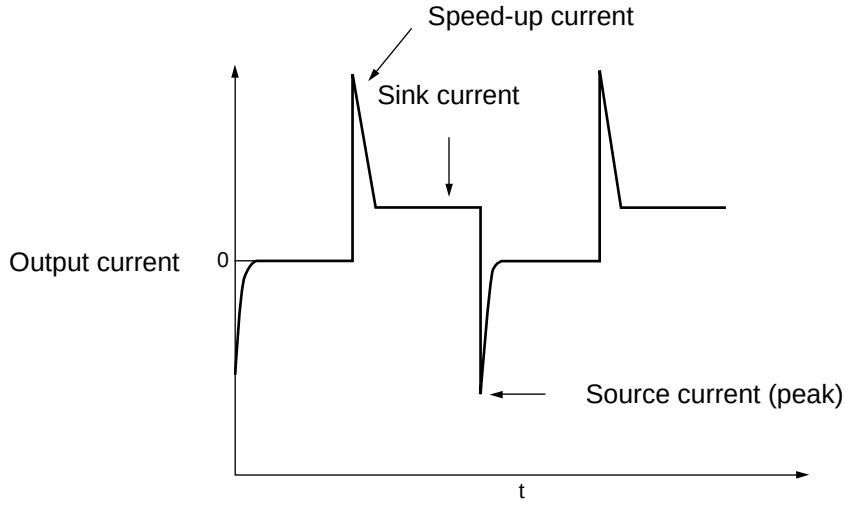


Figure 4. Output current waveform

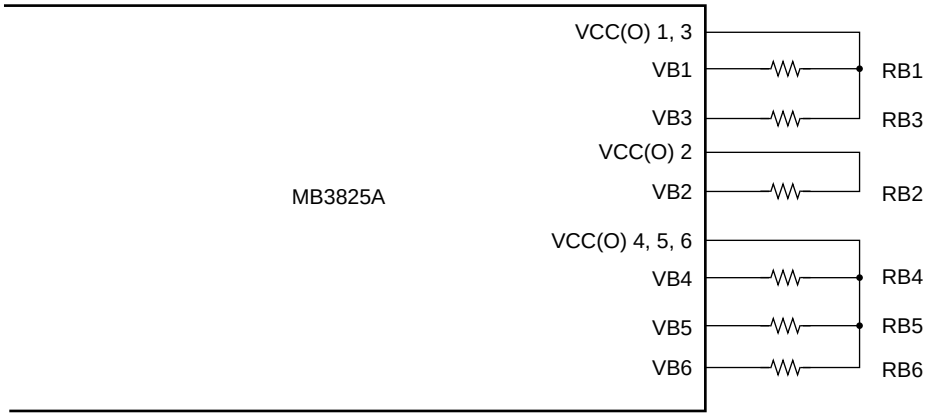


Note :

Output current setting resistance RB1 to RB6 should be connected to each channel as shown in Figure 5 below.

- For channel 1 and 3, connect the respective VB terminals to VCC (O) 1, 3 through the setting resistor RB.
- For channel 2, connect the VB2 terminal to VCC (O) 2 through setting resistor RB2.
- For channels 4 to 6, connect the respective VB terminals to VCC (O) 4, 5, 6 through setting resistor RB.

Figure 5. Output sink current setting pin connections



■ OSCILLATOR FREQUENCY SETTING

The oscillator frequency can be set by connecting a timing capacitor (C_T) to the CT terminal (pin 22) and a timing resistor (R_T) to the RT terminal (pin 21) .

Oscillator frequency : f_{OSC}

$$f_{OSC}\ (kHz) \fallingdotseq \frac{1950000}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

■ METHOD OF SETTING TIME CONSTANT FOR TIMER-LATCH SHORT PROTECTION CIRCUIT

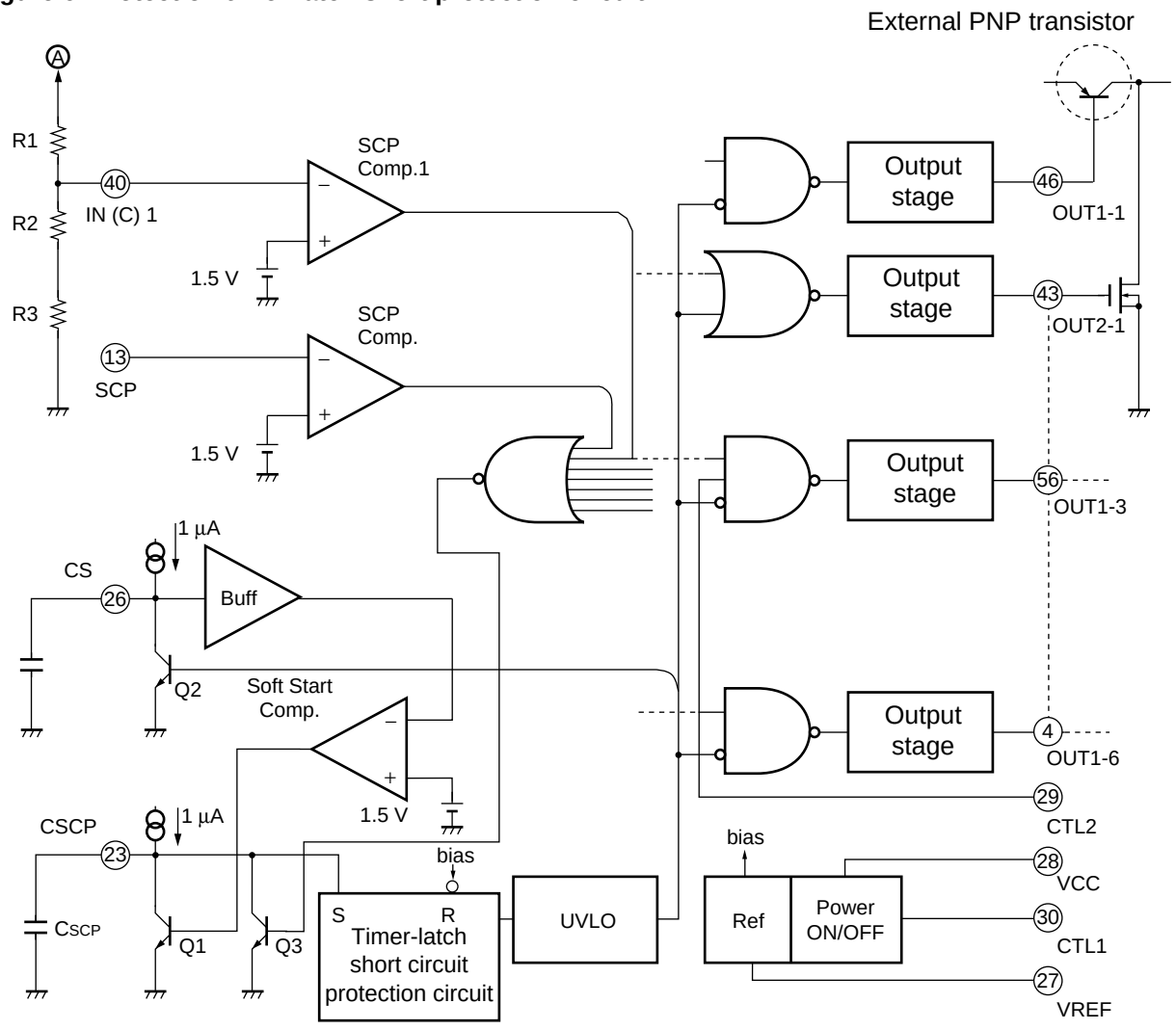
The short detection comparator (SCP comparator) in each of the channels constantly compares the error amplifier output level to the reference voltage and the SCP terminal (pin 13) .
While the switching regulator load conditions are stable on all channels, or when the voltage level at the SCP terminal is higher than the reference voltage, the short detection comparator output remains at “L” level, transistor Q3 is turned on, and the CSCP terminal (pin 23) is held at input standby voltage (V_{STB} ≒ 50 mV) .
If the load conditions change rapidly due to a short-circuiting of load, causing the output voltage to drop, or if the voltage at the SCP terminal falls below the reference voltage level, the output from the short detection comparator on the corresponding channel or the input at the SCP terminal goes to “H” level. This causes transistor Q3 to turn off and the external short protection capacitor C_{SCP} connected to the CSCP terminal to charge at 1.0 μA.

Short Detection Time (t_{PE})

t_{PE} (s) ≒ 0.7 × C_{SCP} (μF)

When the capacitor C_{SCP} is charged to the threshold voltage V_{TH} ≒ 0.7 V the SR latch is set, and the external PNP is turned off (inactive interval is set to 100%) . At this point the SR latch input is closed and the C_{SCP} terminal is held at input latch voltage (V_I ≒ 50 mV) .

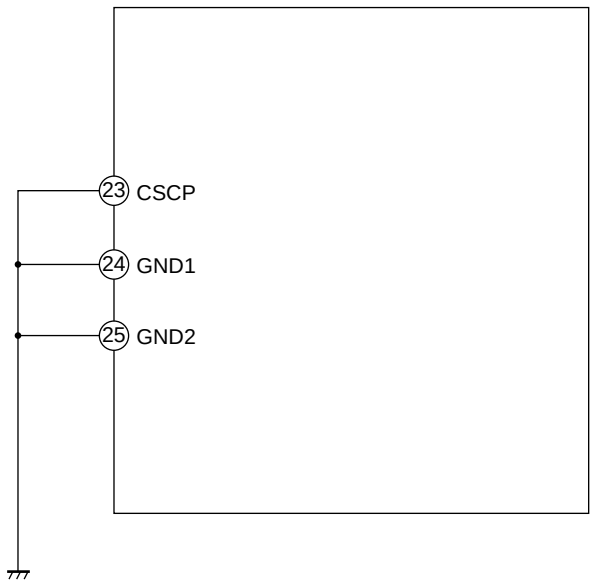
Figure 6. Protection timer-latch short protection circuit



■ TREATMENT WITHOUT USING CSCP

When you do not use the timer-latch short protection circuit, connect the CSCP terminal (pin 23) to GND with the shortest distance.

Figure 7. Treatment when not using CSCP



■ METHOD OF SETTING SOFT START TIME

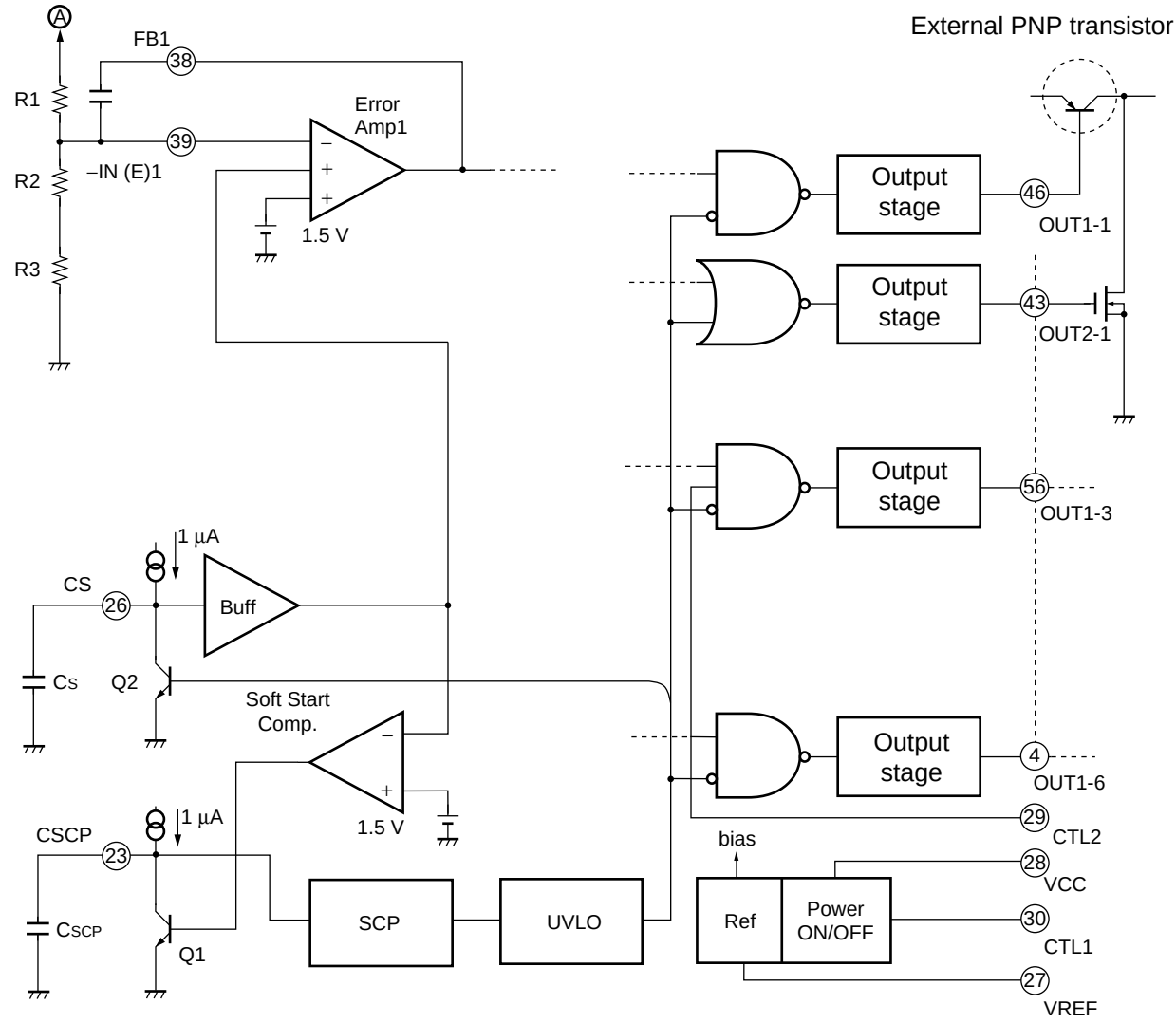
- Channels 1, 2, 4

To provide a soft start by preventing current surges at power-on, soft start capacitor (Cs) can be connected to the CS terminal (pin 26) .
When the IC is started (when the CTL1 terminal (pin 30) goes to “H” level, and $V_{CC} \geq$ UVLO threshold voltage) , transistors Q2 switches off and the CS terminal begins charging the external soft start capacitors (Cs) at 1.0 µA.
The error amplifier makes a soft start in a proportion to the output voltage to the CS teminal voltage regardless of the load current on the DC/DC converter.
Note that the soft start time can be calculated by the following formula.

Soft start time (output rise time)

t_S (s) ≒ 1.5 × C_S (µF) .

Figure 8. Soft start circuit

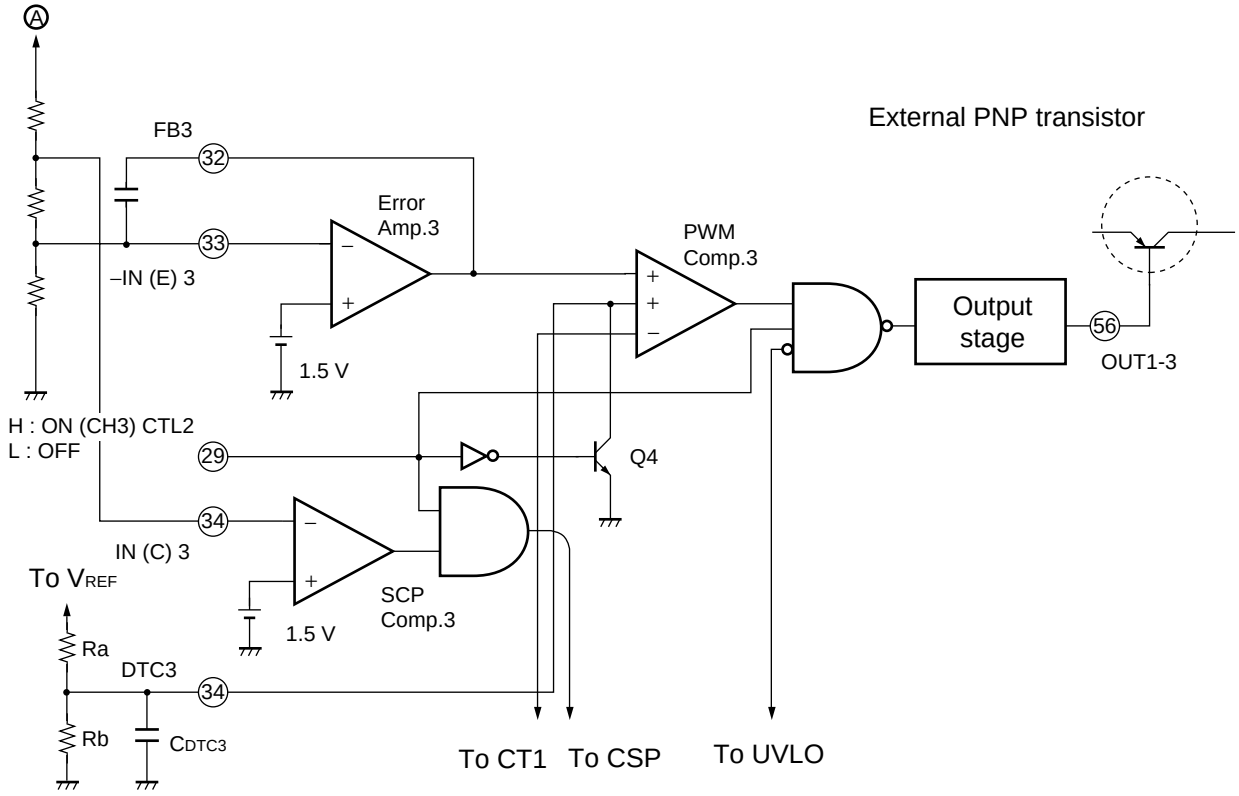


• Channel 3

The capacitor C_{DTC3} is placed between the DTC3 terminal (pin 31) and GND, so that when the CTL2 terminal (pin 29) goes from “L” to “H” level, the transistor Q4 is turned off and the output voltage is in proportion to the DTC3 terminal voltage providing the soft start operation.
As the short detection function is not turned off during soft start operation, this setting should be made under the following condition.

Channel 3 soft start circuit time < Short detection time

Figure 9. Channel 3 soft start circuit



■ PROCESSING WITHOUT USING CS TERMINAL

If the soft start function is not used, the CS terminal (pin 26) for channels 1, 2, and 4 should be left open. For channel 3, connect the DTC3 terminal (pin 31) to the V_{REF} terminal (pin 27) .

Figure 10. When no soft start time is set (1, 2, 4 channel)

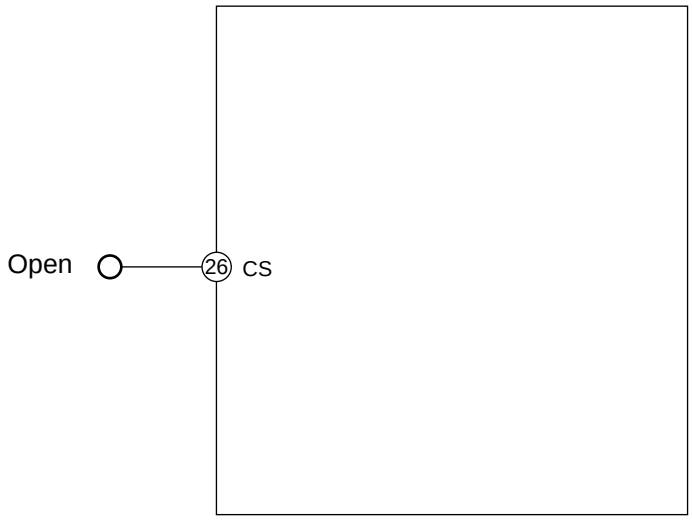
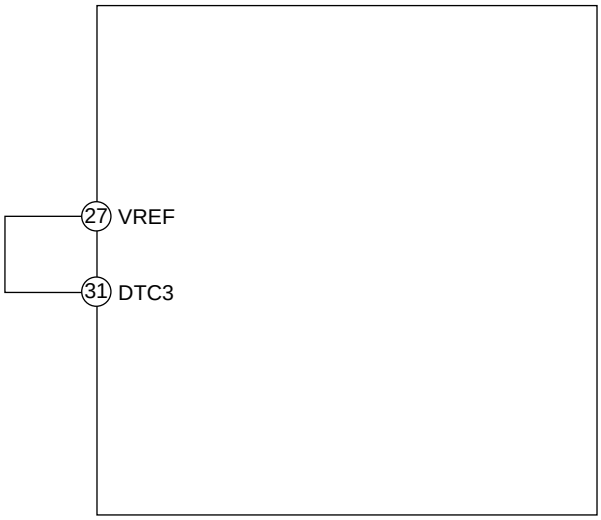


Figure 11. When no soft start time is set (3 channel)



■ METHOD OF SETTING THE DEAD TIME

When the device is set for step-up inverted output based on the flyback method, the output transistor is fixed to full-on state (ON-duty = 100%) at power switch-on.To prevent this problem, you may determine the voltages on the DTC3 terminal (pin 31) from the V_{REF} voltage so you can easily set the output transistor's dead time (maximum ON-duty) independently for each channel as shown Figure.12.

When the voltage on the DTC3 terminal is lower than the triangular-wave (CT1) output voltage from the oscillator, the output transistor turns off. The dead time calculation formula assuming that triangular-wave amplitude≒0.7 V and triangular-wave maximum voltage ≒1.35 V is given below.

$$\text{Duty (ON)}_{MAX} \fallingdotseq \frac{Vdt - 0.65}{0.7} \times 100\ [\%]$$

When you do not use this DTC3 terminal, connect then to V_{REF} terminal (pin 27) as shown Figure.13..

Figure 12. When using DTC to set dead time

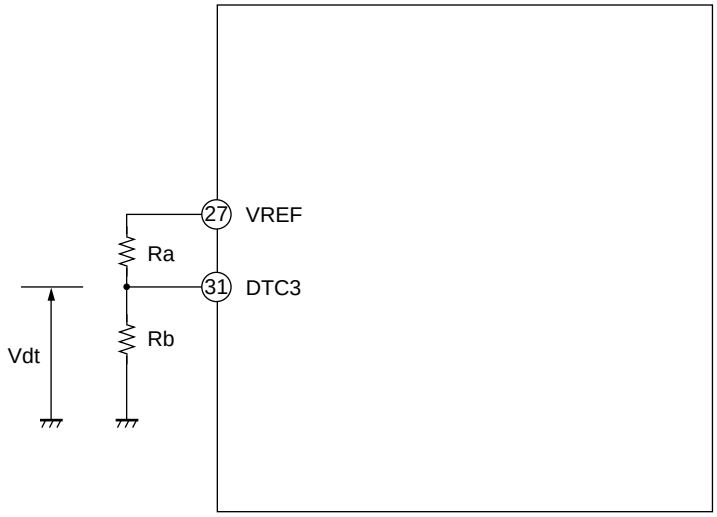
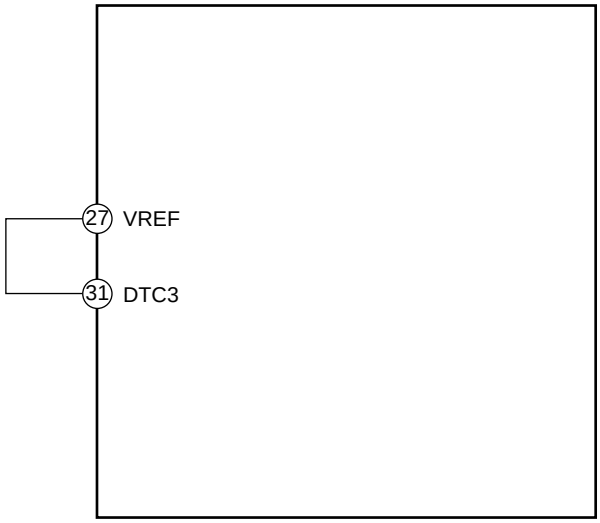
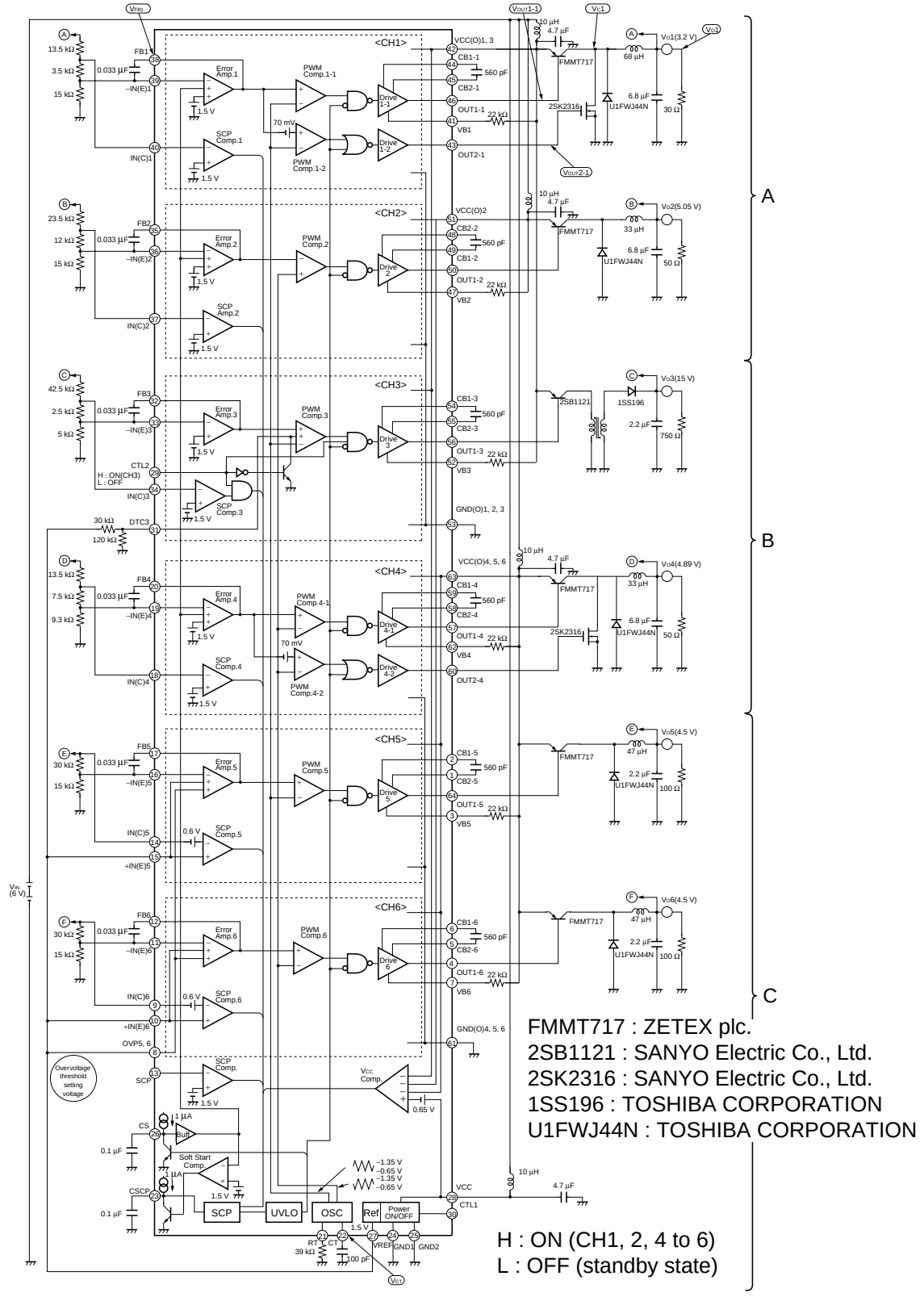


Figure 13. When not using DTC to set dead time



■ APPLICATION EXAMPLE

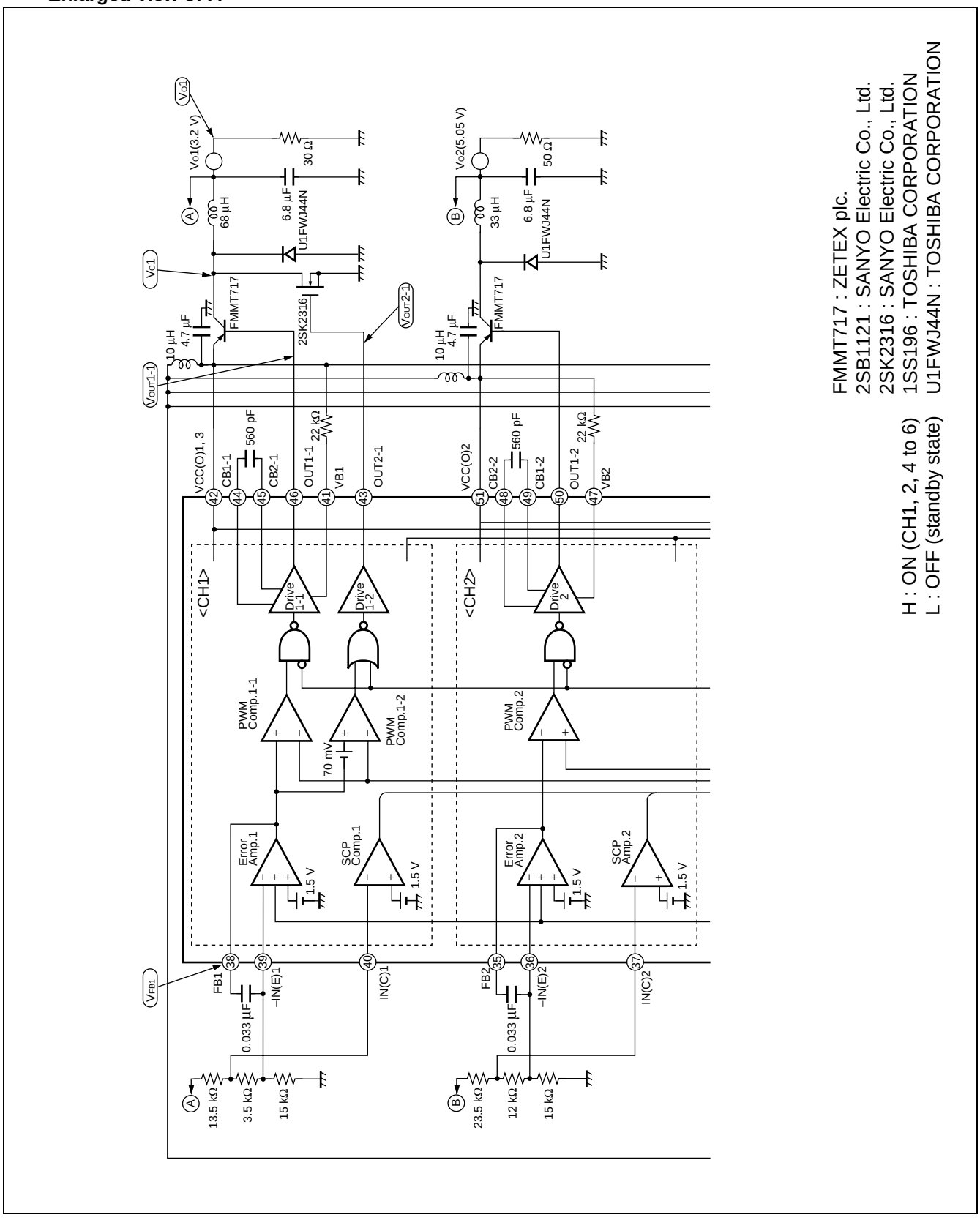
- **General view**



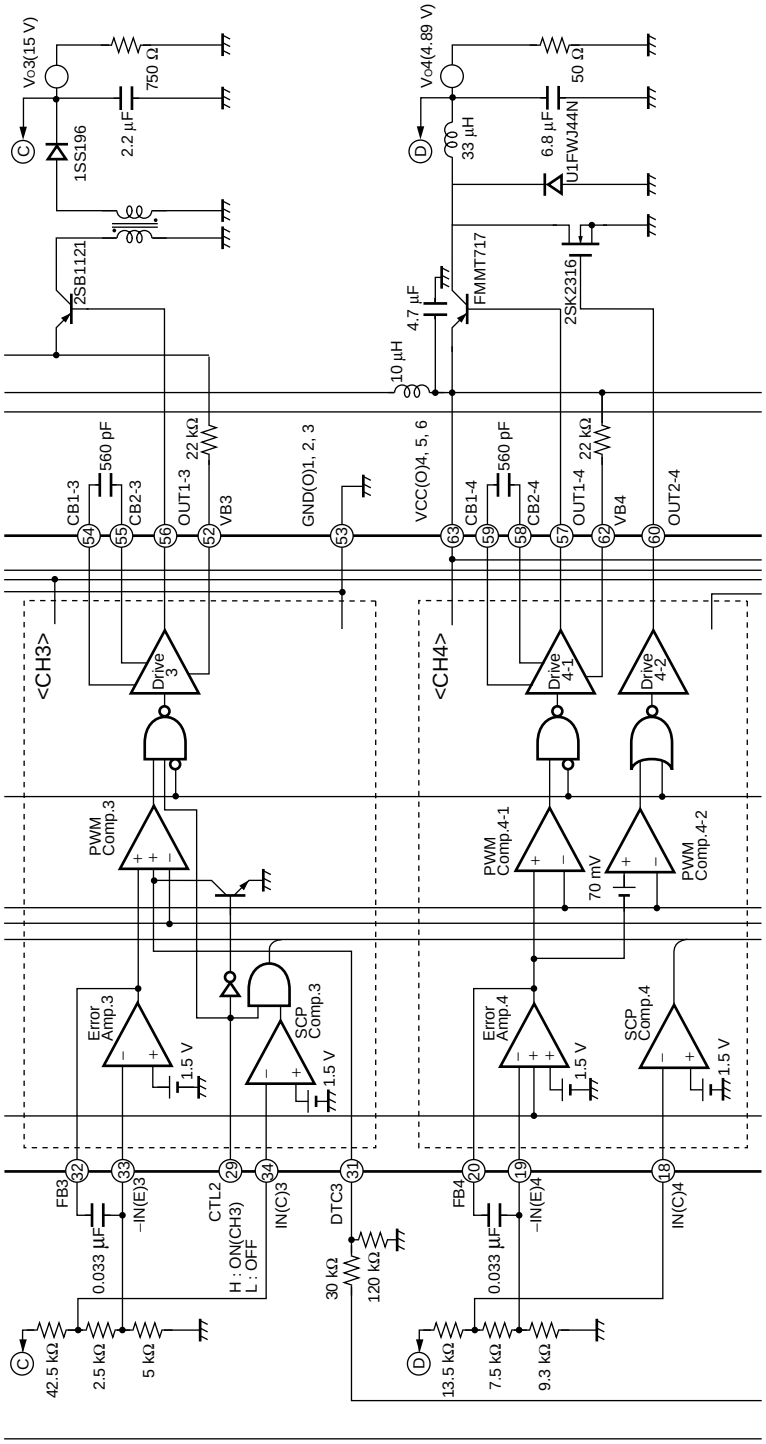
FMMT717 : ZETEX plc.
2SB1121 : SANYO Electric Co., Ltd.
2SK2316 : SANYO Electric Co., Ltd.
1SS196 : TOSHIBA CORPORATION
U1FWJ44N : TOSHIBA CORPORATION

H : ON (CH1, 2, 4 to 6)
L : OFF (standby state)

• **Enlarged view of A**



- **Enlarged view of B**



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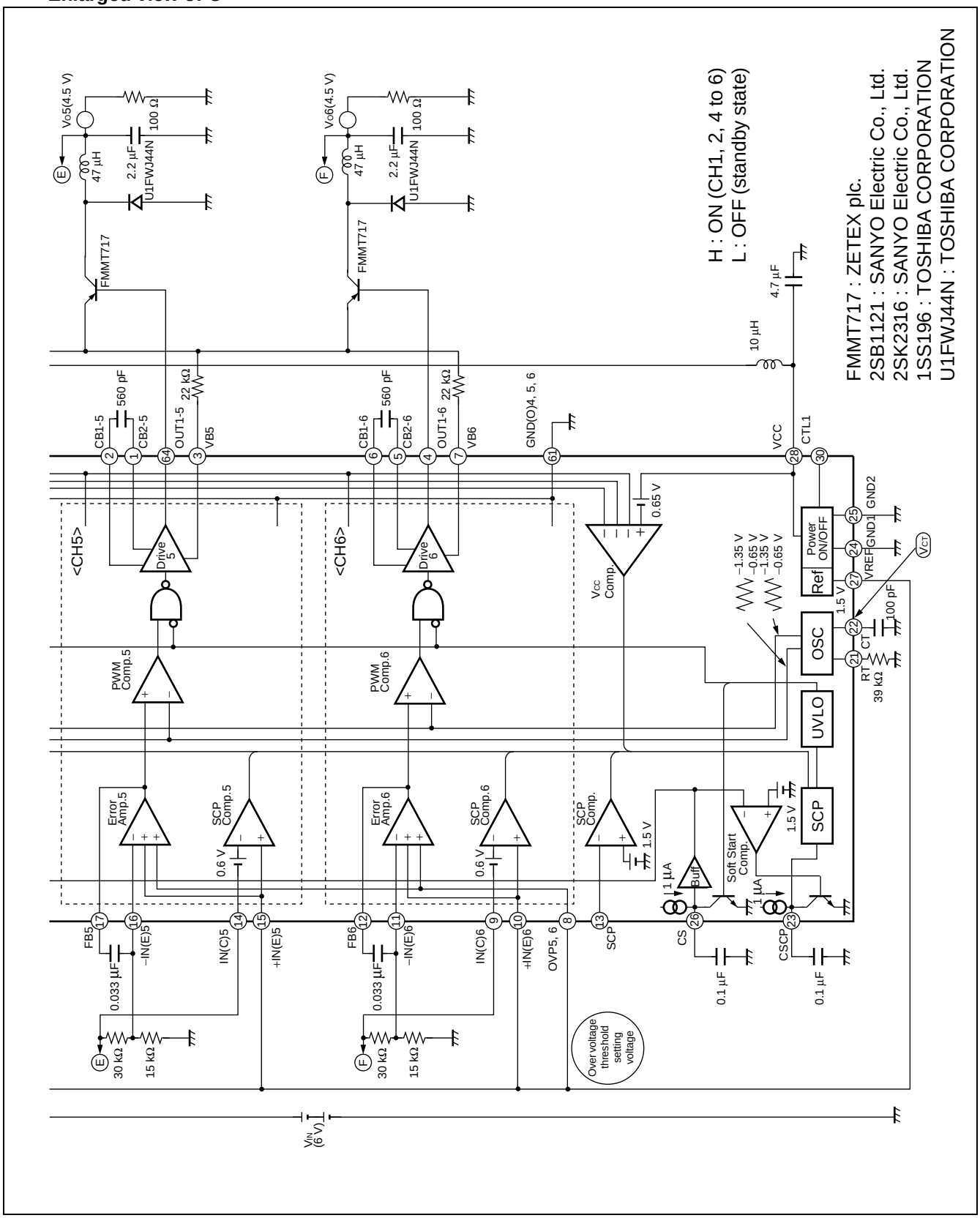
1SS196 : TOSHIBA CORPORATION
U1FWJ44N : TOSHIBA CORPORATION

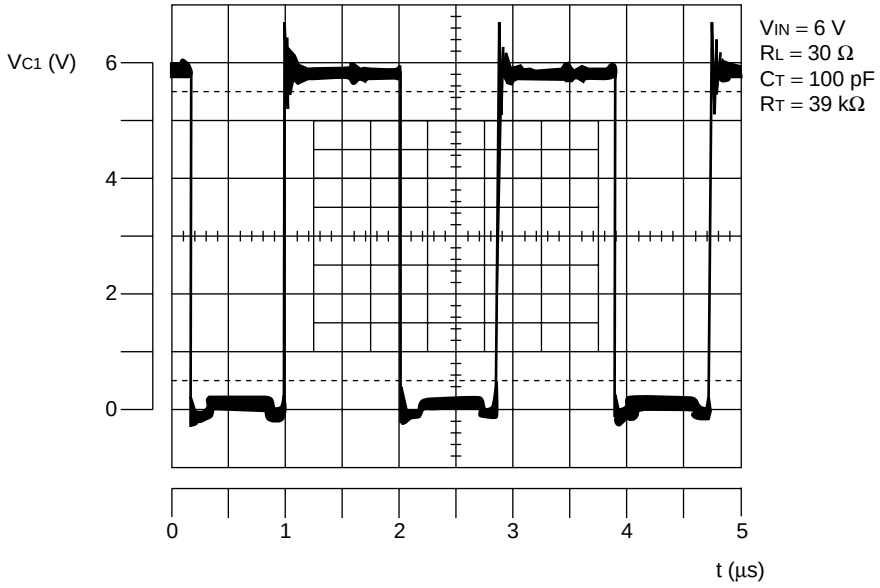
H : ON (CH1, 2, 4 to 6)
L : OFF (standby state)

- **Enlarged view of C**

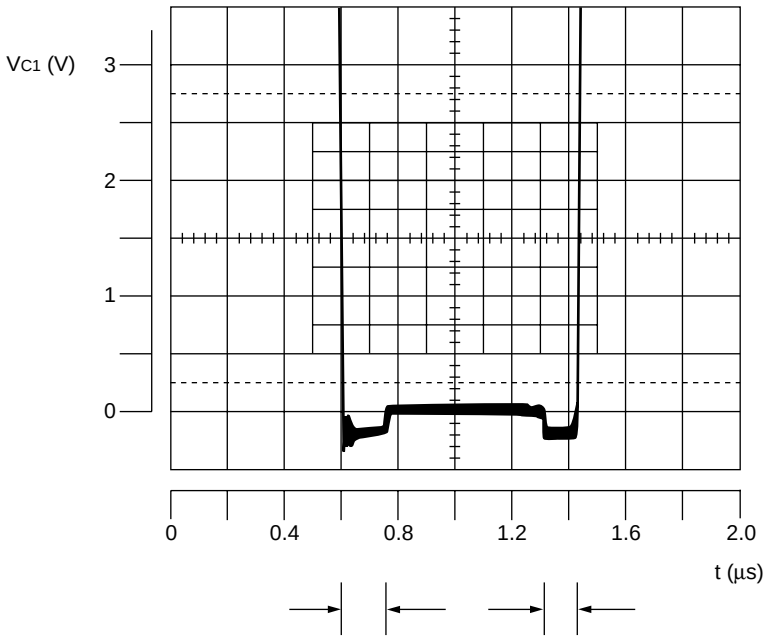


■ REFERENCE DATA

Channel 1 switching operation waveform (operation at 500 kHz)

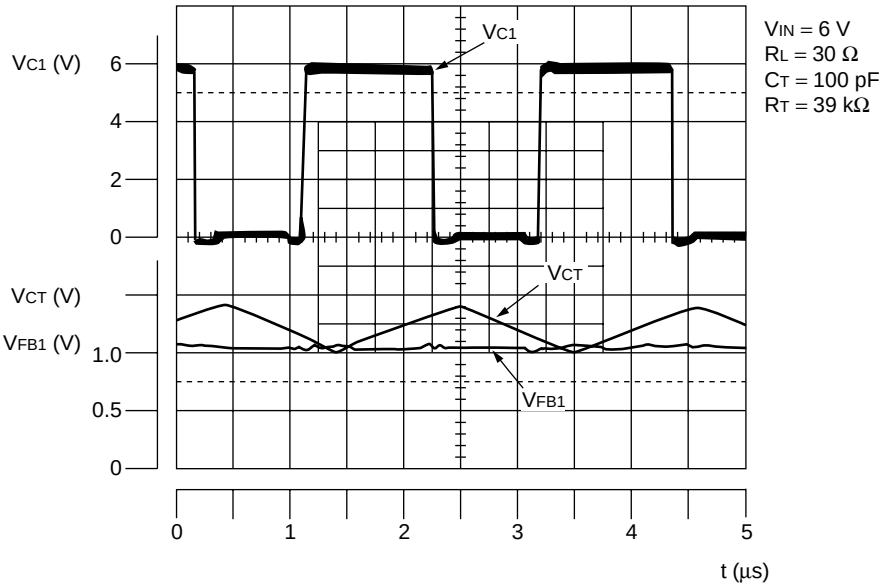


expansion

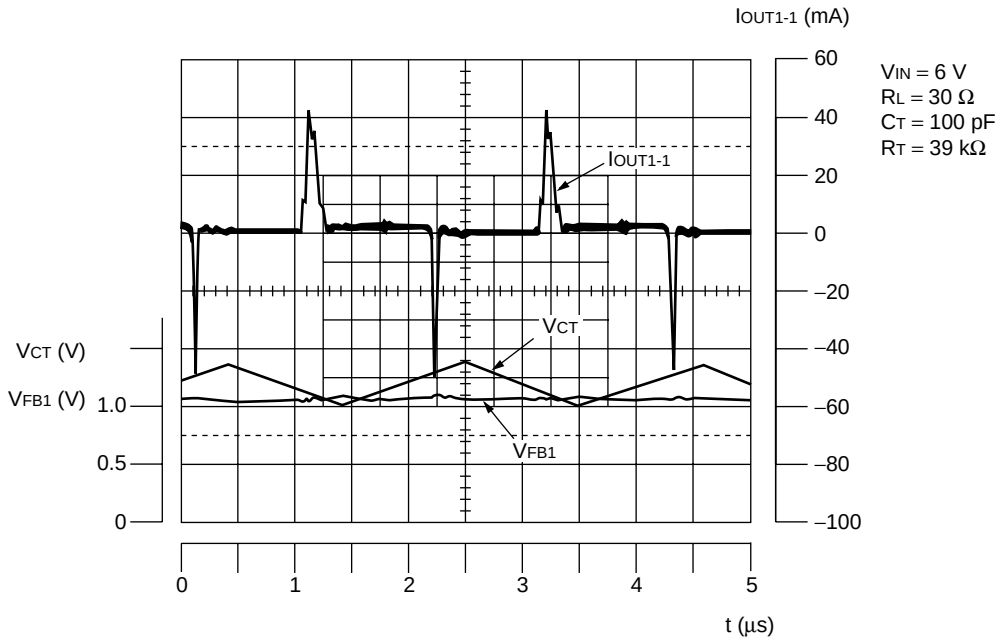


Synchronous rectifier length ÷150 ns ÷120 ns

Channel 1 main side output waveform (operation at 500 kHz)



Channel 1 main side base current waveform (operation at 500 kHz)

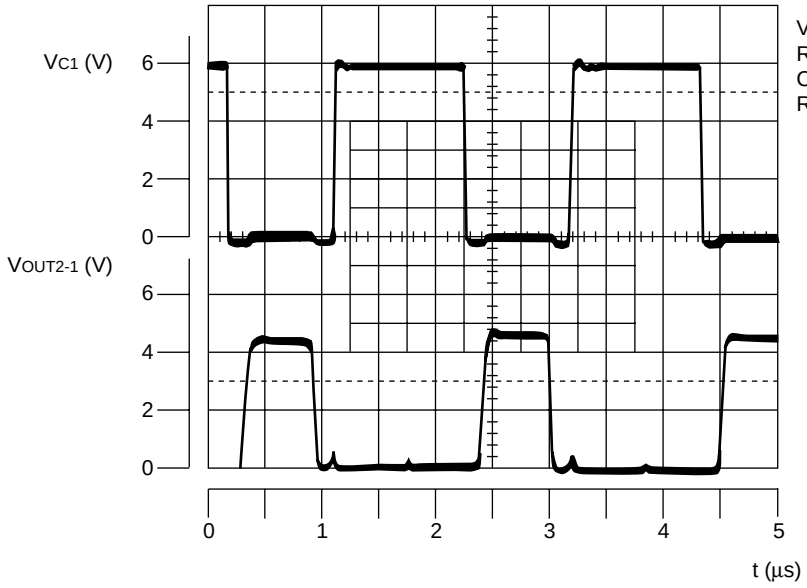


Peak current when turned ON ≒42 mA
Peak current when turned OFF ≒50 mA

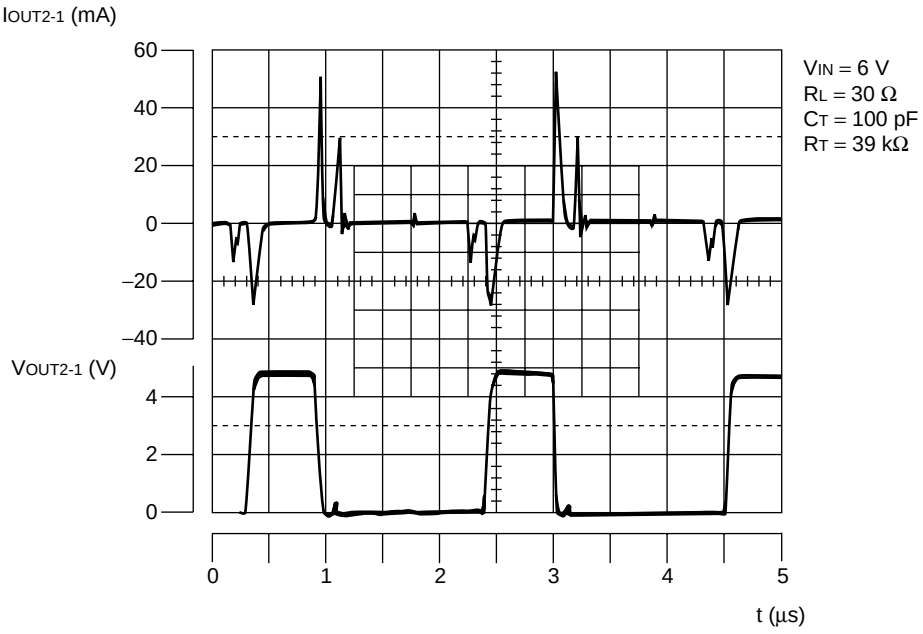
(Continued)

(Continued)

Channel 1 synchronous rectifier side output waveform (operation at 500 kHz)



Channel 1 synchronous rectifier side output waveform (operation at 500 kHz)



Output source current peak value ≒30 mA
Output sink current peak value ≒52 mA

■ USAGE PRECAUTIONS

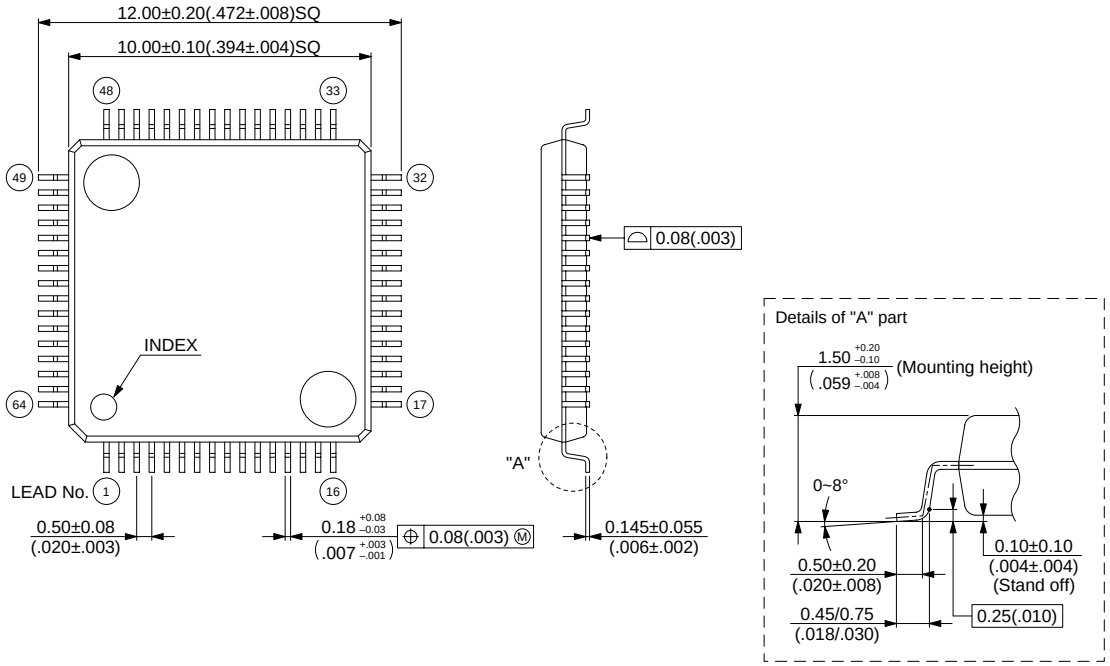
1. **Printed circuit board ground lines should be set up with consideration for common impedance.**
2. **Take the following measures for protection against static charge :**
   - For containing semiconductor devices, use an antistatic or conductive container.
   - When storing or transporting device-mounted circuit boards, use a conductive bag or container.
   - Ground the workbenches, tools, and measuring equipment to earth.
   - Make sure that operators wear wrist straps or other appropriate fittings grounded to earth via a resistance of 250 kΩ to 1 MΩ placed in series between the human body and earth.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3825APFV	64-pin plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSION

64-pin Plastic LQFP
(FPT-64P-M03)



Dimensions in : mm (inches)

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