FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27402-3E

ASSP

POWER-VOLTAGE MONITORING IC WITH WATCHDOG TIMER

MB3793-42

■ DESCRIPTION

The MB3793 is an integrated circuit to monitor power voltage; it incorporates a watchdog timer.
A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fail-safe function for various application systems.
There is also a mask option that can detect voltages of 4.9 to 2.4V in 0.1-V steps.
The model number and package code are as shown below.

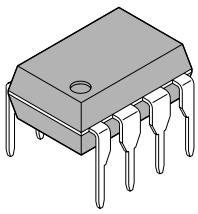
Model No.	Package code	Detection voltage
MB3793-42	3793-A	4.2 V

■ FEATURES

- Precise detection of power voltage fall: ±2.5%
- Detection voltage with hysteresis
- Low power dispersion: I_{CC} = 27 μA (reference)
- Internal dual-input watchdog timer
- Watchdog timer halt function (by inhibition terminal)
- Independently-set watchdog and reset times
- Mask option for detection voltage (4.9 to 2.4 V, 0.1-V steps)

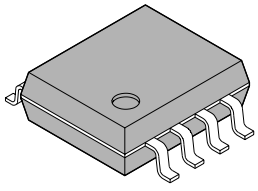
■ PACKAGES

8-pin plastic DIP



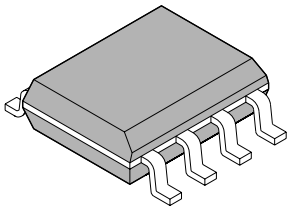
(DIP-8P-M01)

8-pin plastic SOP



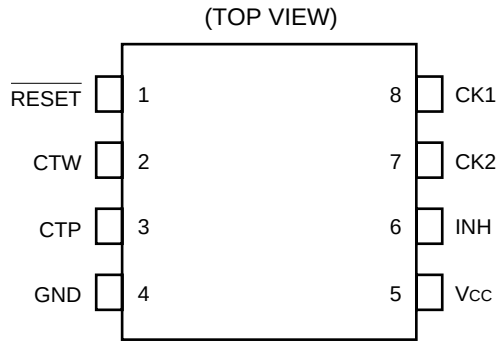
(FPT-8P-M01)

8-pin plastic SOL



(FPT-8P-M02)

■ PIN ASSIGNMENT

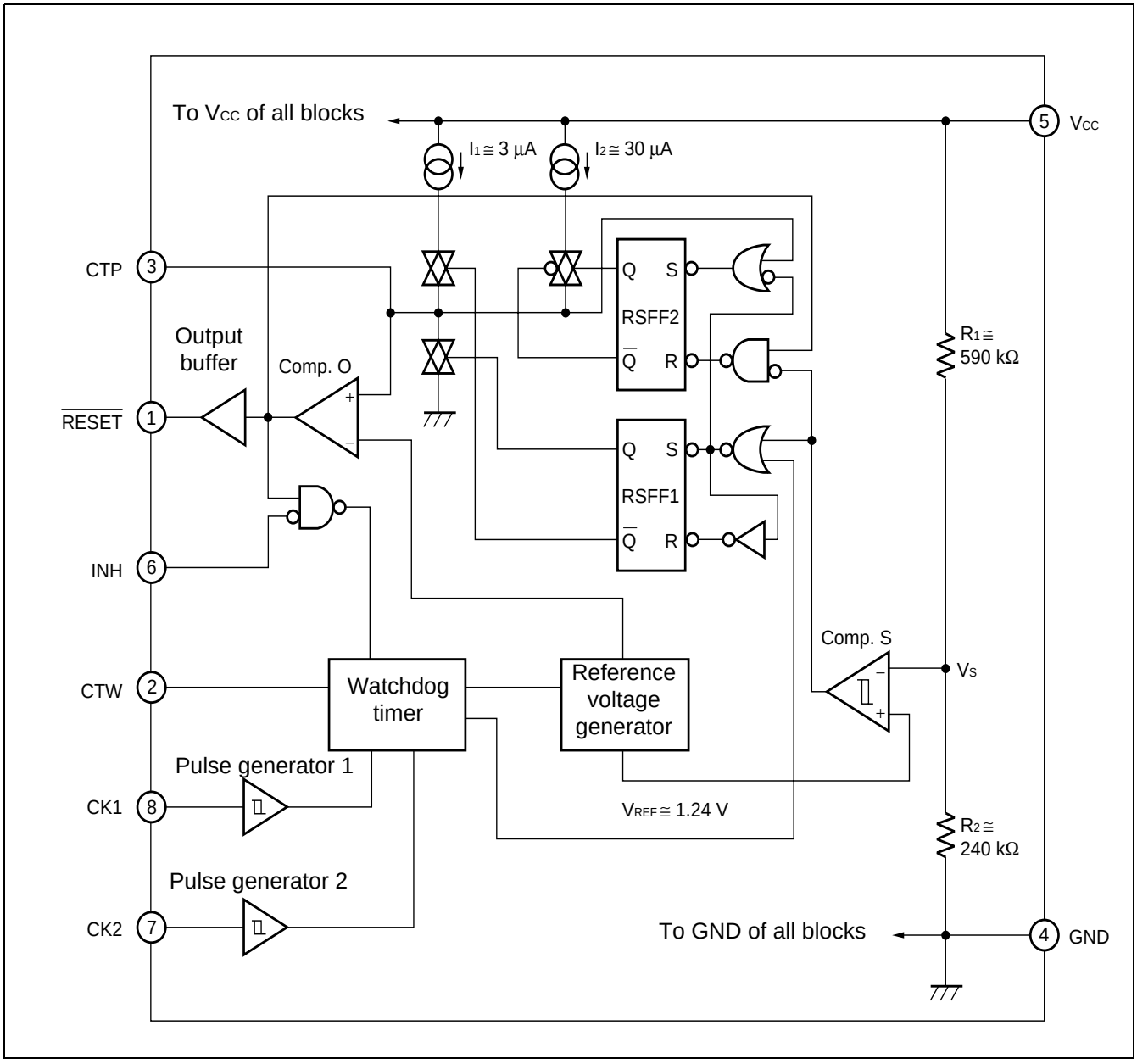


(DIP-8P-M01)
(FPT-8P-M01)
(FPT-8P-M02)

■ PIN DESCRIPTION

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\overline{\text{RESET}}$	Outputs reset	5	V_{CC}	Power supply
2	CTW	Sets monitoring time	6	INH	Inhibits watchdog timer function
3	CTP	Sets power-on reset hold time	7	CK2	Inputs clock 2
4	GND	Ground	8	CK1	Inputs clock 1

■ BLOCK DIAGRAM



■ BLOCK FUNCTIONS

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_S) that is the result of dividing the power voltage (V_{CC}) by resistors R_1 and R_2. When V_S falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality within 1 µs when the power is cut or falls abruptly.

2. Comp. O

Comp. O is a comparator to control the reset signal ($\overline{RESET}$) output and compares the threshold voltage with the voltage at the CTP terminal for setting the power-on reset hold time. When the voltage at the CTP terminal exceeds the threshold voltage, resetting is canceled.

3. Reset output buffer

Since the reset ($\overline{RESET}$) output buffer has CMOS organization, no pull-up resistor is needed.

4. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock terminals changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

5. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock terminals to monitor a single clock pulse.

6. Inhibition terminal

The inhibition (INH) terminal forces the watchdog timer on/off. When this terminal is High level, the watchdog timer is stopped.

7. Flip-flop circuit

The flip-flop circuit RSFF1 controls charging and discharging of the power-on reset hold time setting capacity (C_{TP}). The flip-flop circuit RSFF2 switches the charging accelerator for charging C_{TP} during resetting on/off. This circuit only functions during resetting and does not function at power-on reset.

■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25°C)

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power voltage*		V_{CC}	–0.3	+7	V
Input voltage*	CK1	V_{CK1}	–0.3	+7	V
	CK2	V_{CK2}			
	INH	V_{INH}			
Reset output voltage (direct current)	$\overline{RESET}$	I_{OL} I_{OH}	–10	+10	mA
Power dissipation (Ta ≤ +85°C)		P_D	—	200	mW
Storage temperature		Tstg	–55	+125	°C

*: The power voltage is based on the ground voltage (0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	1.2	5.0	6.0	V
Reset ($\overline{RESET}$) output current	I_{OL} I_{OH}	–5	—	+5	mA
Power-on reset hold time setting capacity	C_{TP}	0.001	0.1	10	µF
Watchdog timer monitoring time setting capacity	C_{TW}	0.001	0.1	1	µF
Watchdog timer monitoring time	t_{WD}	0.1	—	1500	ms
Operating ambient temperature	Ta	–40	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{CC} = +5 V , Ta = +25°C)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Power current	I_{CC1}	Watchdog timer operation*1		—	27	50	µA
	I_{CC2}	Watchdog timer halt*2		—	25	45	
Detection voltage	V_{SL}	V_{CC} falling	Ta = +25°C	4.10	4.20	4.30	V
			Ta = –40 to +85°C	4.05	4.20	4.35	
	V_{SH}	V_{CC} rising	Ta = +25°C	4.20	4.30	4.40	V
			Ta = –40 to +85°C	4.15	4.30	4.45	
Detection voltage hysteresis difference	V_{SHYS}	V_{SH} - V_{SL}		50	100	150	mV
CK input threshold voltage	V_{CIH}	—		(1.4)	1.9	(2.5)	V
	V_{CIL}	—		(0.8)	1.3	(1.8)	V
CK input hysteresis	V_{CHYS}	—		(0.4)	0.6	(0.8)	V
INH input voltage	V_{IIH}	—		3.5	—	V_{CC}	V
	V_{IIL}	—		0	0	0.8	V
Input current (CK1,CK2,INH)	I_{IH}	V_{CK} = V_{CC}		—	0	1.0	µA
	I_{IL}	V_{CK} = 0 V		–1.0	0	—	µA
Reset output voltage	V_{OH}	$I_{\overline{RESET}}$ = –5 mA		4.5	4.75	—	V
	V_{OL}	$I_{\overline{RESET}}$ = +5 mA		—	0.12	0.4	V
Reset-output minimum power voltage	V_{CCL}	$I_{\overline{RESET}}$ = +50 µA		—	0.8	1.2	V

*1: At clock input terminals CK1 and CK2, the pulse input frequency is 1 kHz and the pulse amplitude is 0 V to V_{CC}.

*2: Inhibition input is at High level.

2. AC Characteristics

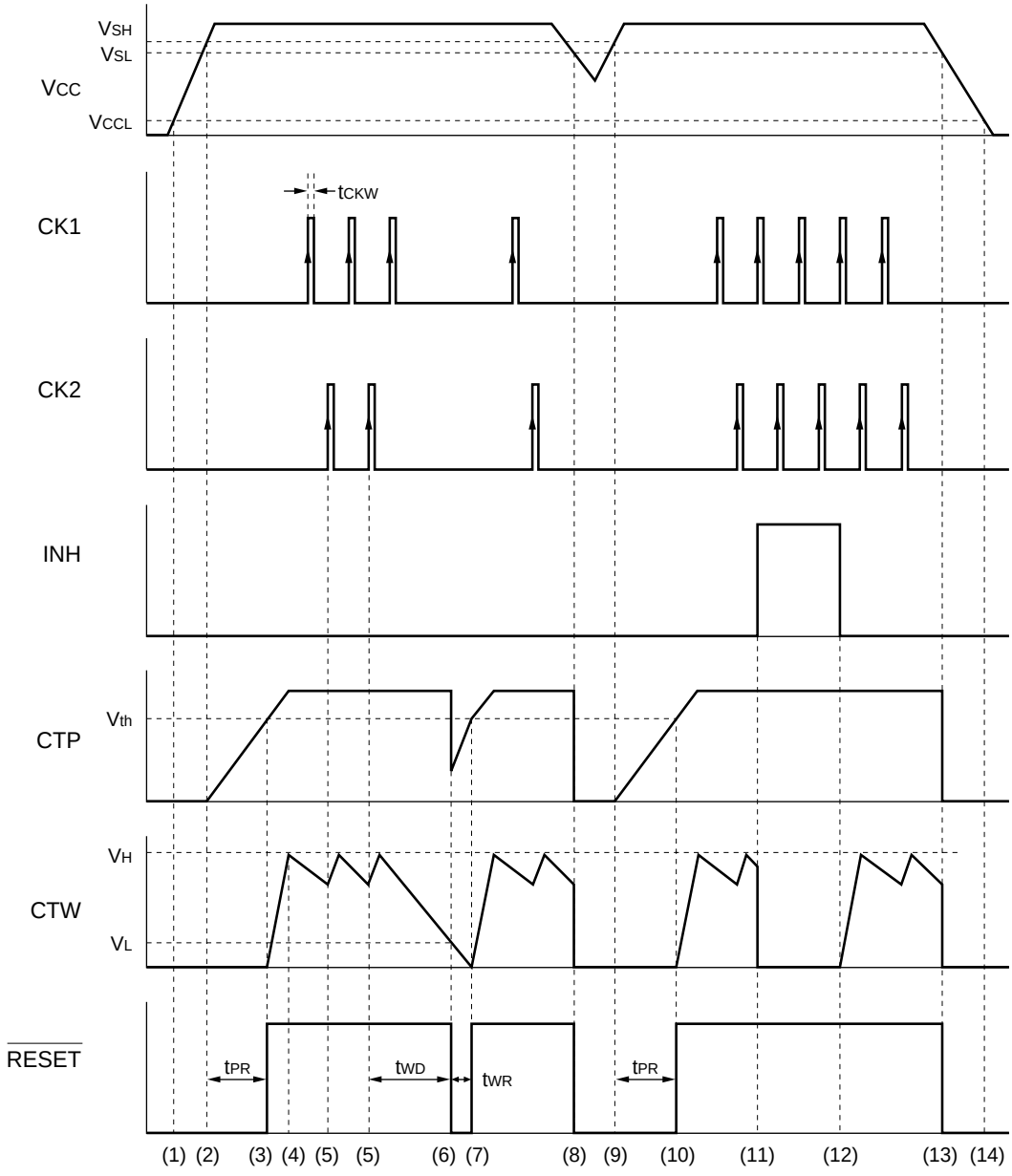
(V_{CC} = +5 V , Ta = +25°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power-on reset hold time		t_{PR}	C_{TP} = 0.1 µF	80	130	180	ms
Watchdog timer monitoring time		t_{WD}	C_{TW} = 0.01 µF C_{TP} = 0.1 µF	7.5	15	22.5	ms
Watchdog timer reset time		t_{WR}	C_{TP} = 0.1 µF	5	10	15	ms
CK input pulse duration		t_{CKW}	—	500	—	—	ns
CK input pulse cycle		t_{CKT}	—	20	—	—	µs
Reset ($\overline{\text{RESET}}$) output transition time	Rising	tr*	C_L = 50pF	—	—	500	ns
	Falling	tf*	C_L = 50pF	—	—	500	ns

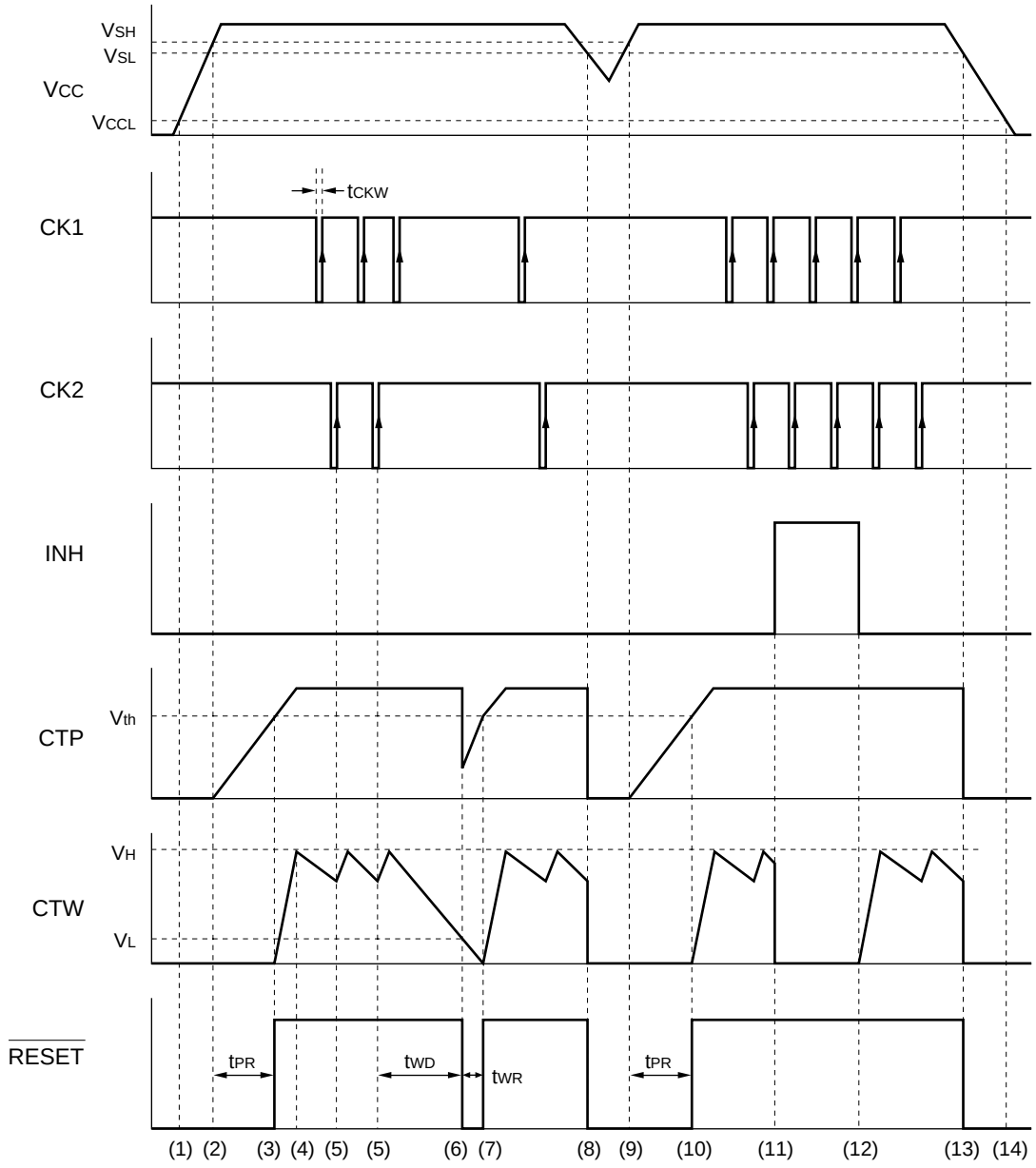
*: The voltage range is 10% to 90% at testing the reset output transition time.

■ TIMING DIAGRAM

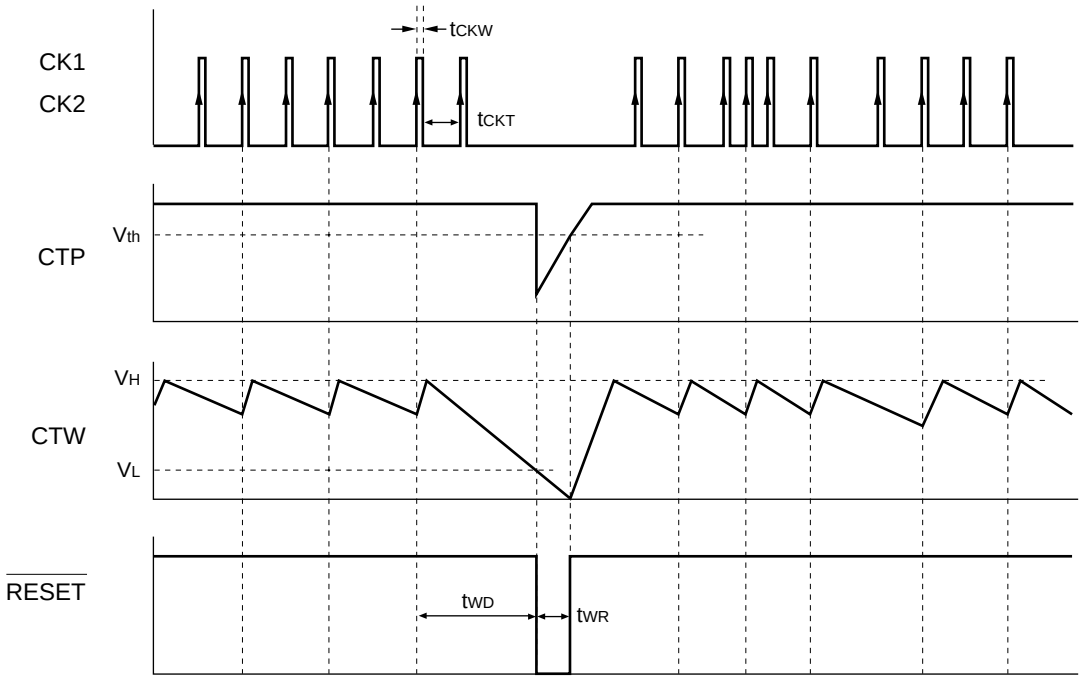
1. Basic operation (Positive clock pulse)



2. Basic operation (Negative clock pulse)

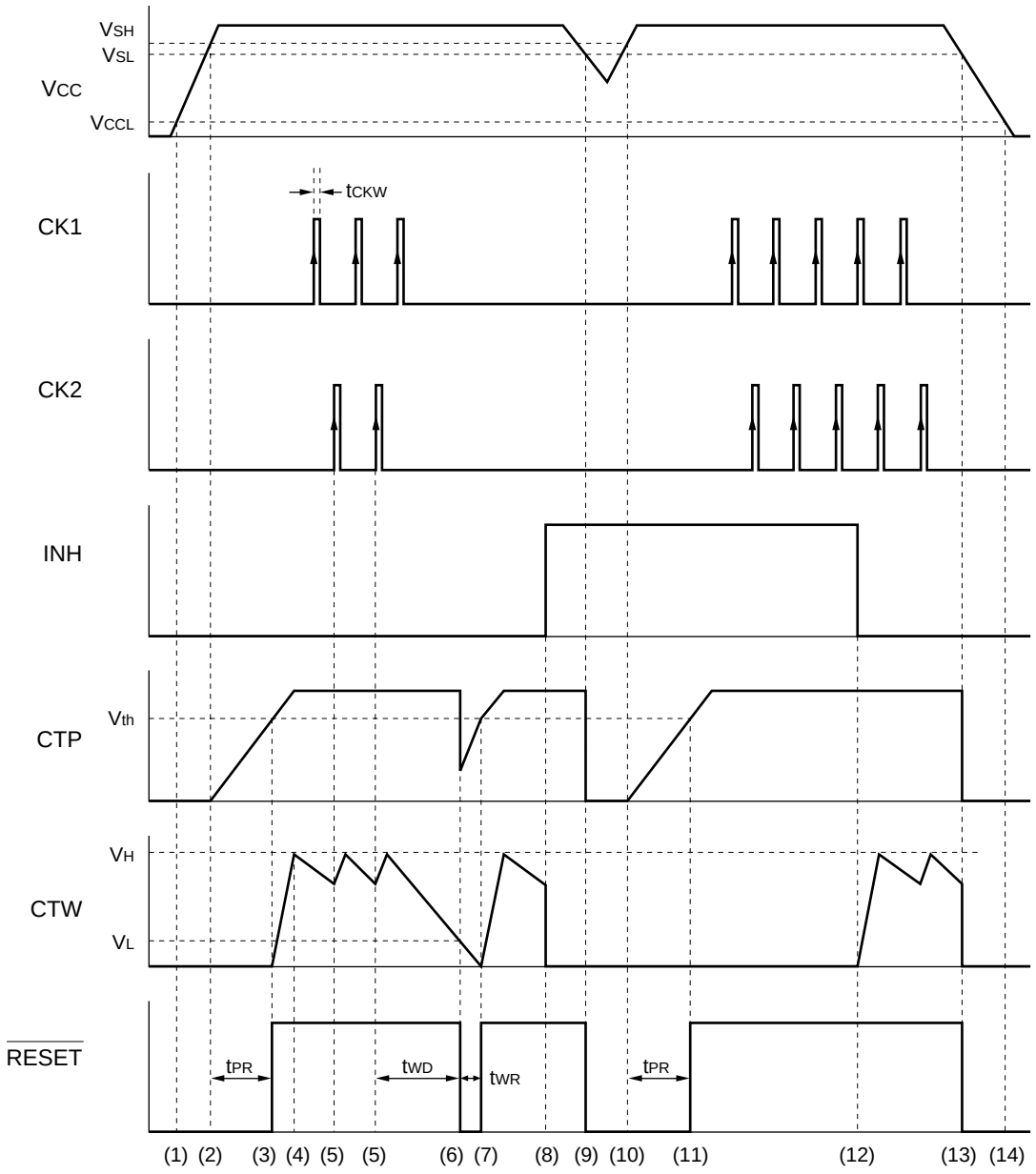


3. Single-clock input monitoring (Positive clock pulse)

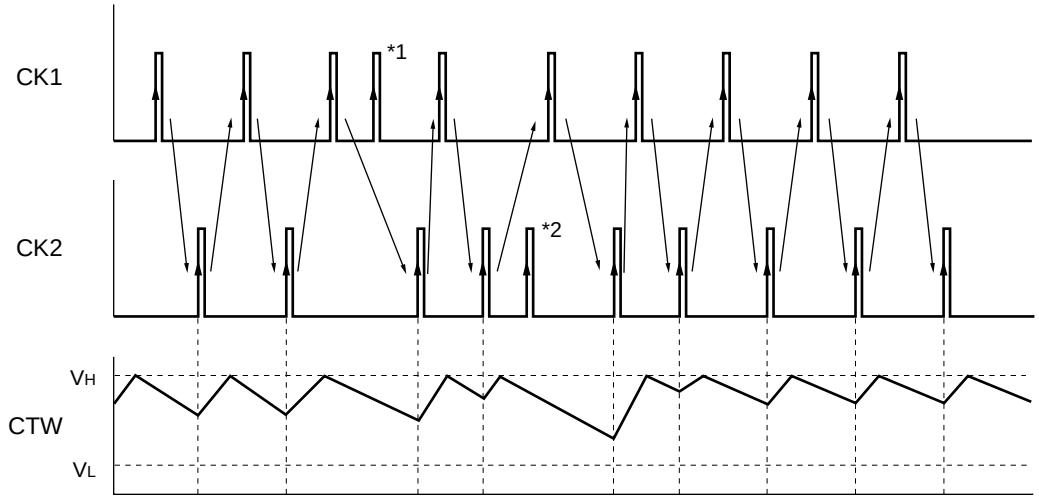


Note: The MB3793 can monitor only one clock.
The MB3793 checks the clock signal at every other input pulse. Therefore, set watchdog timer monitor time t_{WD} to the time that allows the MB3793 to monitor the period twice as long as the input clock pulse.

4. Inhibition operation (Positive clock pulse)

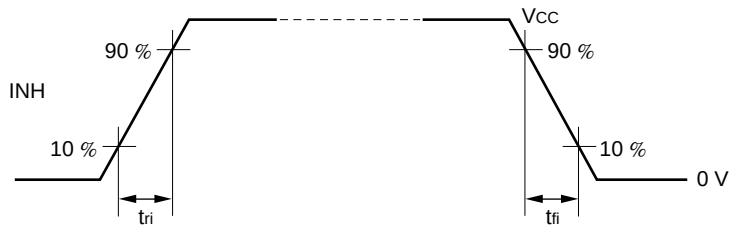


5. Clock pulse input (Positive clock pulse)



Note: The MB3793 watchdog timer monitors Clock 1 (CK1) and Clock 2 (CK2) pulses alternately. When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.
When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored. In the above figure, pulses *1 and *2 are ignored.

6. Inhibition input rising and falling time



■ OPERATION SEQUENCE

The operation sequence is explained by using "■ TIMING DIAGRAM 1. Basic operation (Positive clock pulse)". The following item numbers correspond to the numbers in "■ TIMING DIAGRAM 1. Basic operation (Positive clock pulse)".

(1) When the power voltage (V_{CC}) reaches about 0.8 V (V_{CCL}), a reset signal is output.

(2) When V_{CC} exceeds the rising-edge detection voltage (V_{SH}), charging of power-on reset hold time setting capacitance (C_{TP}) is started. V_{SH} is about 4.3 V.

(3) When the voltage at the CTP terminal setting the power-on reset hold time exceeds the threshold voltage (V_{th}), resetting is canceled and the voltage at the $\overline{\text{RESET}}$ terminal changes to High level to start charging of the watchdog timer monitoring time setting capacitance (C_{TW}). Vth is about 3.6 V.

The power-on reset hold time (t_{PR}) can be calculated by the following equation.

$$t_{PR}\ (\text{ms}) \approx A \times C_{TP}\ (\mu\text{F})$$

Where, A is about 1300.

(4) When the voltage at the CTW terminal setting the monitoring time reaches High level (V_H), C_{TW} switches to discharging from charging. V_H is about 1.24 V (reference value).

(5) When clock pulses are input to the CK2 terminal during C_{TW} discharging after clock pulses are input to the CK1 terminal—positive-edge trigger, C_{TW} switches to charging.

(6) If clock pulse input does not occur at either the CK1 or CK2 clock terminals during the watchdog timer monitoring time (t_{WD}), the CTW voltage falls below Low level (V_L), a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ terminal changes to Low level. V_L is about 0.24 V.

t_{WD} can be calculated from the following equation.

$$t_{WD}\ (\text{ms}) \approx B \times C_{TW}\ (\mu\text{F}) + C \times C_{TP}\ (\mu\text{F})$$

Where, B is about 1500. C is about 3; it is much smaller than B.
Hence, when $C_{TP} / C_{TW} \leq 10$, the calculation can be simplified as follows:

$$t_{WD}\ (\text{ms}) \approx B \times C_{TW}\ (\mu\text{F})$$

(7) When the voltage of the CTP terminal exceeds V_{th} again as a result of recharging C_{TP}, resetting is canceled and the watchdog timer restarts monitoring.

The watchdog timer reset time (t_{WR}) can be calculated by the following equation.

$$t_{WR}\ (\text{ms}) \approx D \times C_{TP}\ (\mu\text{F})$$

Where, D is about 100.

(8) When V_{CC} falls below the rising-edge detection voltage (V_{SL}), the voltage of the CTP terminal falls and a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ terminal changes to Low level. V_{SL} is about 4.2 V.

(9) When V_{CC} exceeds V_{SH}, C_{TP} begins charging.

(10) When the voltage of the CTP terminal exceeds V_{th}, resetting is canceled and the watchdog timer restarts.

(11) When an inhibition signal is input (INH terminal is High level), the watchdog timer is halted forcibly.
In this case, V_{CC} monitoring is continued without the watchdog timer.
The watchdog timer does not function unless this inhibition input is canceled.

(12) When the inhibition input is canceled (INH terminal is Low level), the watchdog timer restarts.

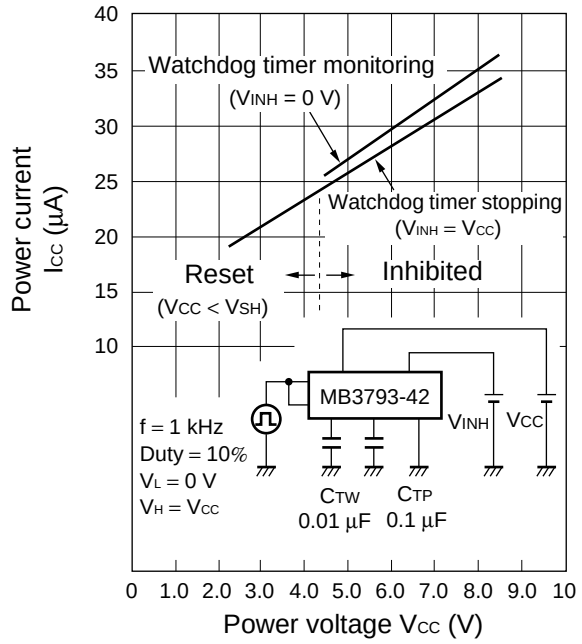
(13) When the V_{CC} voltage falls below V_{SL} after power-off, a reset signal is output.

(14) When the power voltage (V_{CC}) falls below about 0.8 V (V_{CCL}) , a reset signal is released.

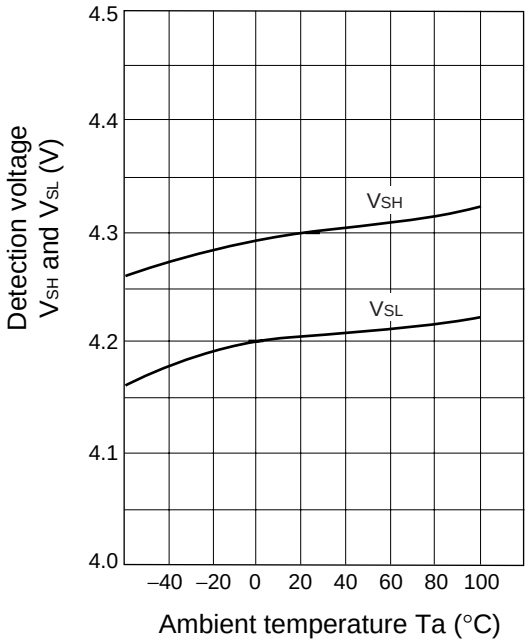
Similar operation is also performed for negative clock-pulse input ("■ TIMING DIAGRAM 2. Basic operation (Negative clock pulse)").
Short-circuit the clock terminals CK1 and CK2 to monitor a single clock. The basic operation is the same but the clock pulses are monitored at every other pulse (■ TIMING Diagram 3. Single-clock input monitoring).

■ TYPICAL CHARACTERISTICS

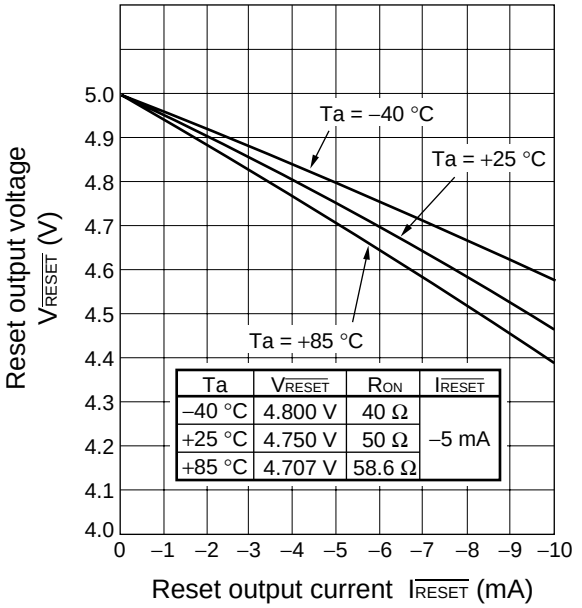
Power Current - Power Voltage



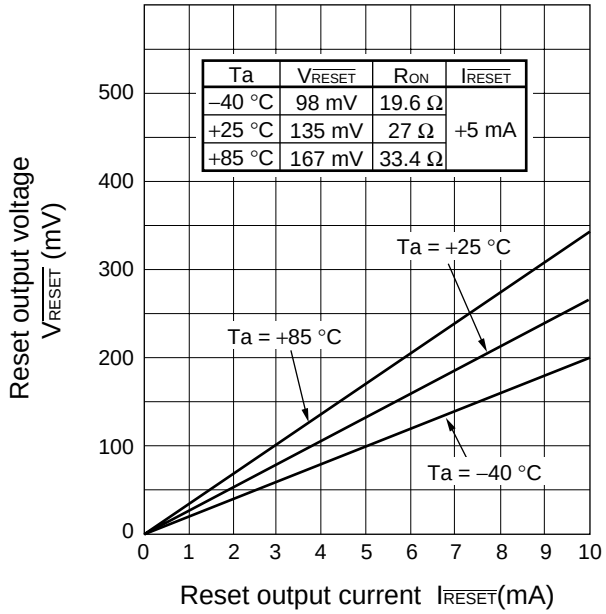
Detection Voltage - Ambient Temperature



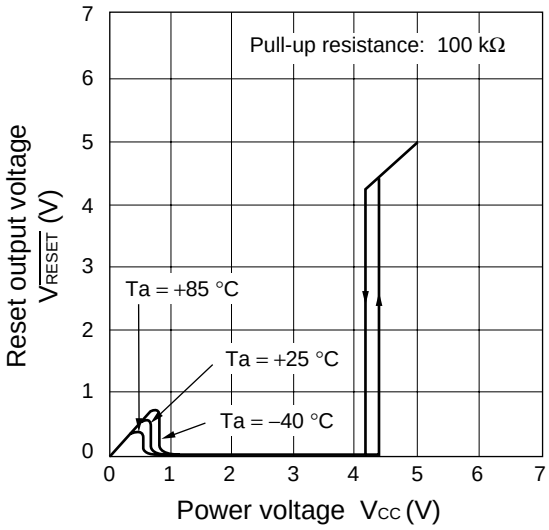
Reset Output Voltage - Reset Output Current (P-MOS side)



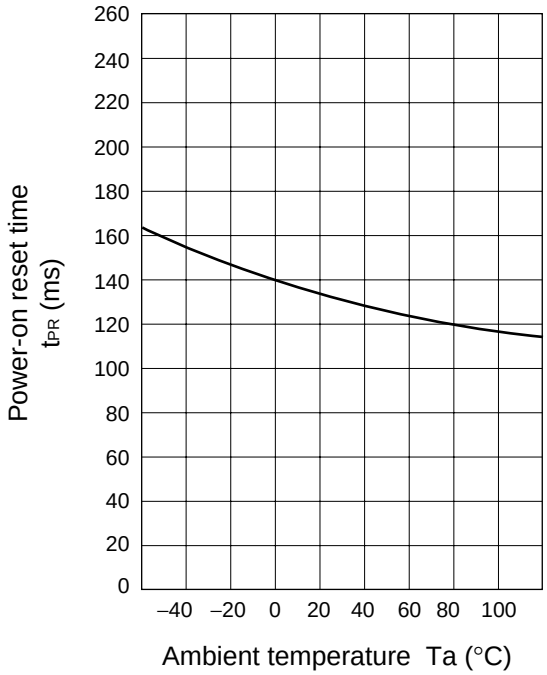
Reset Output Voltage - Reset Output Current (N-MOS side)



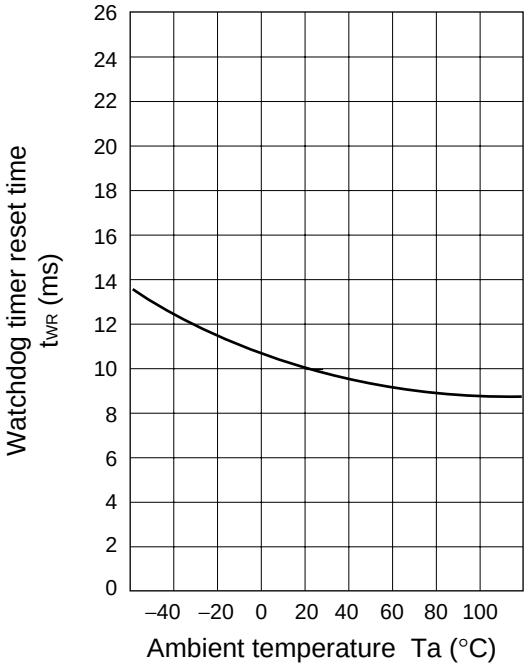
Reset Output Voltage - Power Voltage



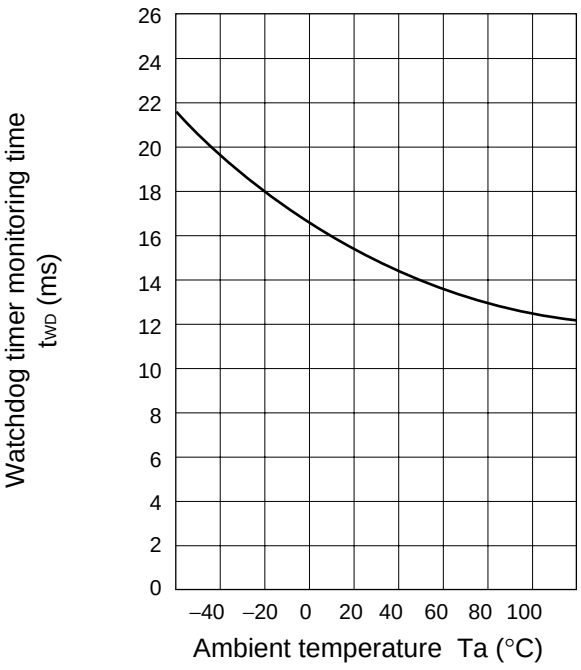
Reset-on Reset Time - Ambient Temperature (when V_{CC} rising)



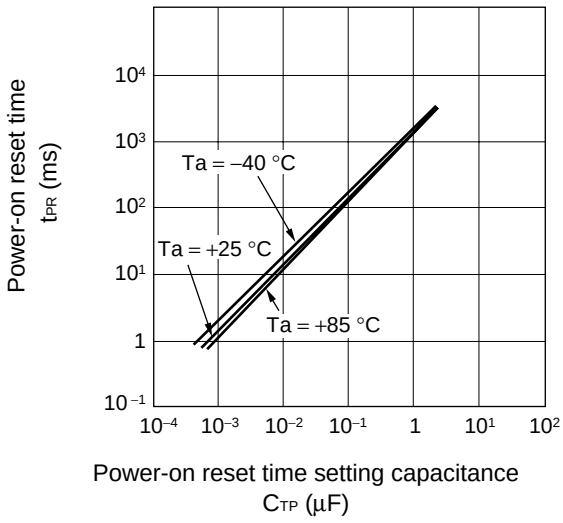
Watchdog Timer Reset Time - Ambient Temperature (when monitoring)



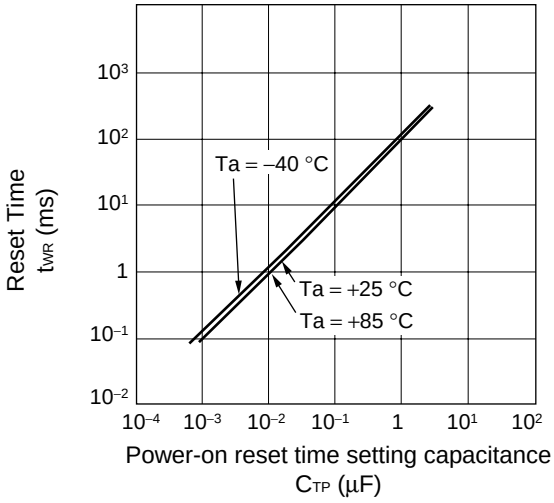
Watchdog Timer Monitoring Time - Ambient Temperature



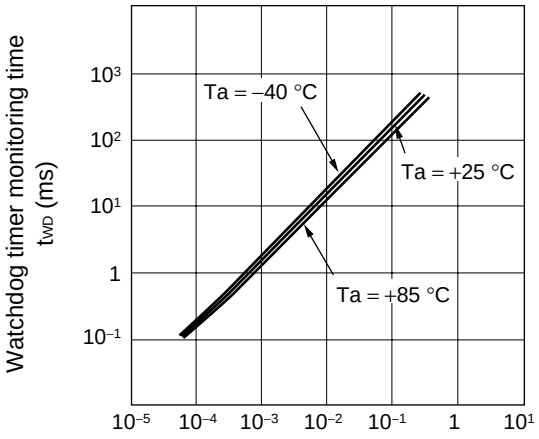
Power-on Reset Time - C_{TP} Capacitance



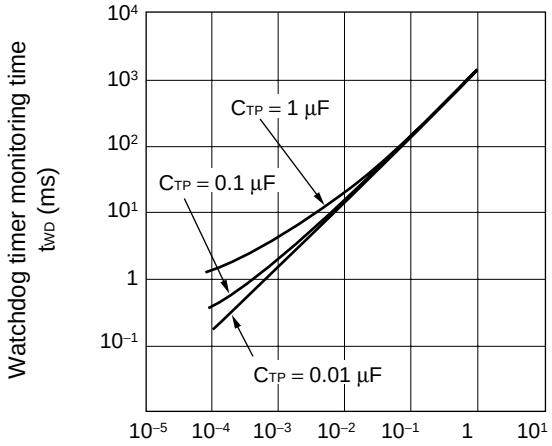
Reset Time - C_{TP} Capacitance



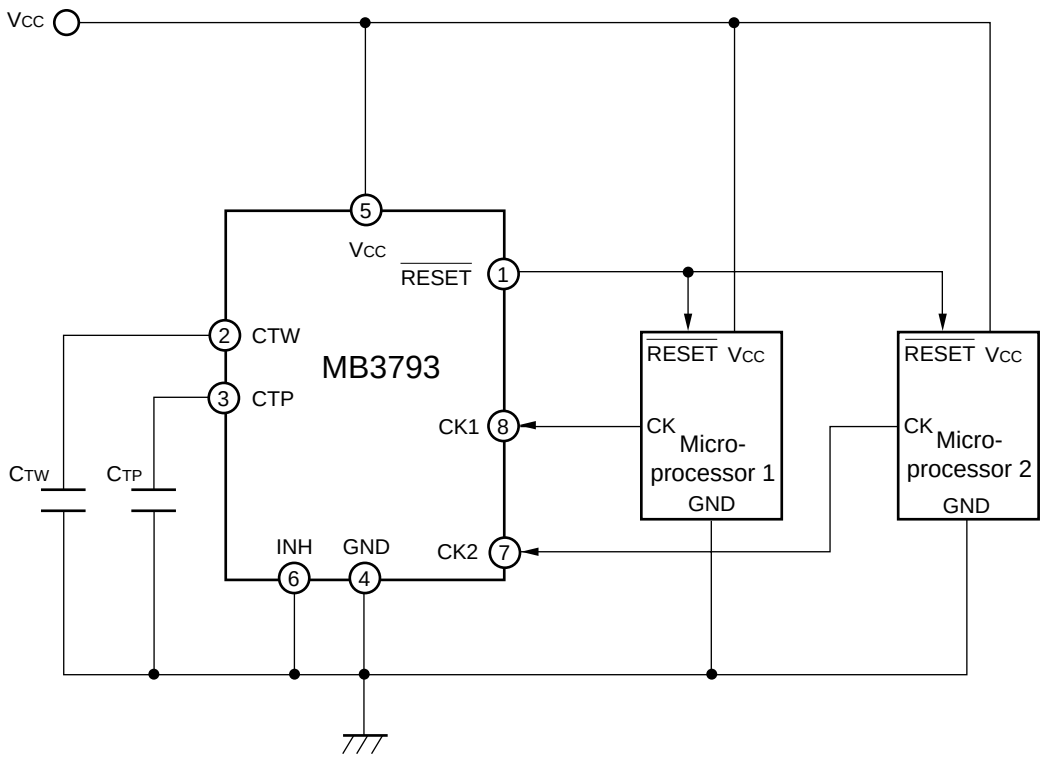
Watchdog Timer Monitoring Time - C_{TW} Capacitance (under Ta condition)



Watchdog Timer Monitoring Time - C_{TW} Capacitance



■ STANDARD CONNECTION



Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

t_{PR} (ms) ≈ A × C_{TP} (µF)

t_{WD} (ms) ≈ B × C_{TW} (µF) + C × C_{TP} (µF)

However, when $C_{TP}/C_{TW} \leq 10$,

t_{WD} (ms) ≈ B × C_{TW} (µF)

t_{WR} (ms) ≈ D × C_{TP} (µF)

Value of A, B, C and D

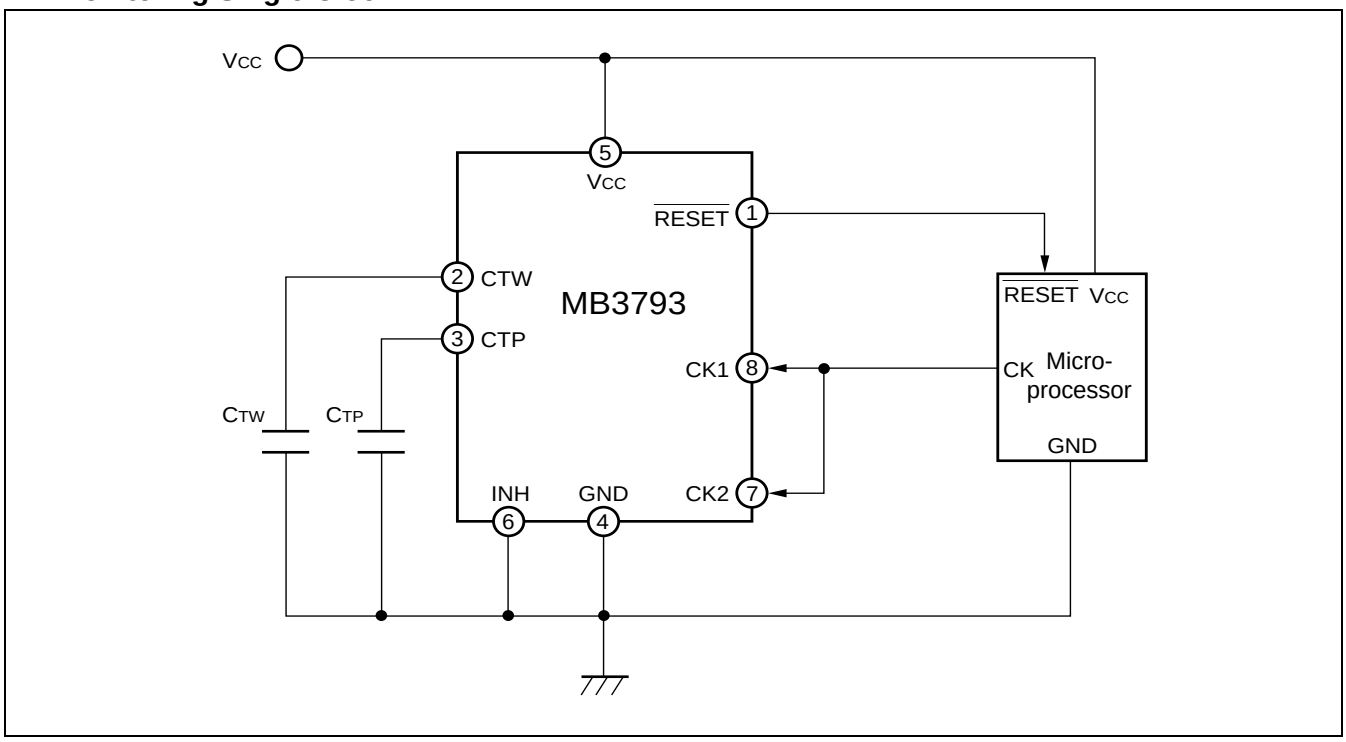
A	B	C	D	Remark
1300	1500	3	100	

(Example) When C_{TP} = 0.1 µF and C_{TW} = 0.01 µF,

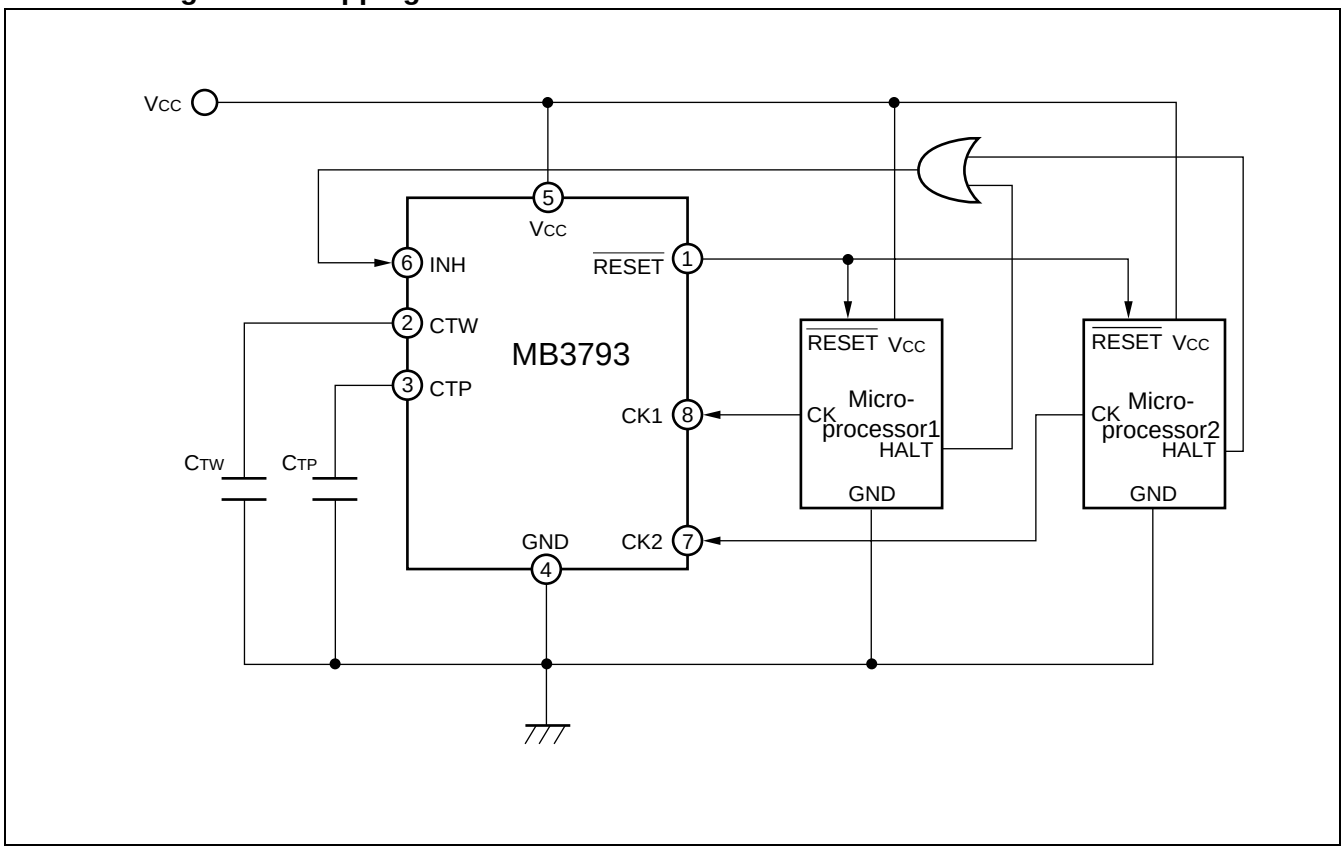
t_{PR} ≈ 130 [ms]
t_{WD} ≈ 15 [ms]
t_{WR} ≈ 10 [ms]

■ APPLICATION EXAMPLE

1. Monitoring Single Clock



2. Watchdog Timer Stopping

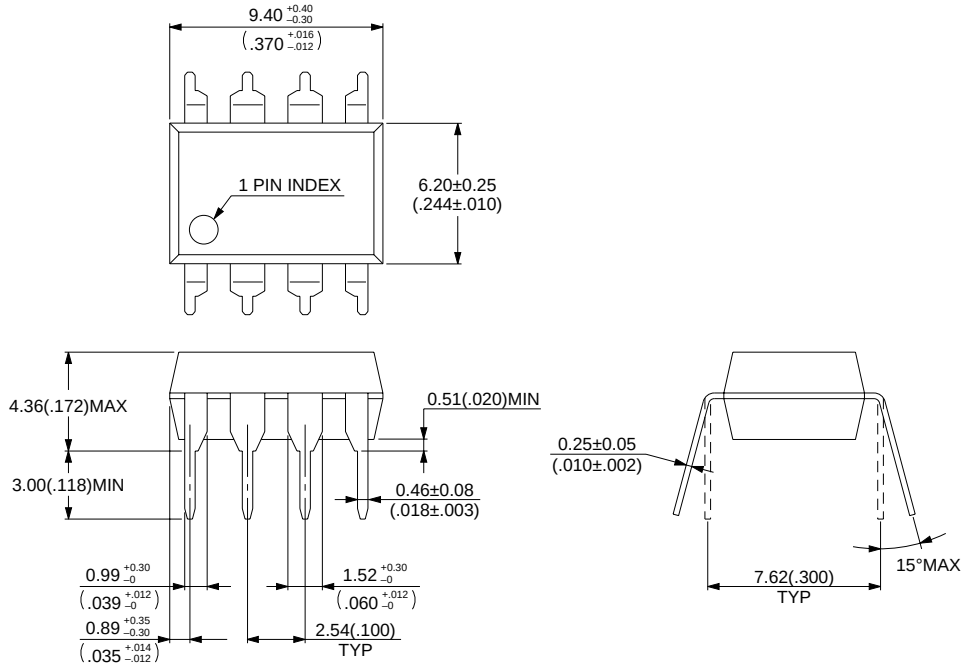


■ ORDERING INFORMATION

Part number	Package	Remarks
MB3793-42P	8-pin plastic DIP (DIP-8P-M01)	
MB3793-42PF	8-pin plastic SOP (FPT-8P-M01)	
MB3793-42PNF	8-pin plastic SOL (FPT-8P-M02)	

■ PACKAGE DIMENSIONS

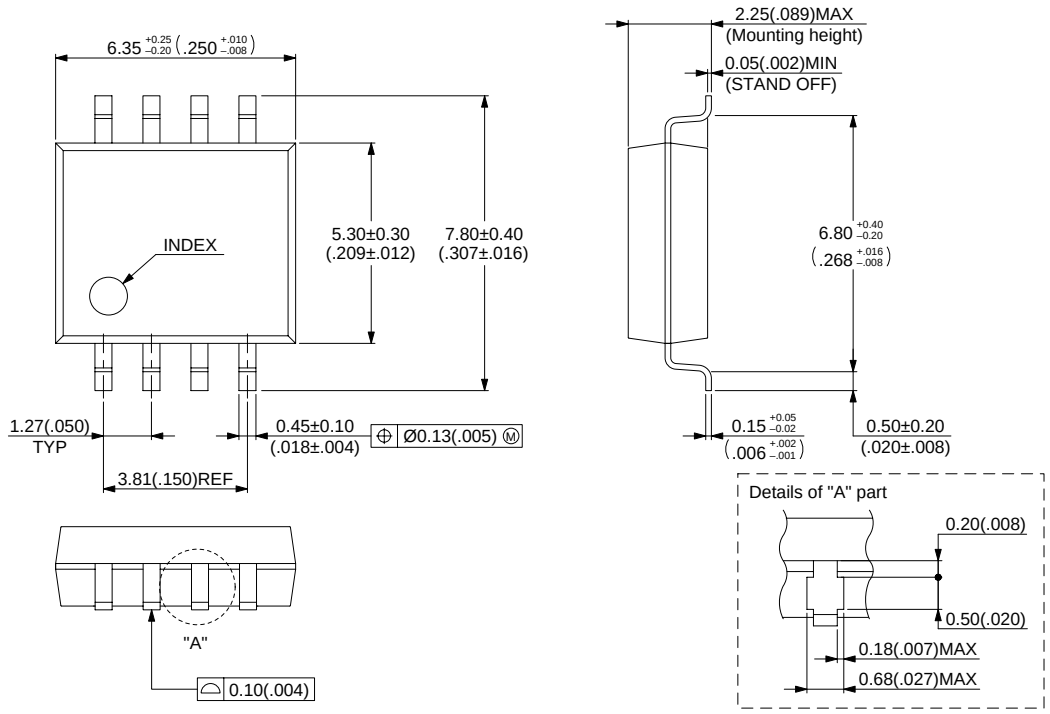
8-pin plastic DIP
(DIP-8P-M01)



Dimensions in mm (inches)

(Continued)

8-pin plastic SOP
(FPT-8P-M01)

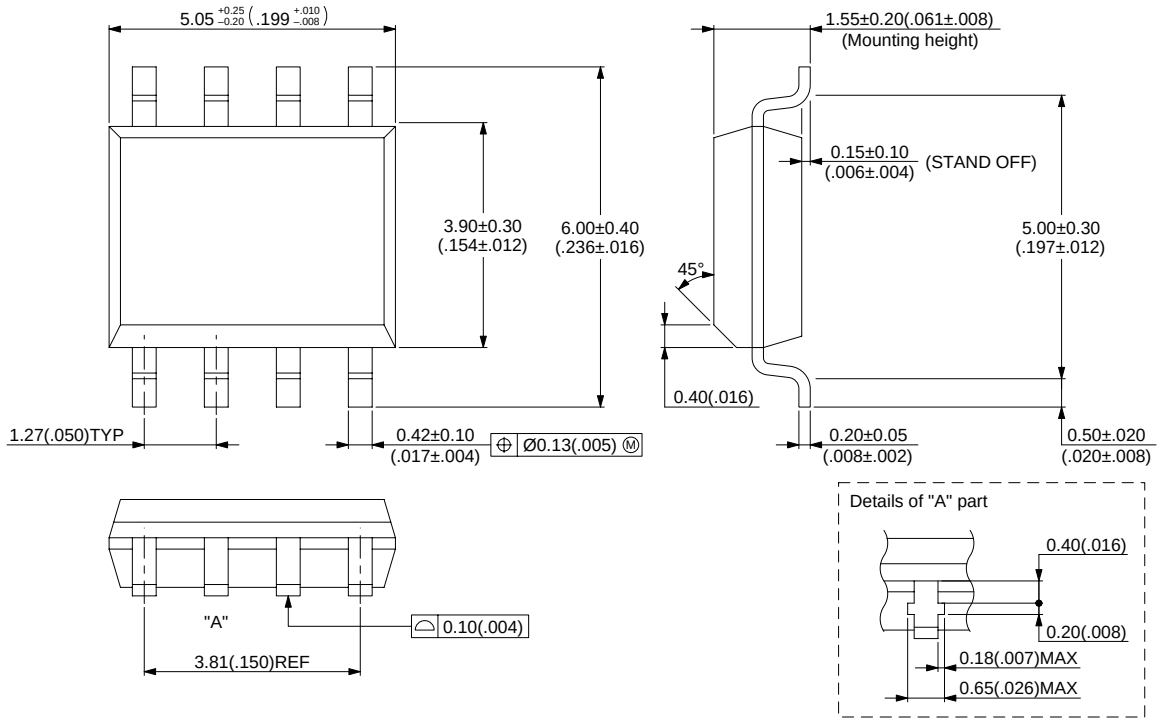


Dimensions in mm (inches)

(Continued)

(Continued)

8-pin plastic SOL
(FPT-8P-M02)



Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Marketing Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3353
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmal.fujitsu.com/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

F0106

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.