

## ASSP For Power Supply Applications (Secondary battery)

# DC/DC Converter IC for Charging Li-ion Battery

## MB3888

### ■ DESCRIPTION

The MB3888 is a DC/DC converter IC suitable for down-conversion, using pulse-width (PWM) charging and enabling output voltage to be set to any desired level from one cell to four cells.

The MB3888 provides a broad power supply voltage range and low standby current as well as high efficiency, making it ideal for use as a built-in charging device in products such as notebook PC.

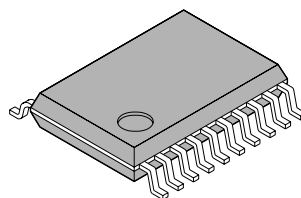
### ■ FEATURES

- Output voltage setting using external resistor : 1 cell to 4 cells
- High efficiency : 96% ( $V_{IN} = 19\text{ V}$ ,  $V_o = 16.8\text{ V}$ )
- Wide range of operating supply voltages : 8 V to 25 V
- Output voltage setting accuracy :  $5\text{ V} \pm 0.74\%$  ( $T_a = -10\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ )
- Charging current accuracy :  $\pm 5\%$

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### ■ PACKAGE

20-pin plastic SSOP

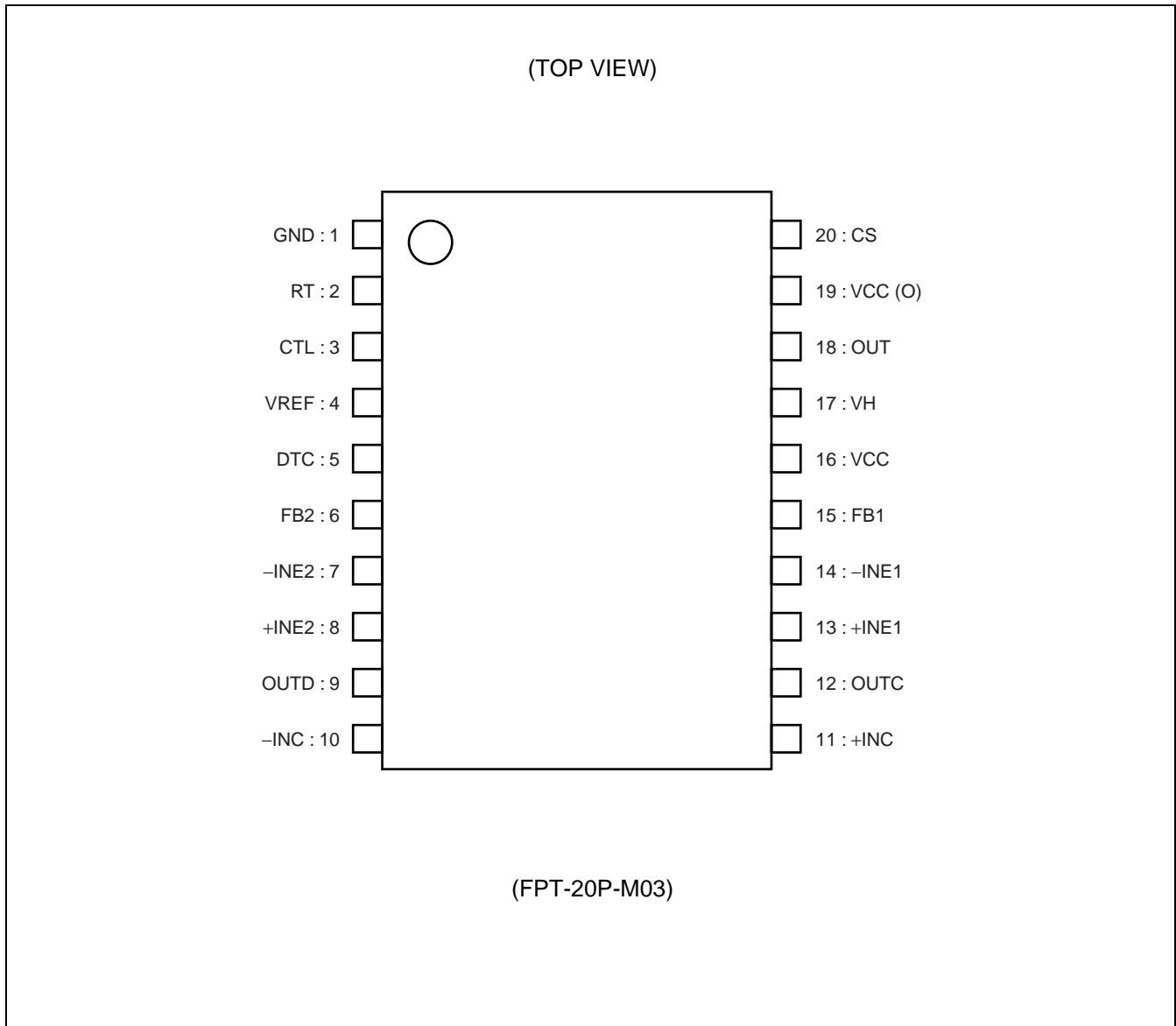


(FPT-20P-M03)

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- Built-in frequency setting capacitor enables frequency setting using external resistor only
- Oscillation frequency range : 100 kHz to 500 kHz
- Built-in current detection amplifier with wide in-phase input voltage range : 0 V to  $V_{CC}$
- In standby mode, leave output voltage setting resistor open to prevent inefficient current loss
- Built-in standby current function : 0  $\mu$ A (standard)
- Built-in soft-start function independent of loads
- Built-in totem-pole output stage supporting P-channel MOS FETs devices

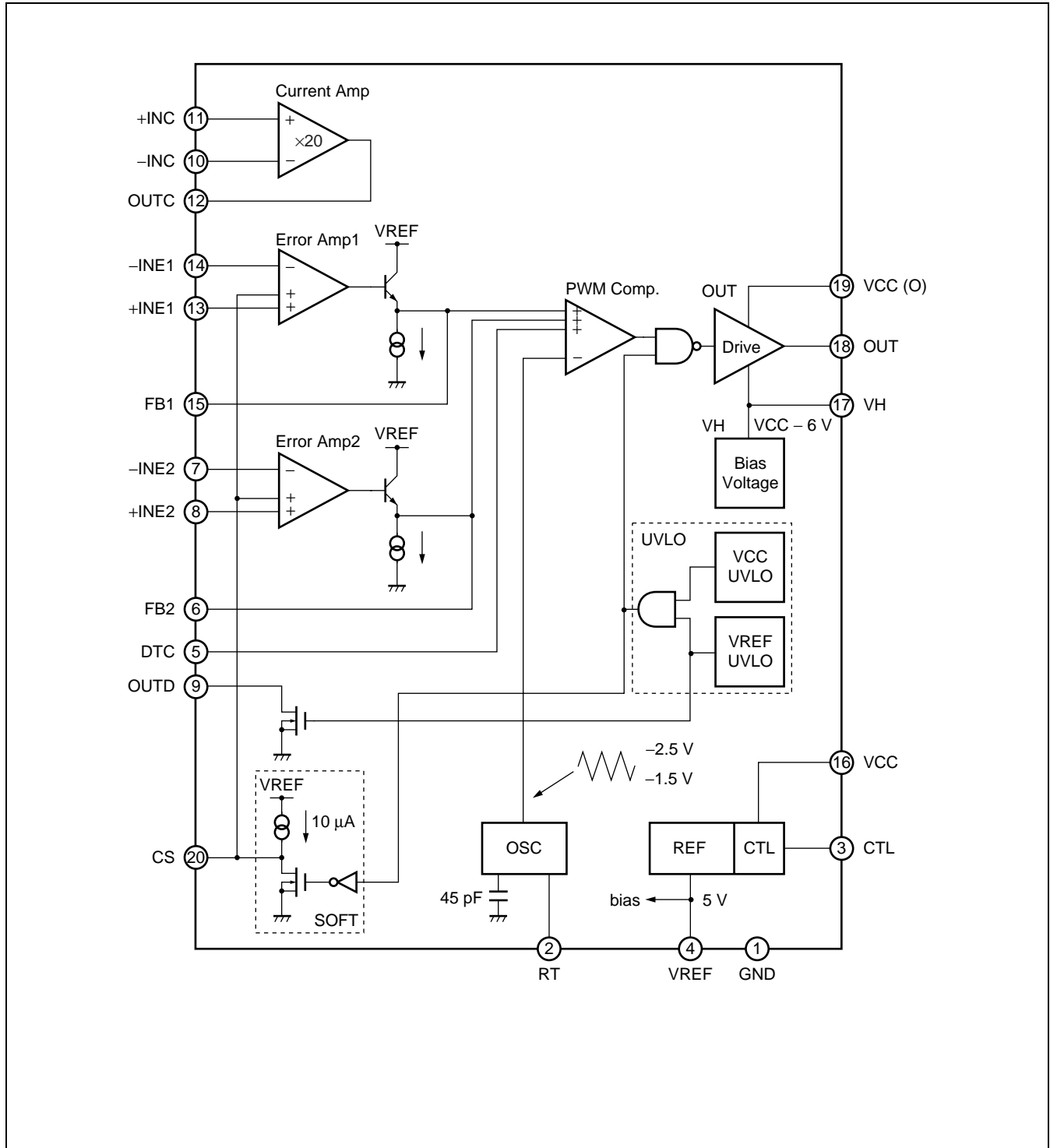
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	GND	—	Ground terminal.
2	RT	—	Triangular-wave oscillation frequency setting resistor connection terminal.
3	CTL	I	Power supply control terminal. Setting the CTL terminal at “L” level places the IC in the standby mode.
4	VREF	O	Reference voltage output terminal.
5	DTC	I	PWM comparator block (PWM) input terminal. Compares the lowest voltage among terminals FB1, FB2, and DTC, with triangular wave and controls output.
6	FB2	O	Error amplifier (Error Amp2) output terminal.
7	-INE2	I	Error amplifier (Error Amp2) inverted input terminal.
8	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal.
9	OUTD	O	With IC in standby mode, this terminal is set to “Hi-Z” to prevent loss of current through output voltage setting resistance. Set CTL terminal to “H” level and OUTD terminal to “L” level.
10	-INC	I	Current detection amplifier (Current Amp) input terminal.
11	+INC	I	Current detection amplifier (Current Amp) input terminal.
12	OUTC	O	Current detection amplifier (Current Amp) output terminal.
13	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal.
14	-INE1	I	Error amplifier (Error Amp1) inverted input terminal.
15	FB1	O	Error amplifier (Error Amp1) output terminal.
16	VCC	—	Power supply terminal for reference power supply and control circuit.
17	VH	O	Power supply terminal for FET drive circuit ( $VH = V_{CC} - 6 V$ ) .
18	OUT	O	External FET gate drive terminal.
19	VCC (O)	—	Output circuit power supply terminal.
20	CS	—	Soft-start capacitor connection terminal.

## ■ BLOCK DIAGRAM



# MB3888

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V <sub>CC</sub>	VCC, VCC (O) terminal	—	28	V
Output current	I <sub>OUT</sub>	—	—	60	mA
Peak output current	I <sub>OUT</sub>	Duty ≤ 5 % (t = 1 / f <sub>osc</sub> × Duty)	—	700	mA
Power dissipation	P <sub>D</sub>	T <sub>a</sub> ≤ +25 °C	—	540*	mW
Storage temperature	T <sub>STG</sub>	—	-55	+125	°C

\* : The package is mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Power supply voltage	V <sub>CC</sub>	VCC, VCC (O) terminal	8	—	25	V
Reference voltage output current	I <sub>REF</sub>	—	-1	—	0	mA
VH terminal output current	I <sub>VH</sub>	—	0	—	30	mA
Input voltage	V <sub>INE</sub>	-INE and +INE terminal	0	—	V <sub>CC</sub> - 1.8	V
	V <sub>INC</sub>	-INC and +INC terminal	0	—	V <sub>CC</sub>	V
	V <sub>DTC</sub>	DTC terminal	0	—	V <sub>CC</sub> - 0.9	V
OUTD terminal output voltage	V <sub>OUTD</sub>	—	0	—	17	V
OUTD terminal output current	I <sub>OUTD</sub>	—	0	—	2	mA
CTL terminal input voltage	V <sub>CTL</sub>	—	0	—	25	V
Output current	I <sub>OUT</sub>	—	-45	—	+45	mA
Peak output current	I <sub>OUT</sub>	Duty ≤ 5 % (t = 1 / f <sub>osc</sub> × Duty)	-600	—	+600	mA
Oscillation frequency	f <sub>osc</sub>	—	100	290	500	kHz
Timing resistor	R <sub>T</sub>	—	27	43	130	kΩ
Soft-start capacitor	C <sub>S</sub>	—	—	0.022	1.0	μF
VH terminal capacitor	C <sub>VH</sub>	—	—	0.1	1.0	μF
Reference voltage output capacitor	C <sub>REF</sub>	—	—	0.1	1.0	μF
Operating ambient temperature	T <sub>a</sub>	—	-30	+25	+85	°C

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter	Sym- bol	Pin No.	Conditions	Rating			Unit	
				Min	Typ	Max		
1. Reference voltage block [REF]	Output voltage	V <sub>REF</sub>	4	Ta = +25 °C	4.975	5.000	5.025	V
				Ta = -10 °C to +85 °C	4.963	5.000	5.037	V
	Input stability	Line	4	VCC = 8 V to 25 V	—	3	10	mV
	Load stability	Load	4	VREF = 0 mA to -1 mA	—	1	10	mV
	Short-circuit output current	I <sub>os</sub>	4	VREF = 1 V	-50	-25	-12	mA
2. Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V <sub>TLH</sub>	16	VCC = VCC (O) , VCC = $\sqrt{\phantom{x}}$	6.2	6.4	6.6	V
		V <sub>THL</sub>	16	VCC = VCC (O) , VCC = $\overline{\sqrt{\phantom{x}}}$	5.2	5.4	5.6	V
	Hysteresis width	V <sub>H</sub>	16	VCC = VCC (O)	—	1.0*	—	V
	Threshold voltage	V <sub>TLH</sub>	4	VREF = $\sqrt{\phantom{x}}$	2.6	2.8	3.0	V
		V <sub>THL</sub>	4	VREF = $\overline{\sqrt{\phantom{x}}}$	2.4	2.6	2.8	V
Hysteresis width	V <sub>H</sub>	4	—	—	0.2*	—	V	
3. Soft-start block [SOFT]	Charge current	I <sub>cs</sub>	20	—	-14	-10	-6	μA
4. Triangular waveform oscillator block [OSC]	Oscillation frequency	f <sub>osc</sub>	18	RT = 43 kΩ	260	290	320	kHz
	Frequency temperature stability	Δf/fdt	18	Ta = -30 °C to +85 °C	—	1*	—	%

\* : Standard design value.

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(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

Parameter		Symbol	Pin No.	Conditions	Rating			Unit
					Min	Typ	Max	
5-1. Error amplifier block [Error Amp1, Error Amp2]	Input offset voltage	V <sub>IO</sub>	7, 8, 13, 14	FB1 = FB2 = 2 V	—	1	5	mV
	Input bias current	I <sub>B</sub>	7, 8, 13, 14	—	-100	-30	—	nA
	Voltage gain	A <sub>V</sub>	6, 15	DC	—	100*	—	dB
	Frequency bandwidth	BW	6, 15	A <sub>V</sub> = 0 dB	—	2*	—	MHz
	Output voltage	V <sub>FBH</sub>	6, 15	—	4.7	4.9	—	V
		V <sub>FBL</sub>	6, 15	—	—	20	200	mV
	Output source current	I <sub>SOURCE</sub>	6, 15	FB1 = FB2 = 2 V	—	-2	-1	mA
	Output sink current	I <sub>SINK</sub>	6, 15	FB1 = FB2 = 2 V	150	300	—	μA
	OUTD terminal output leak current	I <sub>LEAK</sub>	9	OUTD = 17 V	—	0	1	μA
OUTD terminal output ON resistor	R <sub>ON</sub>	9	OUTD = 1 mA	—	35	50	Ω	
6. Current detection amplifier block [Current Amp]	Input offset current	V <sub>IO</sub>	10, 11	+INC = -INC = 3 V to V <sub>CC</sub>	-3	—	+3	mV
	Input current	I <sub>+INCH</sub>	11	+INC = 3 V to V <sub>CC</sub> , ΔV <sub>in</sub> = -100 mV	—	20	30	μA
		I <sub>-INCH</sub>	10	+INC = 3 V to V <sub>CC</sub> , ΔV <sub>in</sub> = -100 mV	—	0.1	0.2	μA
		I <sub>+INCL</sub>	11	+INC = 0 V, ΔV <sub>in</sub> = -100 mV	-180	-120	—	μA
		I <sub>-INCL</sub>	10	+INC = 0 V, ΔV <sub>in</sub> = -100 mV	-195	-130	—	μA
	Current detection voltage	V <sub>OUTC1</sub>	12	+INC = 3 V to V <sub>CC</sub> , ΔV <sub>in</sub> = -100 mV	1.9	2.0	2.1	V
		V <sub>OUTC2</sub>	12	+INC = 3 V to V <sub>CC</sub> , ΔV <sub>in</sub> = -20 mV	0.34	0.40	0.46	V
		V <sub>OUTC3</sub>	12	+INC = 0 V to 3 V, ΔV <sub>in</sub> = -100 mV	1.8	2.0	2.2	V
		V <sub>OUTC4</sub>	12	+INC = 0 V to 3 V, ΔV <sub>in</sub> = -20 mV	0.2	0.4	0.6	V
	In-phase input voltage range	V <sub>CM</sub>	10, 11	—	0	—	V <sub>CC</sub>	V
	Voltage gain	A <sub>V</sub>	12	+INC = 3 V to V <sub>CC</sub> , ΔV <sub>in</sub> = -100 mV	19	20	21	V/V

\* : Standard design value.

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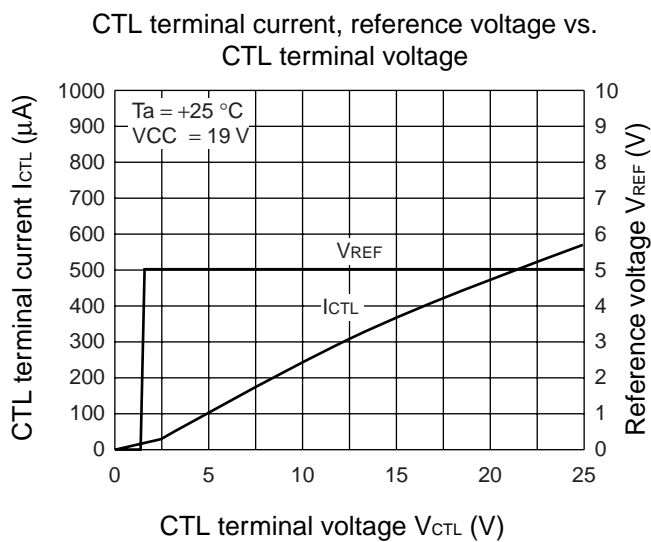
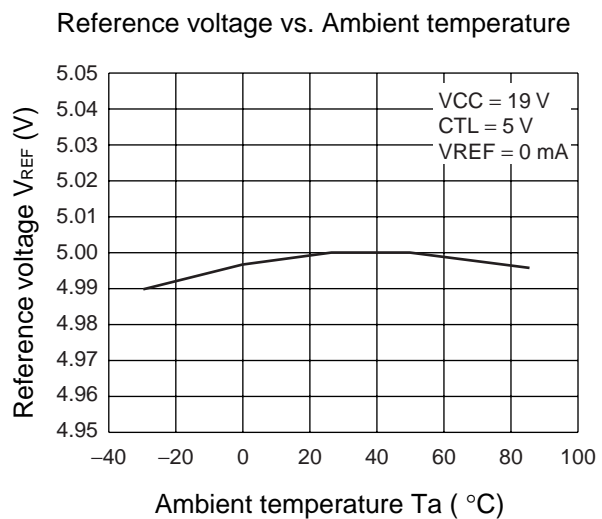
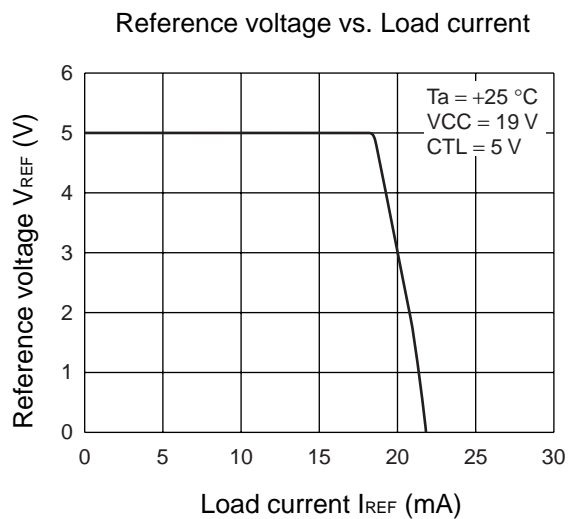
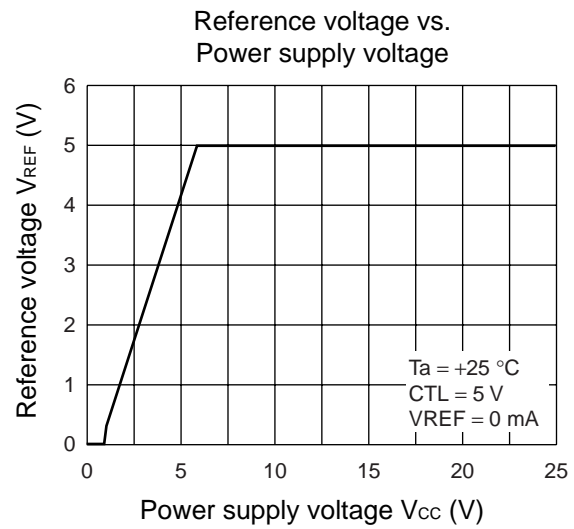
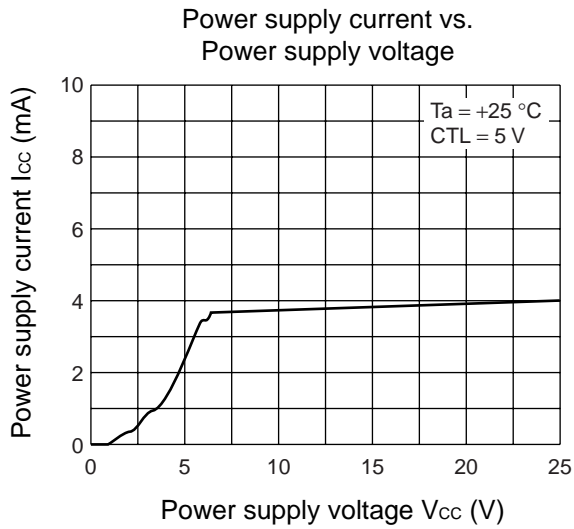
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(Ta = +25 °C, VCC = 19 V, VCC (O) = 19 V, VREF = 0 mA)

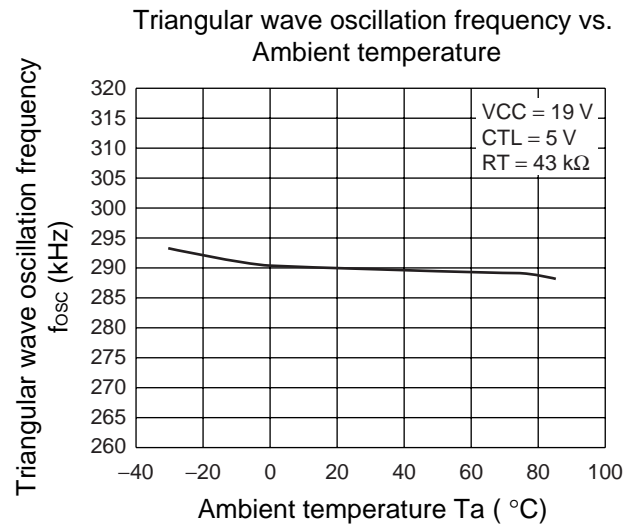
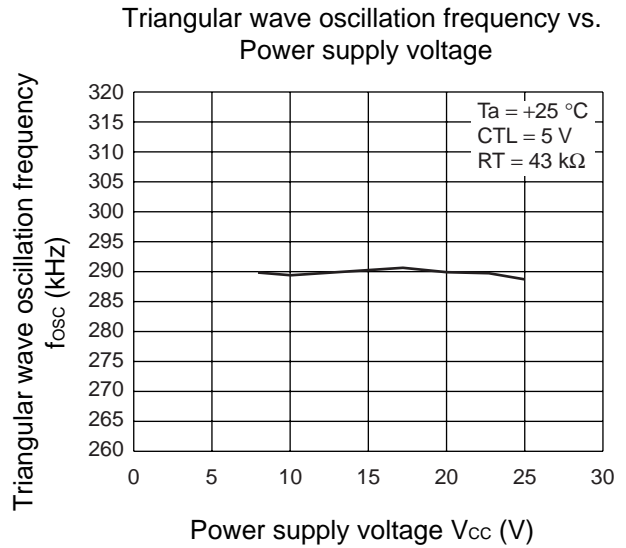
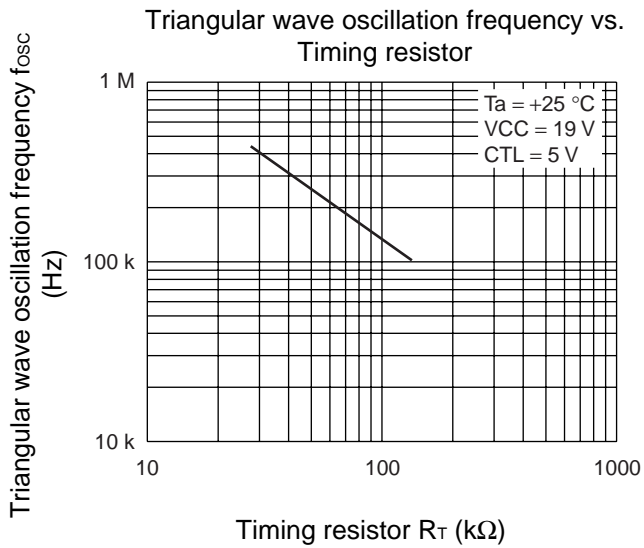
Parameter		Symbol	Pin No.	Conditions	Rating			Unit
					Min	Typ	Max	
6. Current detection amplifier block [Current Amp]	Frequency bandwidth	BW	12	$A_v = 0$ dB	—	2*	—	MHz
	Output voltage	$V_{OUTCH}$	12	—	4.7	4.9	—	V
		$V_{OUTCL}$	12	—	—	20	200	mV
	Output source current	$I_{SOURCE}$	12	OUTC = 2 V	—	-2	-1	mA
	Output sink current	$I_{SINK}$	12	OUTC = 2 V	150	300	—	$\mu$ A
7. PWM comparator block [PWM Comp.]	Threshold voltage	$V_{TL}$	5, 6, 15	Duty cycle = 0 %	1.4	1.5	—	V
		$V_{TH}$	5, 6, 15	Duty cycle = 100 %	—	2.5	2.6	V
	Input bias current	$I_{DTC}$	5	DTC = 0.4 V	-2.0	-0.6	—	$\mu$ A
8. Output block [OUT]	Output source current	$I_{SOURCE}$	18	OUT = 13 V, Duty $\leq$ 5 % ( $t = 1 / f_{osc} \times$ Duty)	—	-400*	—	mA
	Output sink current	$I_{SINK}$	18	OUT = 19 V, Duty $\leq$ 5 % ( $t = 1 / f_{osc} \times$ Duty)	—	400*	—	mA
	Output ON resistor	$R_{OH}$	18	OUT = -45 mA	—	6.5	9.8	$\Omega$
		$R_{OL}$	18	OUT = 45 mA	—	5.0	7.5	$\Omega$
	Rise time	$t_{r1}$	18	OUT = 3300 pF (equivalent to Si4435 $\times$ 1)	—	50*	—	ns
	Fall time	$t_{f1}$	18	OUT = 3300 pF (equivalent to Si4435 $\times$ 1)	—	50*	—	ns
9. Control block [CTL]	CTL input voltage	$V_{ON}$	3	IC Active mode	2	—	25	V
		$V_{OFF}$	3	IC Standby mode	0	—	0.8	V
	Input current	$I_{CTLH}$	3	CTL = 5 V	—	100	150	$\mu$ A
		$I_{CTLL}$	3	CTL = 0 V	—	0	1	$\mu$ A
10. Bias voltage block [VH]	Output voltage	$V_H$	17	$V_{CC} = V_{CC} (O)$ = 8 V to 25 V, $V_H = 0$ to 30 mA	$V_{CC} -$ 6.5	$V_{CC} -$ 6.0	$V_{CC} -$ 5.5	V
11. General	Standby current	$I_{CCS}$	16	$V_{CC} = V_{CC} (O)$ , CTL = 0 V	—	0	10	$\mu$ A
	Power supply current	$I_{CC}$	16	$V_{CC} = V_{CC} (O)$ , CTL = 5 V	—	4	6	mA

\* : Standard design value

## ■ TYPICAL CHARACTERISTICS



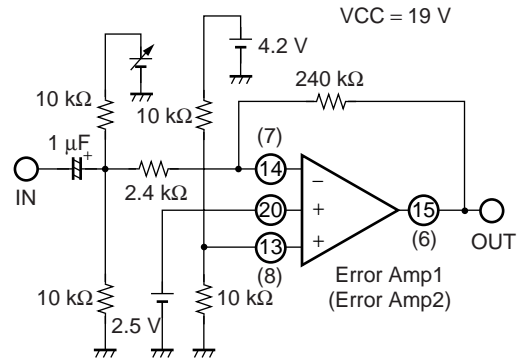
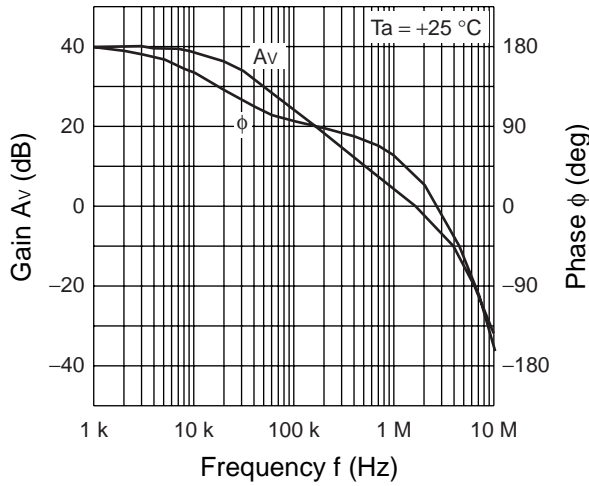
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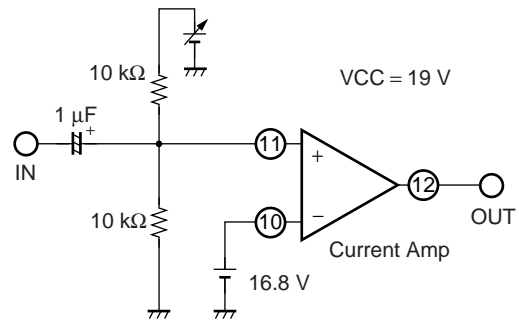
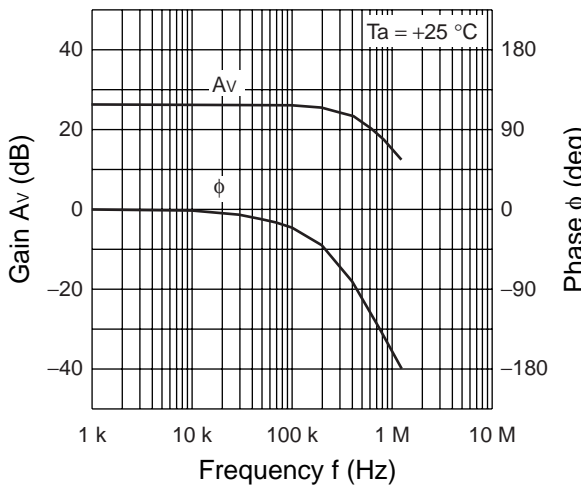
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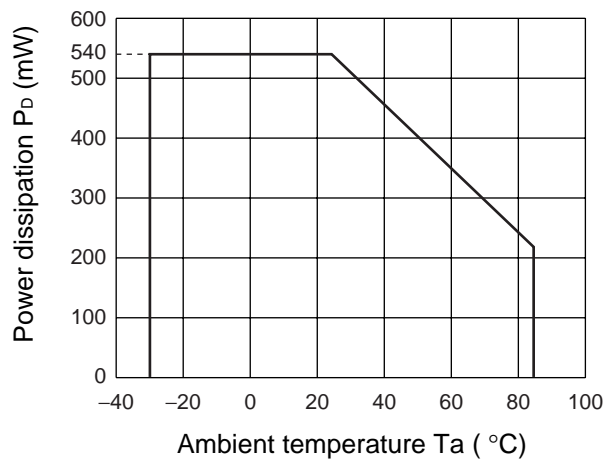
Error amplifier gain and phase vs. Frequency



Current detection amplifier and phase vs. Frequency



Power dissipation vs. Ambient temperature



## ■ FUNCTIONAL DESCRIPTION

### 1. DC/DC Converter Unit

#### (1) Reference voltage block (REF)

The reference voltage generator uses the voltage supplied from the VCC terminal (pin 16) to generate a temperature-compensated, stable voltage (5.0 V Typ) used as the reference supply voltage for the IC's internal circuitry.

This terminal can also be used to obtain a load current to a maximum of 1 mA from the reference voltage VREF terminal (pin 4) .

#### (2) Triangular wave oscillator block (OSC)

The triangular wave oscillator builds the capacitor for frequency setting into, and generates the triangular wave oscillation waveform by connecting the frequency setting resistor with the RT terminal (pin 2) .

The triangular wave is input to the PWM comparator on the IC.

#### (3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current amp1) , compares this to the +INE1 terminal (pin 13) , and outputs a PWM control signal to be used in controlling the charging current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB1 terminal (pin 15) and -INE1 terminal (pin 14) , providing stable phase compensation to the system.

Connecting a soft-start capacitor to the CS terminal (pin 20) prevents rush currents when the IC is turned on.

Using an error amplifier for soft start detection makes the soft start time constant, independent of the output load.

#### (4) Error amplifier block (Error Amp2)

This amplifier (Error Amp2) detects the output voltage from the DC/DC converter and outputs the PWM control signal. External output voltage setting resistors can be connected to the error amplifier inverse input terminal to set the desired level of output voltage from 1 cell to 4 cells.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB2 terminal (pin 6) to the -INE2 terminal (pin 7) of the error amplifier, enabling stable phase compensation to the system.

Connecting a soft-start capacitor to the CS terminal (pin 20) prevents rush currents when the IC is turned on.

Using an error amplifier for soft-start detection makes the soft-start time constant, independent of the output load.

#### (5) Current detector amplifier block (Current Amp)

The current detection amplifier (Current Amp) detects a voltage drop which occurs between both ends of the output sense resistor ( $R_s$ ) due to the flow of the charge current, using the +INC terminal (pin 11) and -INC terminal (pin 10) . Then it outputs the signal amplified by 20 times to the error amplifier (Error Amp1) at the next stage.

#### (6) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1 and Error Amp2) and DTC terminal (pin 5) depending on their output voltage.

The PWM comparator circuit compares the triangular wave generated by the triangular wave oscillator to the error amplifier output voltage or DTC terminal voltage, and turns on the external output transistor during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

## (7) Output block (OUT)

The output circuit uses a totem-pole configuration capable of driving an external P-channel MOS FET.

The output “L” level sets the output amplitude to 6 V (Typ) using the voltage generated by the bias voltage block (VH) .

This results in increasing conversion efficiency and suppressing the withstand voltage of the connected external transistor in a wide range of input voltages.

## (8) Control block (CTL)

Setting the CTL terminal (pin 3) at “L” level places the IC in the standby mode. (The supply current is 10  $\mu$ A at maximum in the standby mode.) Setting the CTL terminal at “H” level generates an internal reference voltage, placing the system under outputting status.

**CTL function table**

CTL	Power	OUTD
L	OFF (Standby)	Hi-Z
H	ON (Active)	L

## (9) Bias voltage block (VH)

The bias voltage circuit outputs  $V_{cc} - 6$  V (Typ) as the minimum potential of the output circuit. In the standby mode, this circuit outputs the potential equal to  $V_{cc}$ .

## 2. Protection Functions

### Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage or internal reference voltage (VREF) , which occurs when the power supply (VCC) is turned on, may cause malfunctions in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects a supply voltage or internal reference voltage drop and fixes the OUT terminal (pin 18) to the “H” level. The system restores voltage supply when the supply voltage or internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

### Protection function (UVLO) operation table

When UVLO is operating (VCC or VREF voltage is lower than UVLO threshold voltage) .

OUTD	OUT	CS
Hi-Z	H	L

## 3. Soft-Start Function

### Soft-start block (SOFT)

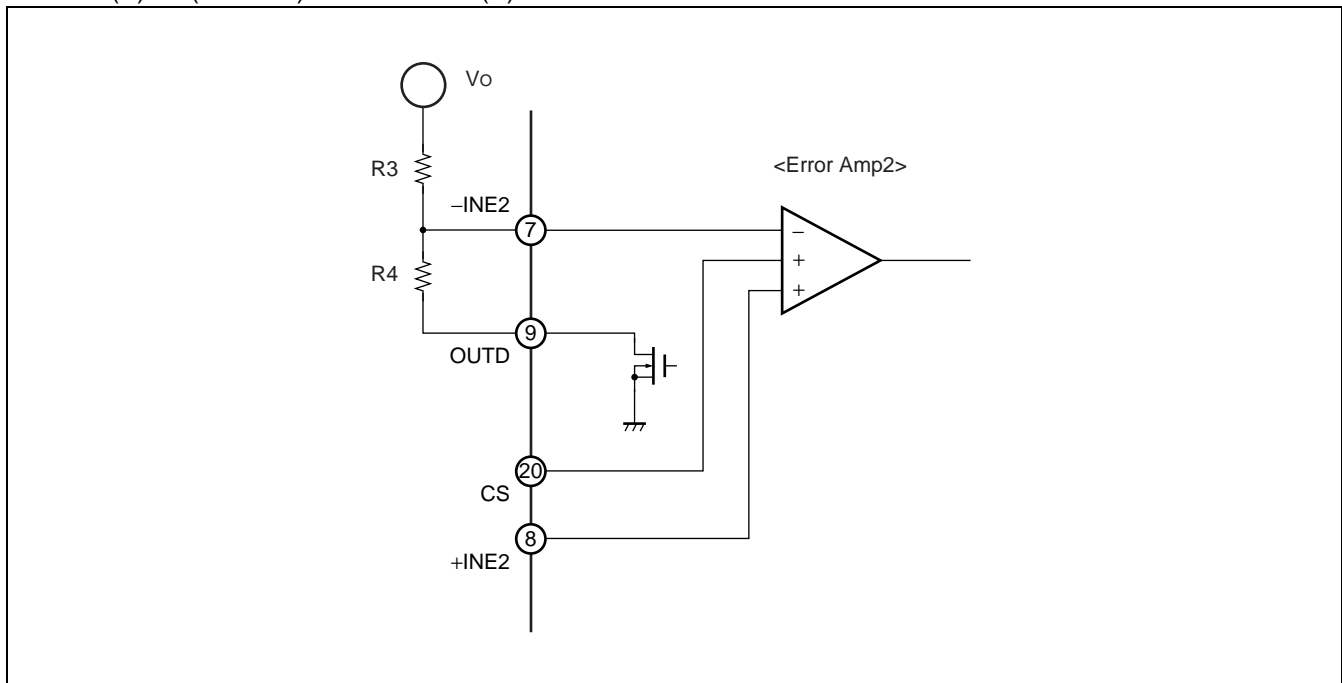
Connecting a capacitor to the CS terminal (pin 20) prevents surge currents when the IC is turned on. Using an error amplifier for soft-start detection makes the soft-start time constant, being independent of the output load of the DC/DC converter.

## ■ SETTING THE CHARGING VOLTAGE

The charging voltage (DC/DC output voltage) can be set by connecting external voltage setting resistors (R3, R4) to the -INE2 terminal (pin 7) according to the voltage at the +INE2 terminal (pin 8). Be sure to select a resistor value that allows you to ignore the on resistor (35 Ω, 1 mA) of the internal FET connected to the OUTD terminal (pin 9). In standby mode, the charging voltage is applied to OUTD terminal. Therefore, output voltage must be adjusted so that voltage applied to OUTD terminal is 17 V or less.

Battery charging voltage :  $V_o$

$$V_o (V) = (R3 + R4) / R4 \times +INE2 (V)$$



## ■ METHOD OF SETTING THE CHARGING CURRENT

The charge current (output limit current) value can be set with the voltage at the +INE1 terminal (pin 13).

If a current exceeding the set value attempts to flow, the charge voltage drops according to the set current value.

Battery charge current setting voltage : +INE1

$$+INE1 (V) = 20 \times I1 (A) \times R_s (\Omega)$$

## ■ METHOD OF SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor ( $R_T$ ) connected the RT terminal (pin 2).

Triangular wave oscillation frequency :  $f_{osc}$

$$f_{osc} (kHz) \approx 12690 / R_T (k\Omega)$$



## ■ METHOD OF SETTING THE SOFT-START TIME

### (1) Setting constant voltage mode soft-start

For preventing rush current upon activation of IC, the IC allows soft-start using the capacitor ( $C_s$ ) connected to the CS terminal (pin 20) .

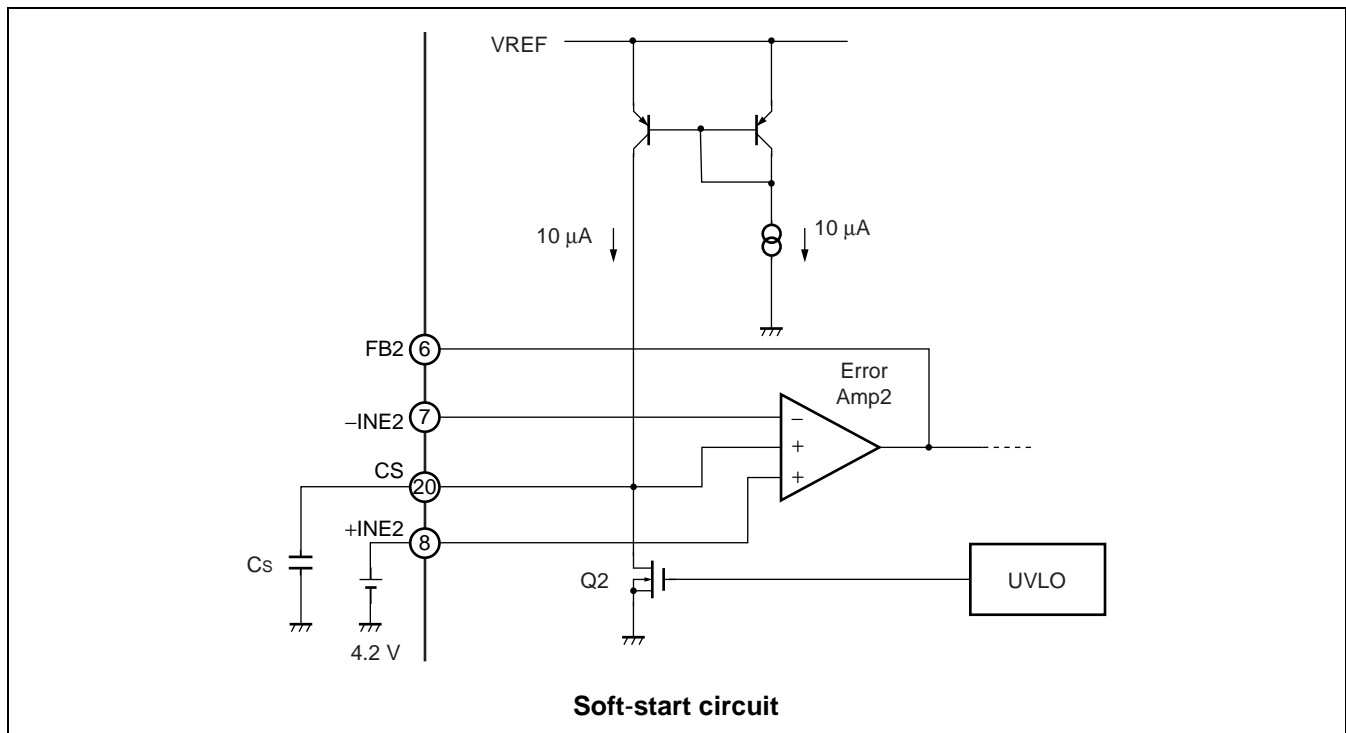
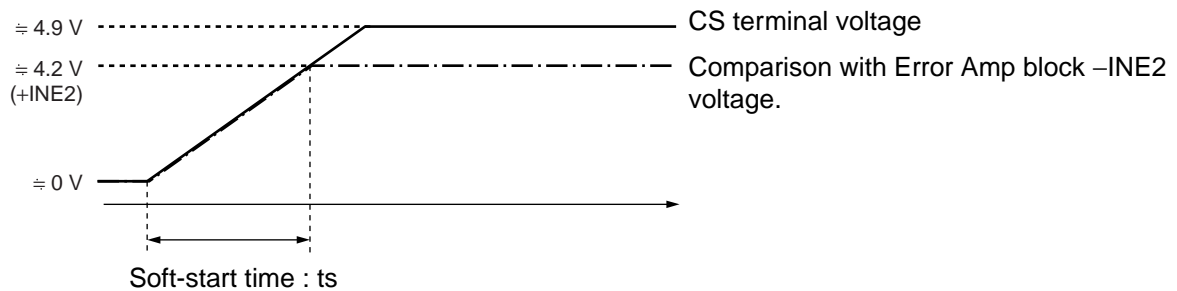
When CTL terminal (pin 3) is placed under “H” level and IC is activated ( $V_{CC} \geq UVLO$  threshold voltage) , Q2 is turned off and the external soft-start capacitor ( $C_s$ ) connected to the CS terminal is charged at  $10 \mu A$ .

Error Amp output (FB2 terminal (pin 6) ) is determined by comparison between the lower voltage of the two non-inverted input terminals (+INE2 terminal (pin 8) and CS terminal voltage) and inverted input terminal voltage (-INE2 terminal (pin 7) voltage) . Within the soft-start period (CS terminal voltage  $<$  +INE2) , FB2 is determined by comparison between -INE2 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.

Soft-start time is obtained from the following formula :

Soft-start time :  $t_s$  (time to output 100 %)

$$t_s (s) \approx 0.42 \times C_s (\mu F) , \text{ at } +INE2 = 4.2 V$$



## (2) Setting constant current mode soft-start

For preventing rush current upon activation of IC, the IC allows soft start using the capacitor ( $C_s$ ) connected to the CS terminal (pin 20) .

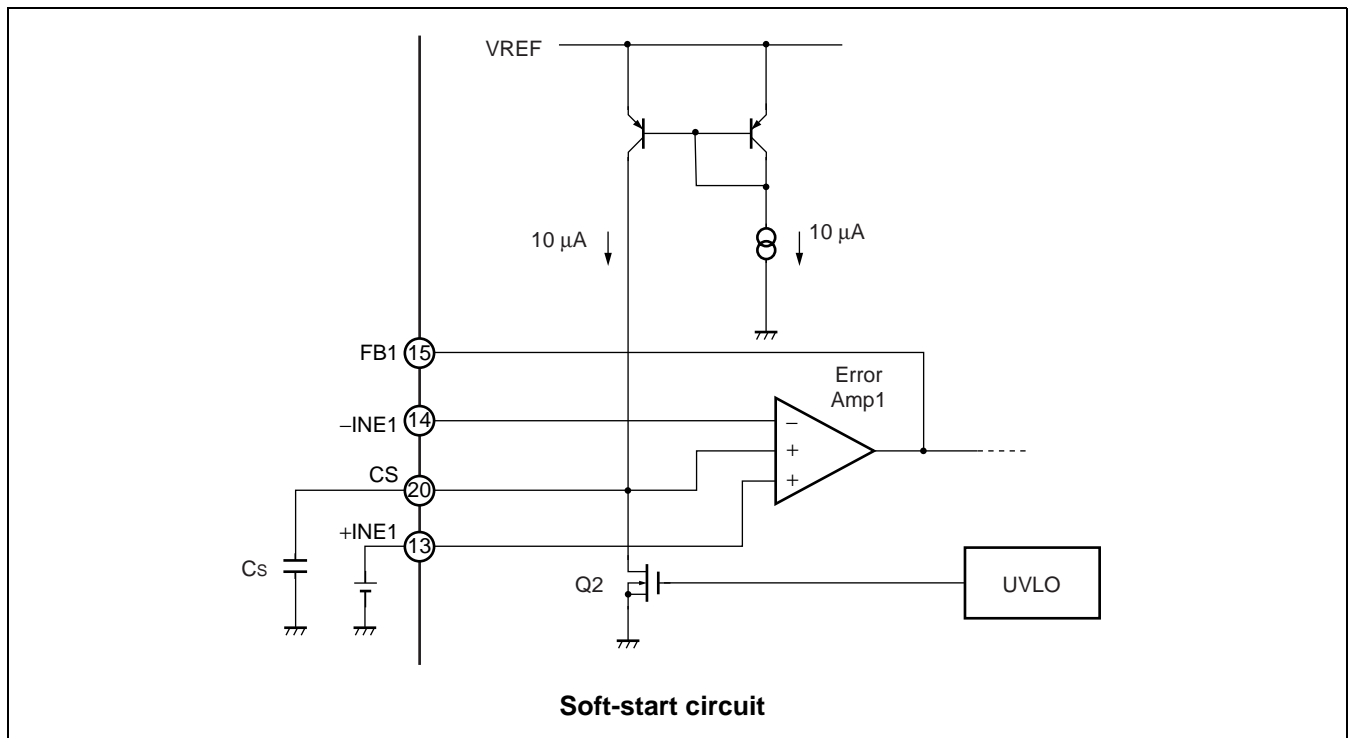
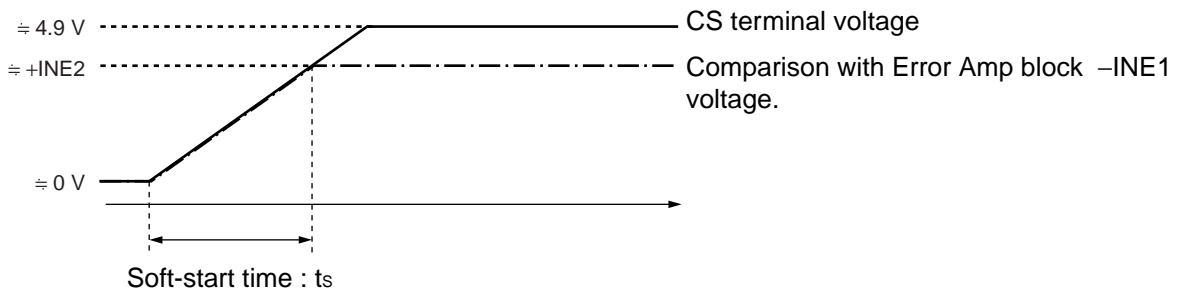
When CTL terminal (pin 3) is placed under “H” level and IC is activated ( $V_{CC} \geq UVLO$  threshold voltage) , Q2 is turned off and the external soft-start capacitor ( $C_s$ ) connected to the CS terminal is charged at  $10 \mu A$ .

Error Amp output (FB1 terminal (pin 15) ) is determined by comparison between the lower voltage of the two non-inverted input terminals (+INE1 terminal (pin 13) and CS terminal voltage) and inverted input terminal voltage (-INE1 terminal (pin 14) voltage) . Within the soft start period (CS terminal voltage  $<$  +INE1) , FB1 is determined by comparison between -INE1 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.

Soft-start time is obtained from the following formula :

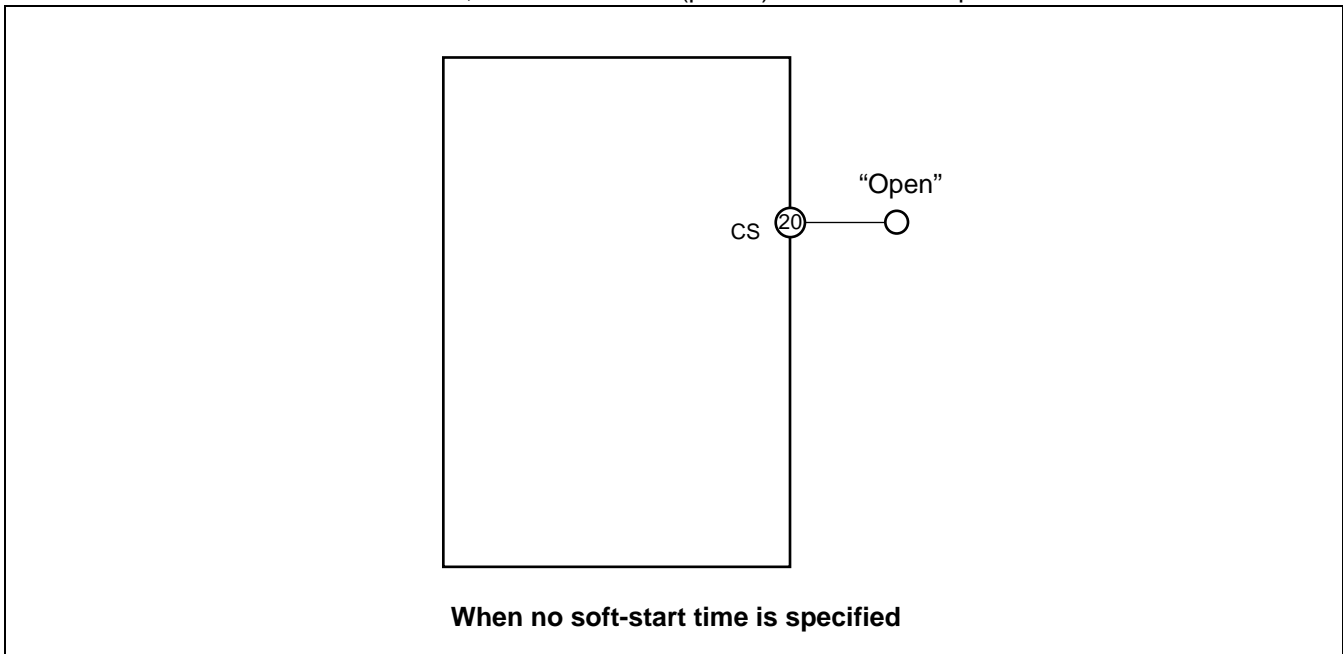
Soft-start time :  $t_s$  (time to output 100 %)

$$t_s (s) \approx +INE2 / 10 (\mu A) \times C_s (\mu F)$$



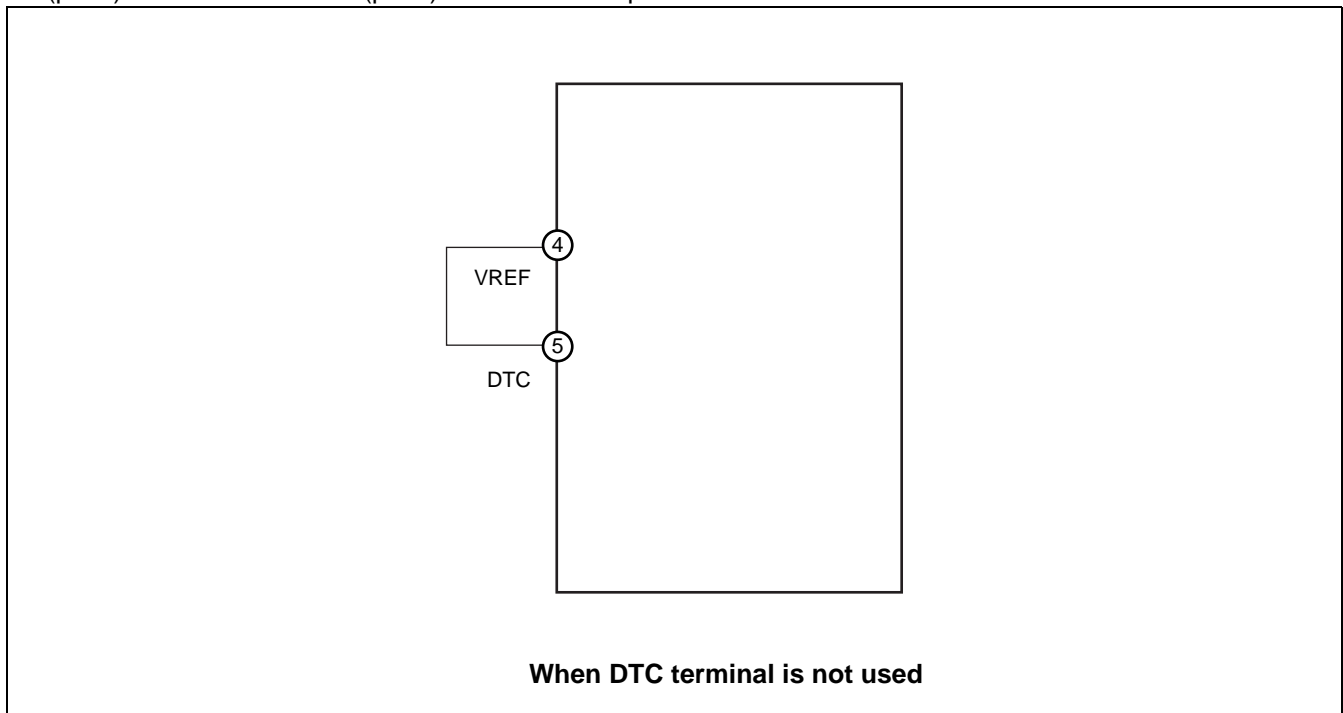
## ■ PROCESSING WITHOUT USING OF THE CS TERMINAL

When soft-start function is not used, the CS terminal (pin 20) should be left open.



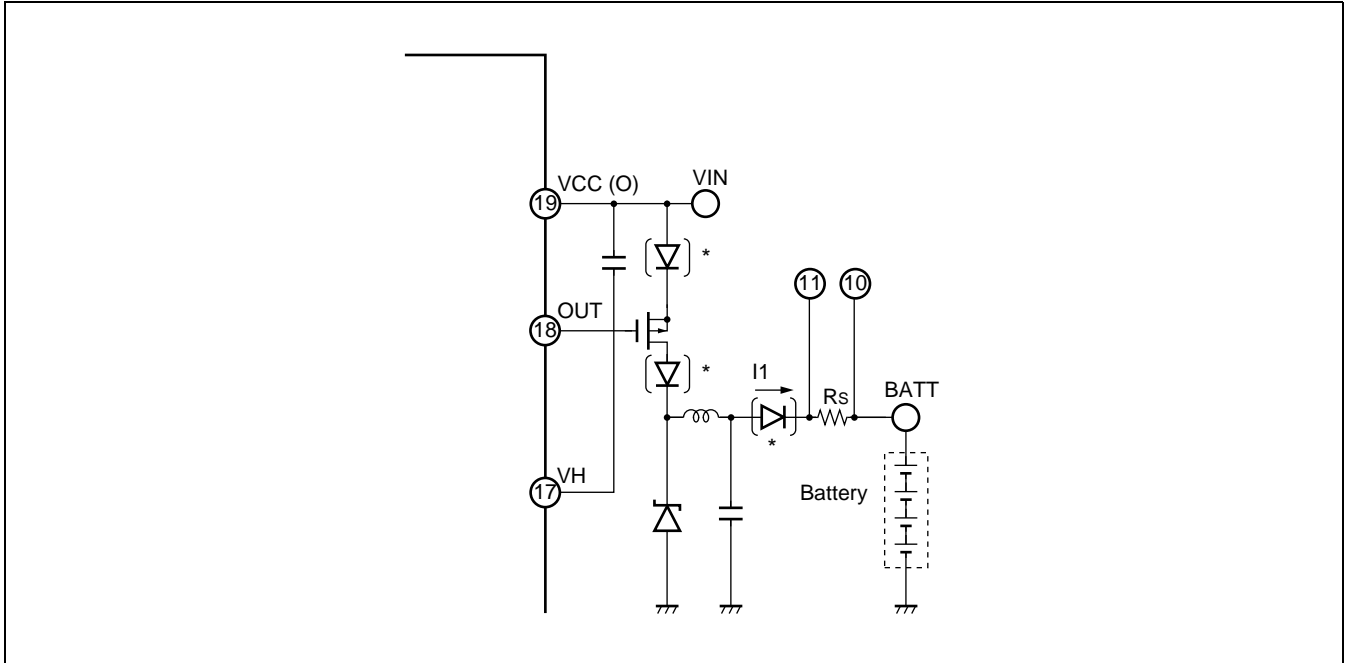
## ■ PROCESSING WITHOUT USING OF THE DTC TERMINAL

When external duty control is not performed using DTC terminal, make a short circuit between the DTC terminal (pin 5) and VREF terminal (pin 4) with a shortest-possible wire.



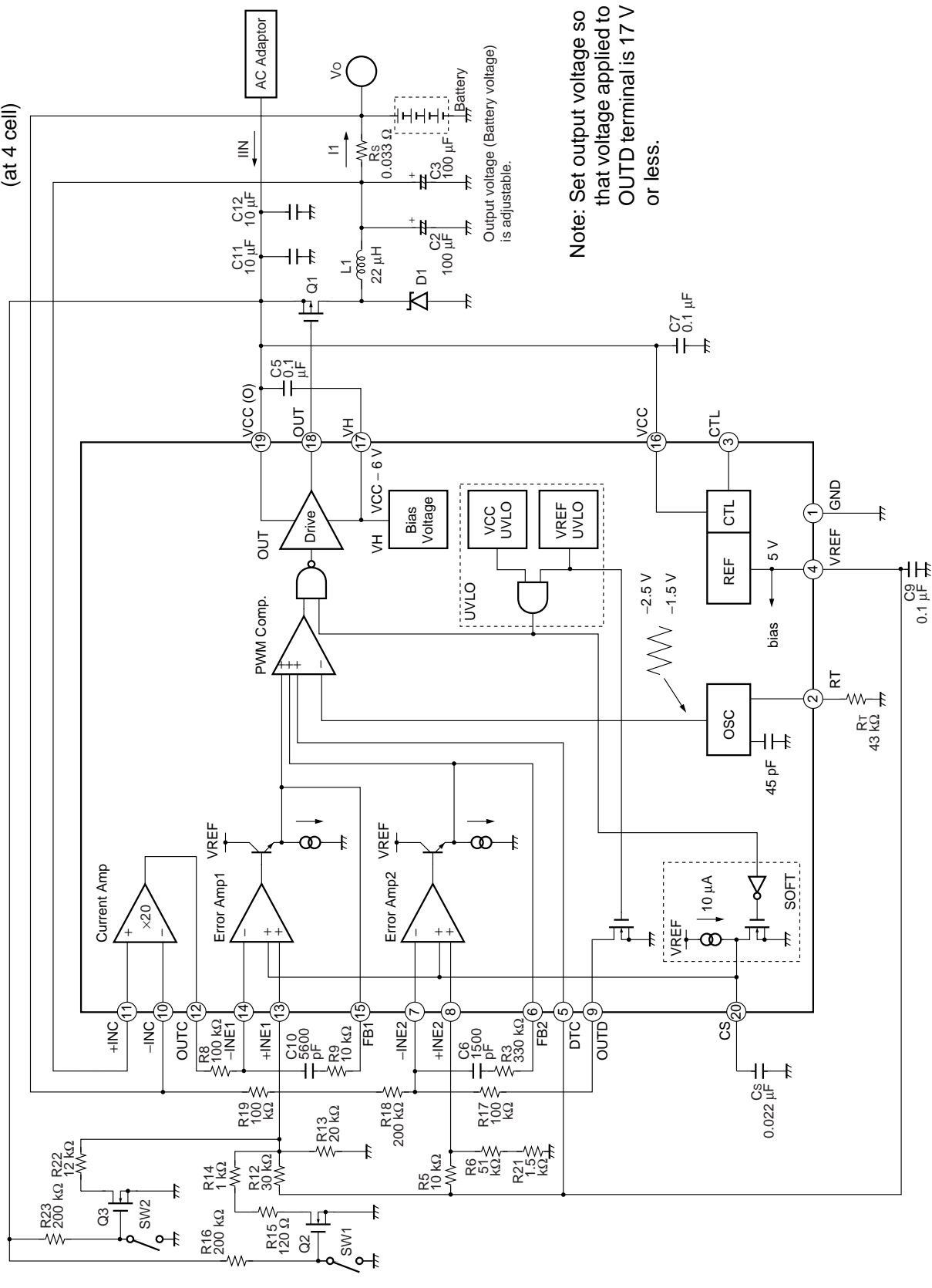
## ■ NOTE ON AN EXTERNAL REVERSE-CURRENT PREVENTIVE DIODE

- Insert a reverse-current preventive diode at one of the three locations marked \* to prevent reverse current from the battery.
- When selecting the reverse current prevention diode, be sure to consider the reverse voltage ( $V_R$ ) and reverse current ( $I_R$ ) of the diode.



## APPLICATION EXAMPLE

VIN = 13.6 V to 25 V  
(at 3 cell)  
VIN = 17.8 V to 25 V  
(at 4 cell)



Output voltage (Battery voltage) is adjustable.

Note: Set output voltage so that voltage applied to OUTD terminal is 17 V or less.

## ■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1	P-ch FET	VDS = -30 V, ID = ±8 A (Max)		VISHAY SILICONIX	Si4435DY
Q2	N-ch FET	VDS = 60 V, ID = 0.115 A (Max)		VISHAY SILICONIX	2N7002E
D1	Diode	VF = 0.42 V (Max) , at IF = 3 A		ROHM	RB053L-30
L1	Inductor	22 μH	3.5 A, 31.6 mΩ	TDK	SLF12565T-220M3R5
C2, C3	Electrolytic condenser	100 μF	25 V (10 %)	SANYO	25CV100AX
Cs	Ceramics Condenser	0.022 μF	50 V	TDK	C1608JB1H223K
C5	Ceramics Condenser	0.1 μF	50 V	TDK	C1608JB1H104K
C6	Ceramics Condenser	1500 pF	10 V	MURATA	GRM39B152K10
C7	Ceramics Condenser	0.1 μF	50 V	TDK	C1608JB1H104K
C9	Ceramics Condenser	0.1 μF	50 V	TDK	C1608JB1H104K
C10	Ceramics Condenser	5600 pF	10 V	MURATA	GRM39B562K10
C11, C12	Ceramics Condenser	10 μF	25 V	TDK	C3225JF1E106Z
Rs	Resistor	0.033 Ω	1.0 %	SEIDEN TECHNO	SRS1R033F
Rr	Resistor	43 kΩ	0.5 %	ssm	RR0816P433D
R3	Resistor	330 kΩ	0.5 %	ssm	RR0816P334D
R5	Resistor	10 kΩ	0.5 %	ssm	RR0816P103D
R6	Resistor	51 kΩ	0.5 %	ssm	RR0816P513D
R8	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R9	Resistor	10 kΩ	0.5 %	ssm	RR0816P103D
R12	Resistor	30 kΩ	0.5 %	ssm	RR0816P303D
R13	Resistor	20 kΩ	0.5 %	ssm	RR0816P203D
R14	Resistor	1 kΩ	0.5 %	ssm	RR0816P102D
R15	Resistor	120 Ω	0.5 %	ssm	RR0816P121D
R16, R18, R23	Resistor	200 kΩ	0.5 %	ssm	RR0816P204D
R17, R19	Resistor	100 kΩ	0.5 %	ssm	RR0816P104D
R21	Resistor	1.5 kΩ	0.5 %	ssm	RR0816P152D
R22	Resistor	12 kΩ	0.5 %	ssm	RR0816P123D

Note : VISHAY SILICONIX : VISHAY Intertechnology, Inc.

ROHM : ROHM CO., LTD.

TDK : TDK Corporation

SANYO : SANYO Electric Co., Ltd.

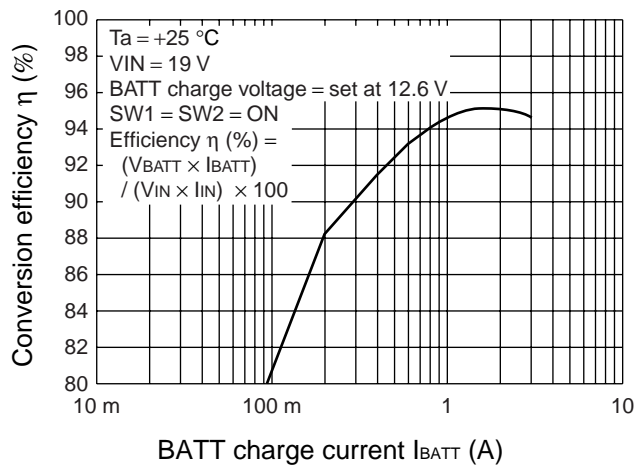
SEIDEN TECHNO : SEIDEN TECHNO CO., LTD.

MURATA : Murata Manufacturing Co., Ltd.

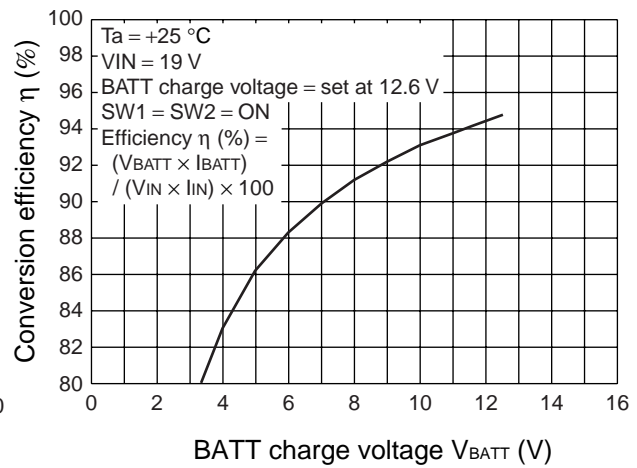
ssm : SUSUMU Co., Ltd.

## REFERENCE DATA

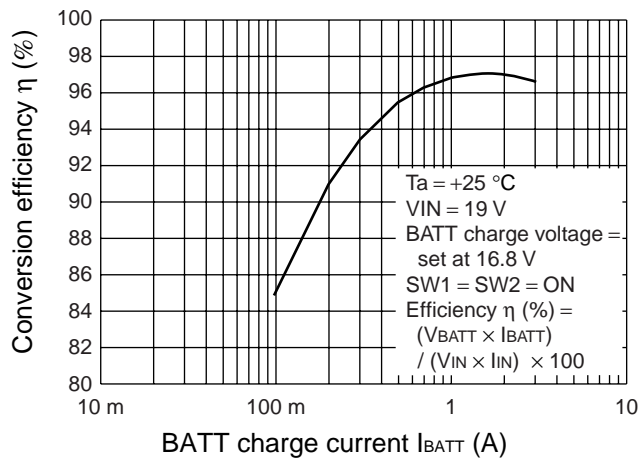
Conversion efficiency vs. Charge current  
(Constant voltage mode)



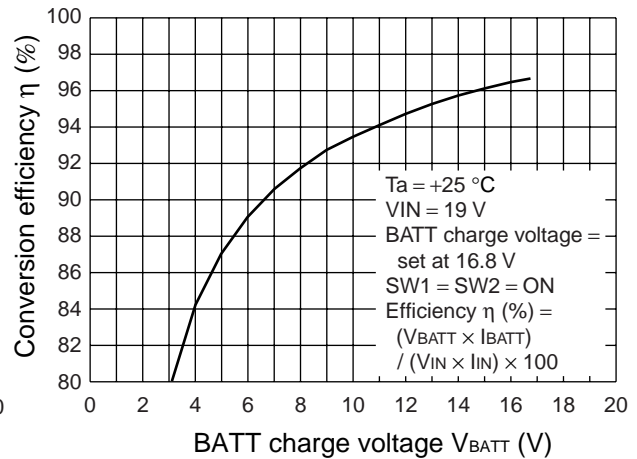
Conversion efficiency vs. Charge current  
(Constant current mode)



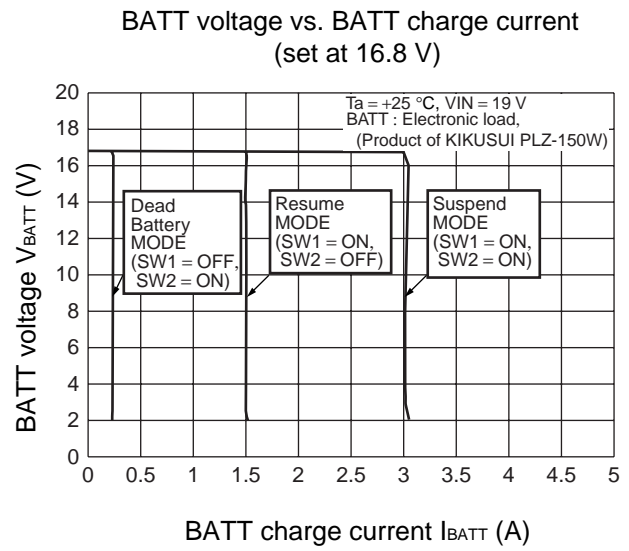
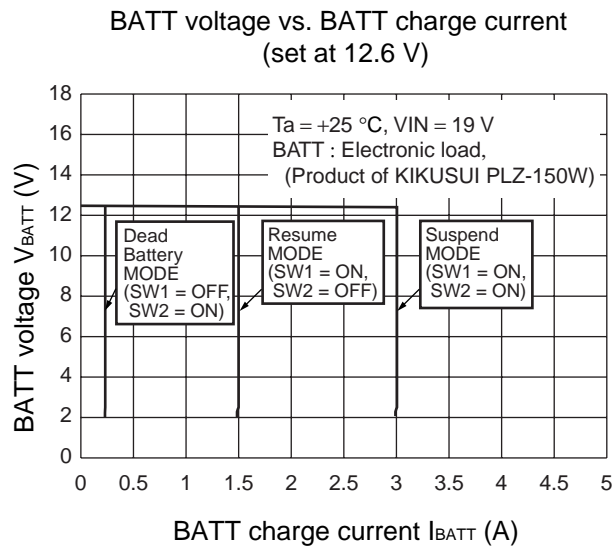
Conversion efficiency vs. Charge current  
(Constant voltage mode)



Conversion efficiency vs. Charge current  
(Constant current mode)



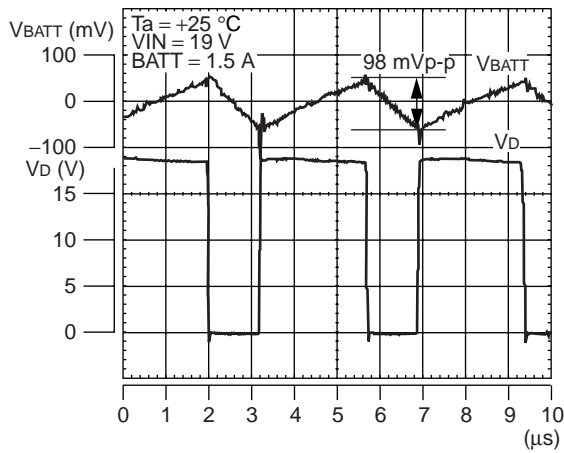
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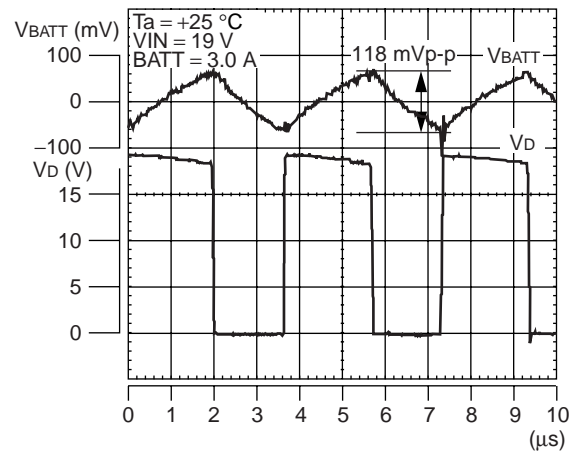
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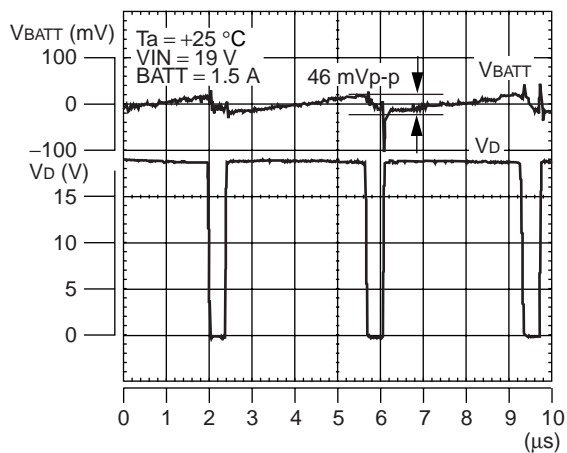
Switching waveform constant voltage mode  
(set at 12.6 V)



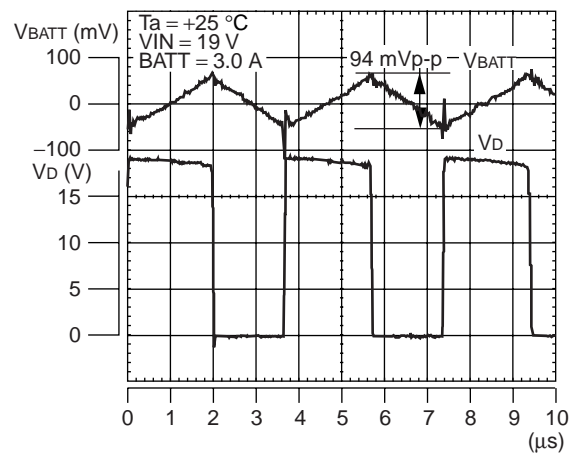
Switching waveform constant current mode  
(set at 12.6 V, with 10 V)



Switching waveform constant voltage mode  
(set at 16.8 V)

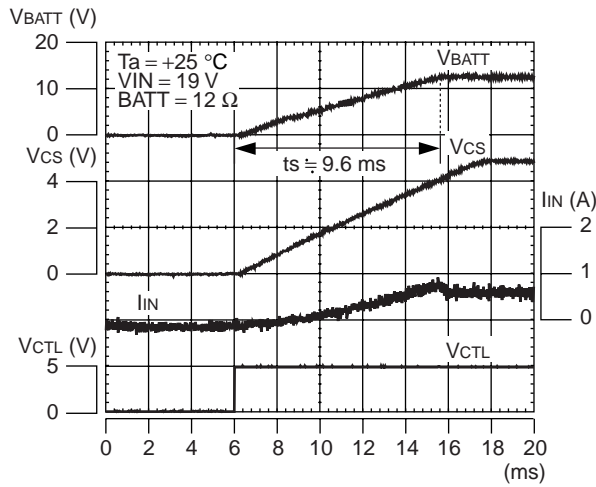


Switching waveform constant current mode  
(set at 16.8 V, with 10 V)

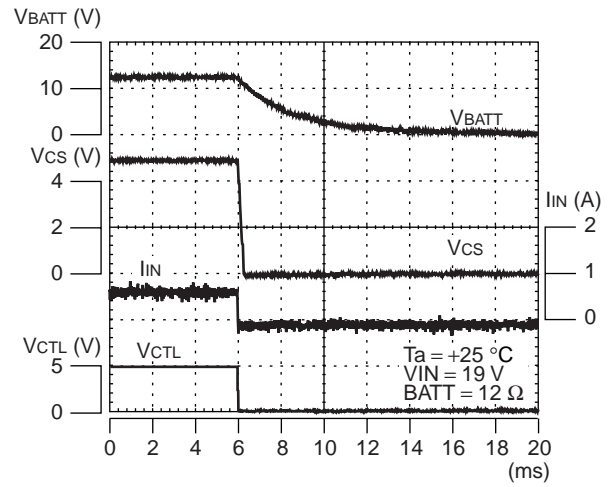


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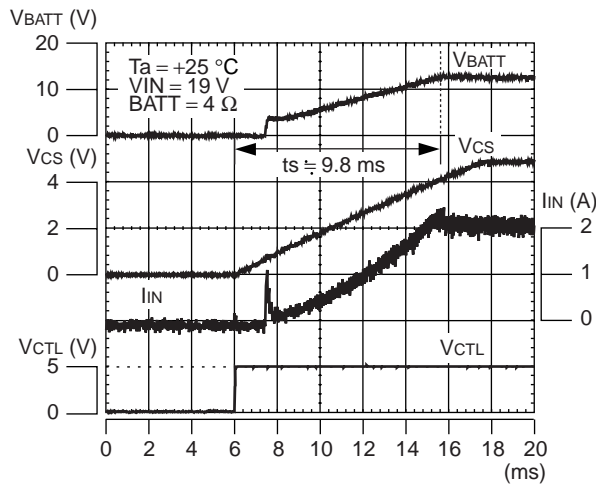
Soft-start operating waveform constant voltage mode (set at 12.6 V)



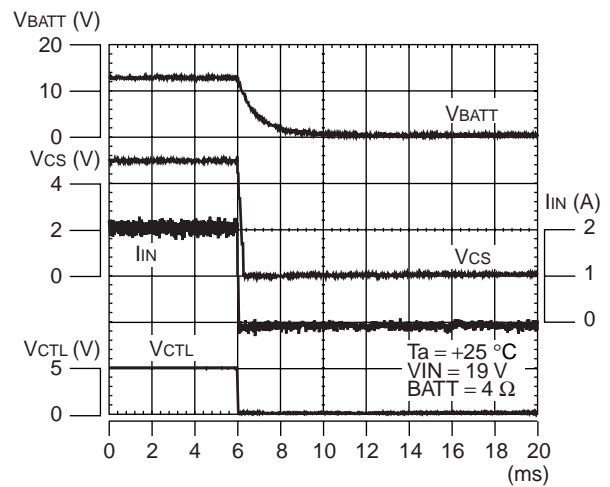
Discharge operating waveform constant voltage mode (set at 12.6 V)



Soft-start operating waveform constant current mode (set at 12.6 V)



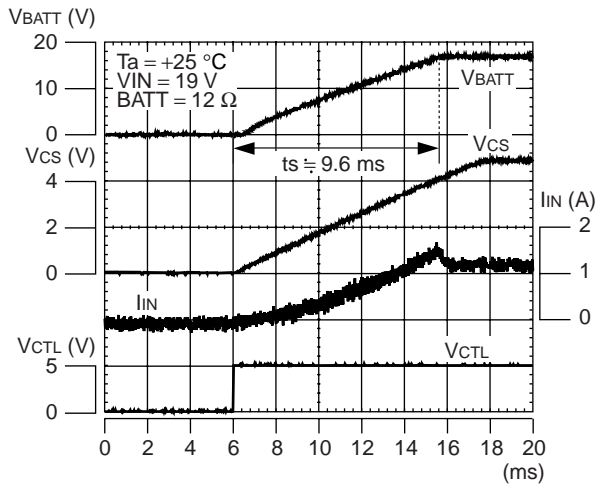
Discharge operating waveform constant current mode (set at 12.6 V)



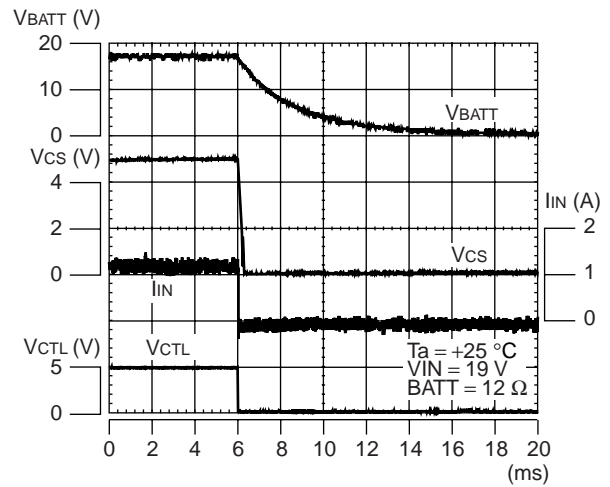
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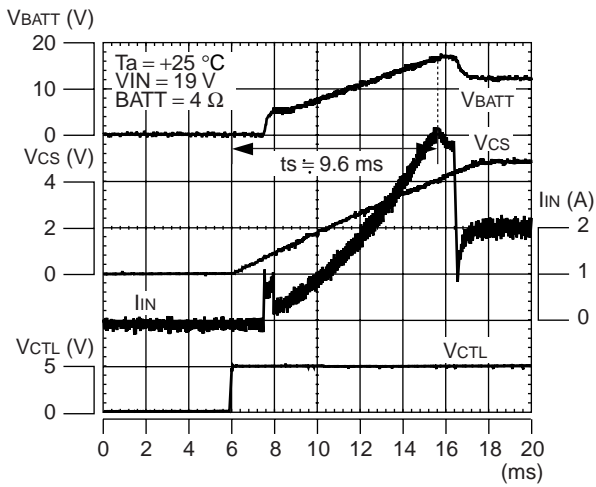
Soft-start operating waveform constant voltage mode (set at 16.8 V)



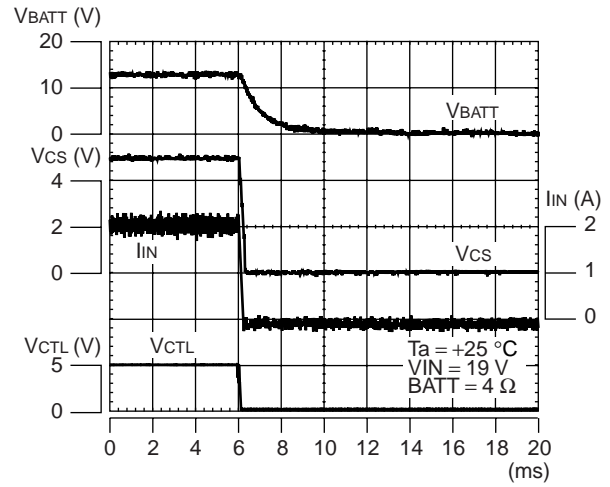
Discharge operating waveform constant voltage mode (set at 16.8 V)



Soft-start operating waveform constant current mode (set at 16.8 V)



Discharge operating waveform constant current mode (set at 16.8 V)



# MB3888

## ■ USAGE PRECAUTIONS

- Printed circuit board ground lines should be set up with consideration for common impedance.
- Take appropriate static electricity measures.
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 k $\Omega$  to 1 M $\Omega$  between body and ground.
- Do not apply negative voltages.
  - The use of negative voltages below  $-0.3$  V may create parasitic transistors on LSI lines, which can cause malfunction.

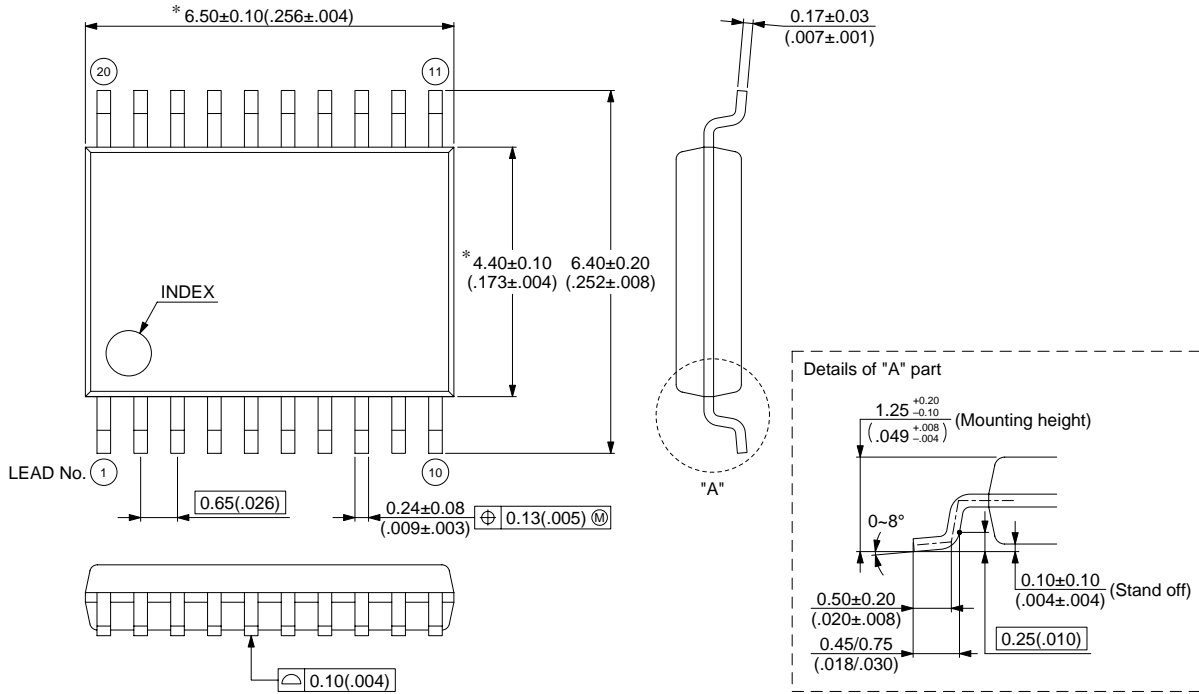
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB3888PFV	20-pin plastic SSOP (FPT-20P-M03)	

## PACKAGE DIMENSION

20-pin plastic SSOP  
(FPT-20P-M03)

Note 1 : These dimensions do not include resin protrusion.  
Note 2 : Pins width and thickness includes plating thickness.



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Dimensions in mm (inches)

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