FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11401-2E

MEMORY

CMOS

8 x 256K x 32 BIT DOUBLE DATA RATE FCRAM™

MB81N643289-50/-60

CMOS 8-BANK x 262,144-WORD x 32 BIT
Fast Cycle Random Access Memory (FCRAM)
with Double Data Rate

■ DESCRIPTION

The Fujitsu MB81N643289 is a CMOS Fast Cycle Random Access Memory (FCRAM) containing 67,108,864 memory cells accessible in an 32-bit format. The MB81N643289 features a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81N643289 is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints. The MB81N643289 uses Double Data Rate (DDR) where data bandwidth is twice of fast speed compared with regular SDRAMs.

The MB81N643289 is designed using Fujitsu advanced FCRAM Core Technology.

The MB81N643289 is ideally suited for Digital Visual System, High Performance Graphic Adapters, Hardware Accelerators, Buffers, and other applications where large memory density and high effective bandwidth are required and where a simple interface is needed.

The MB81N643289 adopts new I/O interface circuitry, 2.5 V CMOS Source Termination I/O interface, which is capable of extremely fast data transfer of quality under point to point bus environment.

■ PRODUCT LINE

Parameter		MB81N643289	
		-50	-60
Clock Frequency	CL = 3	200 MHz (Max.)	167 MHz (Max.)
	CL = 2	133 MHz (Max.)	111 MHz (Max.)
Burst Mode Cycle Time	CL = 3	2.5 ns (Min.)	3.0 ns (Min.)
	CL = 2	3.75 ns (Min.)	4.5 ns (Min.)
Random Address Cycle Time		30 ns (Min.)	36 ns (Min.)
DQS Access Time From Clock		$0.1 \times t_{CK}$ + 0.2 ns (Max.)	$0.1 \times t_{CK}$ + 0.2 ns (Max.)
Operating Current		450 mA (Max.)	385 mA (Max.)
Power Down Current		35 mA (Max.)	

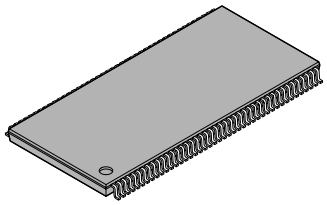
Note : FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Double Data Rate
- Bi-directional Data Strobe Signal
- Eight bank operation
- Burst read/write operation
- Programmable, burst length, and CAS latency
- Write latency (Write command to data input) = CAS latency -1
- Byte write control by DM_0 to DM_3
- Page Close Power Down Mode
- Distributed Auto-refresh cycle in 8 μs
- 2.5 V CMOS Source Termination I/O for all signals
- V_{DD}: +2.5V Supply ± 0.2V tolerance
- V_{DDQ}: +2.5V Supply ± 0.2V tolerance

■ PACKAGE

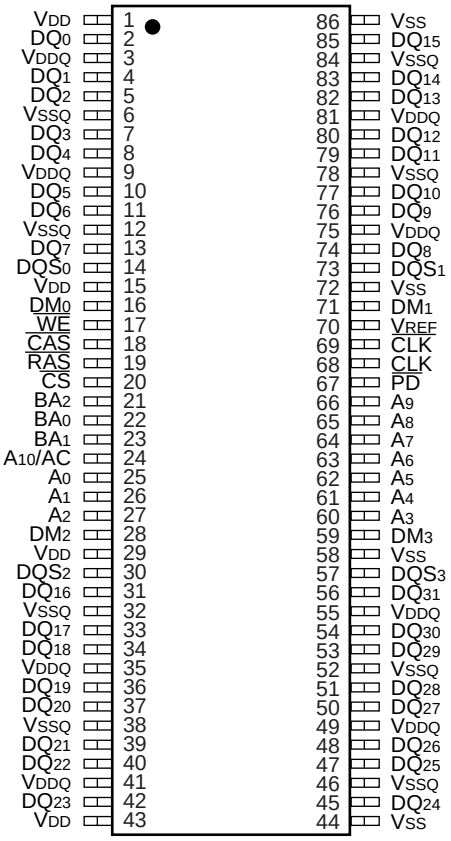
86-pin plastic TSOP(II)



(FPT-86P-M01)
(Normal Bend)

■ PIN ASSIGNMENTS

86-pin TSOP (II)
(TOP VIEW)
(Normal Bend)



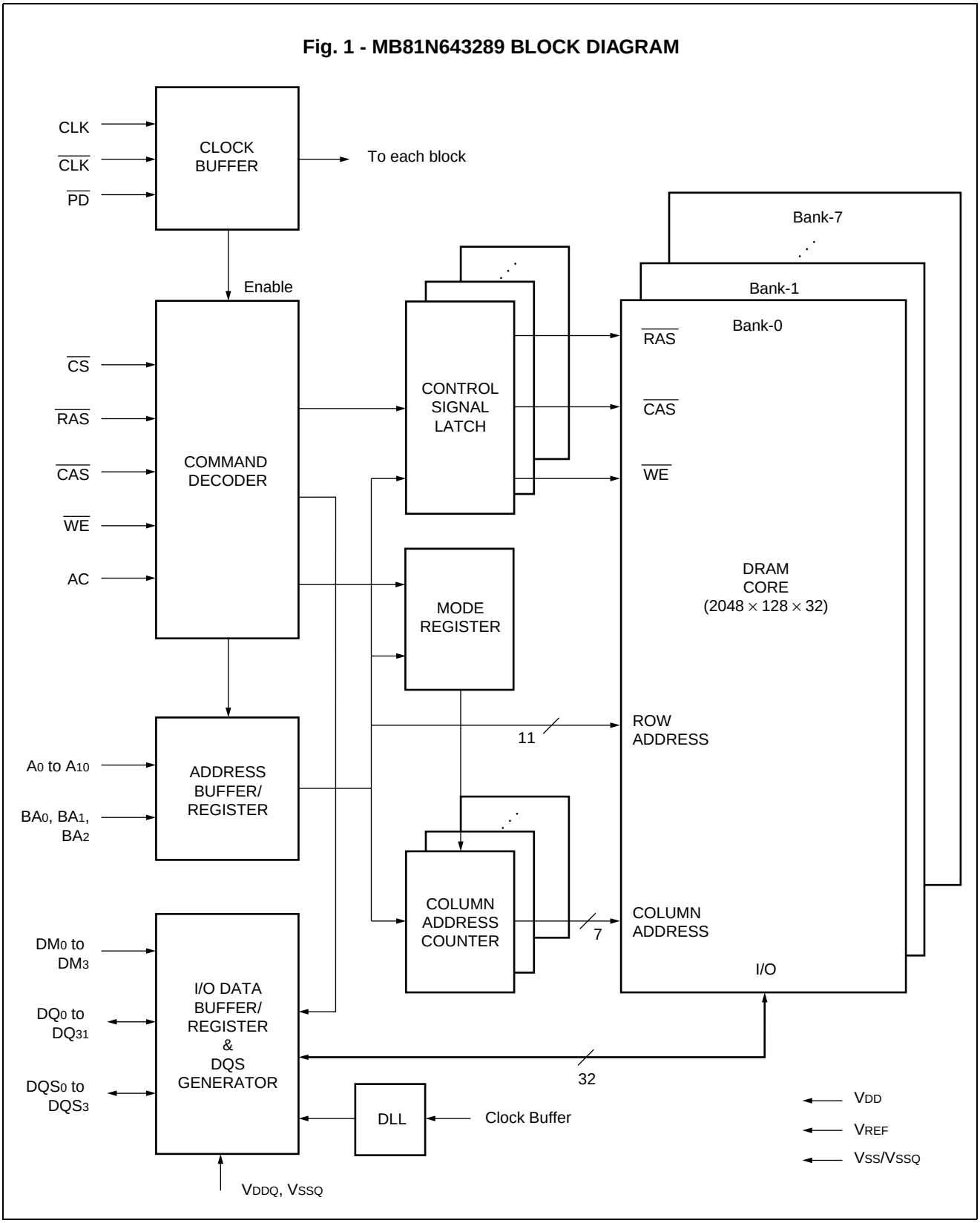
(FPT-86P-M01)

■ DESCRIPTIONS

Pin Number	Symbol	Function
1, 3, 9, 15, 29, 35, 41, 43, 49, 55, 75, 81	V_{DD}, V_{DDQ}	Supply Voltage
6, 12, 32, 38, 44, 46, 52, 58, 72, 78, 84, 86	V_{SS}, V_{SSQ}	Ground
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	DQ_0 to DQ_{31}	Data I/O • Byte 0 : DQ_0 to DQ_7 • Byte 1 : DQ_8 to DQ_{15} • Byte 2 : DQ_{16} to DQ_{23} • Byte 3 : DQ_{24} to DQ_{31}
14, 30, 57, 73	DQS_0 to DQS_3	Data Strobe • DQS_0 : for DQ_0 to DQ_7 • DQS_1 : for DQ_8 to DQ_{15} • DQS_2 : for DQ_{16} to DQ_{23} • DQS_3 : for DQ_{24} to DQ_{31}
16, 28, 59, 71	DM_0 to DM_3	Input Mask
17	$\overline{WE}$	Write Enable
18	$\overline{CAS}$	Column Address Strobe
19	$\overline{RAS}$	Row Address Strobe
20	$\overline{CS}$	Chip Select
21, 22, 23	BA_2, BA_1, BA_0	Bank Select (Bank Address)
24	AC	Auto Close Enable
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	A_0 to A_{10}	Address Input • Row: A_0 to A_{10} • Column: A_0 to A_6
67	$\overline{PD}$	Power Down
68	CLK	Clock Input
69	$\overline{CLK}$	Clock Input
70	V_{REF}	Input Reference Voltage

■ BLOCK DIAGRAM

Fig. 1 - MB81N643289 BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Note *1

COMMAND TRUTH TABLE

Note *2, and *3

Function	Notes	Symbol	$\overline{PD}$	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA_{2-0}	A_{10}/AC	A_{9-7}	A_{6-0}
Device Deselect	*4	DESL	H	H	X	X	X	X	X	X	X
No Operation	*4	NOP	H	L	H	H	H	X	X	X	X
Reserved		—	H	L	H	H	L	X	X	X	X
Read	*5	RD	H	L	H	L	H	V	L	X	V
Read with Auto-close	*5	RDA	H	L	H	L	H	V	H	X	V
Write	*5	WR	H	L	H	L	L	V	L	X	V
Write with Auto-close	*5	WRA	H	L	H	L	L	V	H	X	V
Bank Active ($\overline{RAS}$)	*6	ACTV	H	L	L	H	H	V	V	V	V
Page Close Single Bank	*7	PC	H	L	L	H	L	V	L	X	X
Page Close All Banks	*7	PCA	H	L	L	H	L	X	H	X	X
Mode Register Set/ Extended Mode Register Set	*7,*8,*9	MRS/ EMRS	H	L	L	L	L	V	L	V	V

Notes: *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H, Hi-Z = High Impedance.
*2. All commands are assumed to be valid state transitions.
*3. All inputs for command are latched on the rising edge of clock(CLK).
*4. NOP and DESL commands have the same effect on the part.
Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.
*5. RD, RDA, WR and WRA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to “■STATE DIAGRAM”.
*6. ACTV command should only be issued after corresponding bank has been page closed by PC or PCA command.
*7. Either PC or PCA command and MRS or EMRS command are required after power up.
*8. MRS or EMRS command should only be issued after all banks have been page closed (PC or PCA command), and DQs are in Hi-Z. Refer to “■STATE DIAGRAM”.
*9. Refer to “■MODE REGISTER TABLE”.

DM TRUTH TABLE (Effective during Write mode)

Function	Command	$\overline{PD}$		DM_0	DM_1	DM_2	DM_3
		(n - 1)	(n)				
Data Mask for DQ_0 to DQ_7	MASK0	H	X	H	X	X	X
Data Mask for DQ_8 to DQ_{15}	MASK1	H	X	X	H	X	X
Data Mask for DQ_{16} to DQ_{23}	MASK2	H	X	X	X	H	X
Data Mask for DQ_{24} to DQ_{31}	MASK3	H	X	X	X	X	H

$\overline{PD}$ TRUTH TABLE

Current State	Function	Notes	Command	$\overline{PD}$		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AC	BA_0 to BA_2	A_0 to A_{10}	DQ_0 to DQ_{31}
				(n-1)	(n)								
Idle	Auto-refresh	*10	REF	H	H	L	L	L	H	X	X	X	—
Idle	Self-refresh Entry	*10 *11	SELF	H	L	L	L	L	H	X	X	X	Hi-Z
Self-refresh	Self-refresh Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Self-refresh	Self-refresh Exit		SELFX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z
Idle	Power Down Entry	*12	PDEN	H	L	L	H	H	H	X	X	X	Hi-Z
				H	L	H	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Exit		PDEX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z

Notes: *10. The REF and SELF commands should only be issued after all banks have been precharged (PC or PCA command). In case of SELF command, it should also be issued after the last read data have been appeared on DQ. Refer to "■STATE DIAGRAM."

*11. $\overline{PD}$ must bring to Low level together with REF command.

*12. The PDEN command should only be issued after the last read data have been appeared on DQ and after the l_{WPL} is satisfied from last write data input.

OPERATION COMMAND TABLE (Applicable to single bank) **Note *13**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	—	—	Illegal	*14
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*15
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Bank Active after l_{RCD}	
	L	L	H	L	BA, AC	PC	NOP	
	L	L	H	L	BA, AC	PCA	NOP	*14
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*16
	L	L	L	L	MODE	MRS/EMRS	Mode Register / Extended Mode Register Set (Idle after l_{RSC})	*16
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Begin Read; Determine AC	
	L	H	L	L	BA, CA, AC	WR/WRA	Begin Write; Determine AC	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Page Close	
	L	L	H	L	BA, AC	PCA	Page Close	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	
	L	L	H	L	BA, AC	PCA	Illegal	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Bank Active)	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	
	L	L	H	L	BA, AC	PCA	Illegal	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read With Auto-Close	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Bank Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Bank Idle)	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*17
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*17
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	*15
	L	L	H	L	BA, AC	PCA	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	
Write with Auto-Close	H	X	X	X	X	DESL	NOP (Continue Burst to End -> Bank Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End -> Bank Idle)	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*17
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*17
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	*15
	L	L	H	L	BA, AC	PCA	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Page Close	H	X	X	X	X	DESL	NOP (Idle after t_{PCL})	
	L	H	H	H	X	NOP	NOP (Idle after t_{PCL})	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*15
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	NOP	*15
	L	L	H	L	BA, AC	PCA	NOP	*14
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after l_{RCD})	
	L	H	H	H	X	NOP	NOP (Bank Active after l_{RCD})	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*15
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*15
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	*15
	L	L	H	L	BA, AC	PCA	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Write Recovering	H	X	X	X	X	DESL	NOP (Bank Active after l_{WRL})	
	L	H	H	H	X	NOP	NOP (Bank Active after l_{WRL})	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	
	L	H	L	L	BA, CA, AC	WR/WRA	New Write; Determine AC	
	L	L	H	H	BA, RA	ACTV	Illegal	
	L	L	H	L	BA, AC	PC	Illegal	*15
	L	L	H	L	BA, AC	PCA	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	
Write Recovering with Auto-Close	H	X	X	X	X	DESL	NOP (Idle after l_{WAL})	
	L	H	H	H	X	NOP	NOP (Idle after l_{WAL})	
	L	H	H	L	—	—	Illegal	
	L	H	L	H	BA, CA, AC	RD/RDA	Illegal	*17
	L	H	L	L	BA, CA, AC	WR/WRA	Illegal	*17
	L	L	H	H	BA, RA	ACTV	Illegal	*15
	L	L	H	L	BA, AC	PC	Illegal	*15
	L	L	H	L	BA, AC	PCA	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS/EMRS	Illegal	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after l_{REFC})	
	L	H	H	X	X	NOP	NOP (Idle after l_{REFC})	
	L	H	L	X	X	RD/RDA/ WR/WRA	Illegal	
	L	L	H	X	X	ACTV/ PC/PCA	Illegal	
	L	L	L	X	X	REF/SELF/ MRS/EMRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after I_{RSC})	
	L	H	H	H	X	NOP	NOP (Idle after I_{RSC})	
	L	H	H	L	—	—	Illegal	
	L	H	L	X	X	RD/RDA/ WR/WRA	Illegal	
	L	L	X	X	X	ACTV/PC/PCA/ REF/SELF/ MRS/EMRS	Illegal	

Abbreviations: RA = Row Address BA = Bank Address
CA = Column Address AC = Auto Close

Notes: *13. All entries assume the $\overline{PD}$ was High during the proceeding clock cycle and the current clock cycle.
*14. Entry may affect other banks.
*15. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
*16. Illegal if any bank is not idle.
*17. Entry may legal specified by BA if applicable AC specification are satisfied.

COMMAND TRUTH TABLE FOR $\overline{PD}$

Current State	$\overline{PD}$ (n-1)	$\overline{PD}$ (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Idle after I_{LOCK})	
	L	H	L	H	H	H	X	Exit Self-refresh (Idle after I_{LOCK})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after I_{LOCK}	
	H	H	L	H	H	H	X	Idle after I_{LOCK}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Power Down (Idle after t_{PDE})	
	L	H	L	H	H	H	X	Exit Power Down (Idle after t_{PDE})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	

COMMAND TRUTH TABLE FOR $\overline{PD}$ (continued)

Current State	$\overline{PD}$ (n-1)	$\overline{PD}$ (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
All Banks Idle	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	H	X	X	X	X	Power Down Entry	*18
	H	L	L	H	H	H	X	Power Down Entry	*18
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh Entry	
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	

COMMAND TRUTH TABLE FOR $\overline{PD}$ (continued)

Current State	$\overline{PD}$ (n-1)	$\overline{PD}$ (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Read, Write, Write Page Closing	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*19
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	
Refreshing	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	H	X	X	X	X	Illegal	
	H	L	L	H	H	H	X	Illegal	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	

*18. PDEN and SELF command should only be issued after the last read data have been appeared on DQ.

*19. The Clock Suspend mode is not supported on this device and it is illegal if $\overline{PD}$ is brought to Low during the Burst Read or Write mode.

■ STATE DIAGRAM

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

First command \ Second command (same bank)	MRS	ACTV	RD	RDA	WR	WRA	PC	PCA *1	REF	SELF
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV			t_{RCD}	t_{RCD} *3	t_{RCDW}	t_{RCDW} *3	t_{RAS}	t_{RAS}		
RD			t_{CCD}	t_{CCD} * 3	t_{RWL} * 2	t_{RWL} *2, 3	t_{RPL} *3	t_{RPL} *3		
RDA	t_{RDA} *4, 5	t_{RDA}					t_{RDA} *3	t_{RDA} *3	t_{RDA} *5	t_{RDA} *4, 5
WR			t_{WRL}	t_{WRL} *3	t_{CCD}	t_{CCD} *3	t_{WPL} *3	t_{WPL} *3		
WRA	t_{WAL} *5	t_{WAL}					t_{WAL} *3	t_{WAL} *3	t_{WAL} *5	t_{WAL} *5
PC	t_{PCL} *4, 5	t_{PCL}					1	1 *3	t_{PCL} *5	t_{PCL} *4, 5
PCA	t_{PCAL} *4	t_{PCAL}					1	1	t_{PCAL}	t_{PCAL} *4
REF	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{LOCK}	t_{LOCK}					t_{LOCK}	t_{LOCK}	t_{LOCK}	t_{LOCK}

Notes: *1. Assume PCA command does not affect any operation on the other banks.
*2. Assume no I/O conflict.
*3. t_{RAS} must be satisfied.
*4. Assume all outputs are in High-Z state.
*5. Assume all other banks are in idle state.

Illegal Command

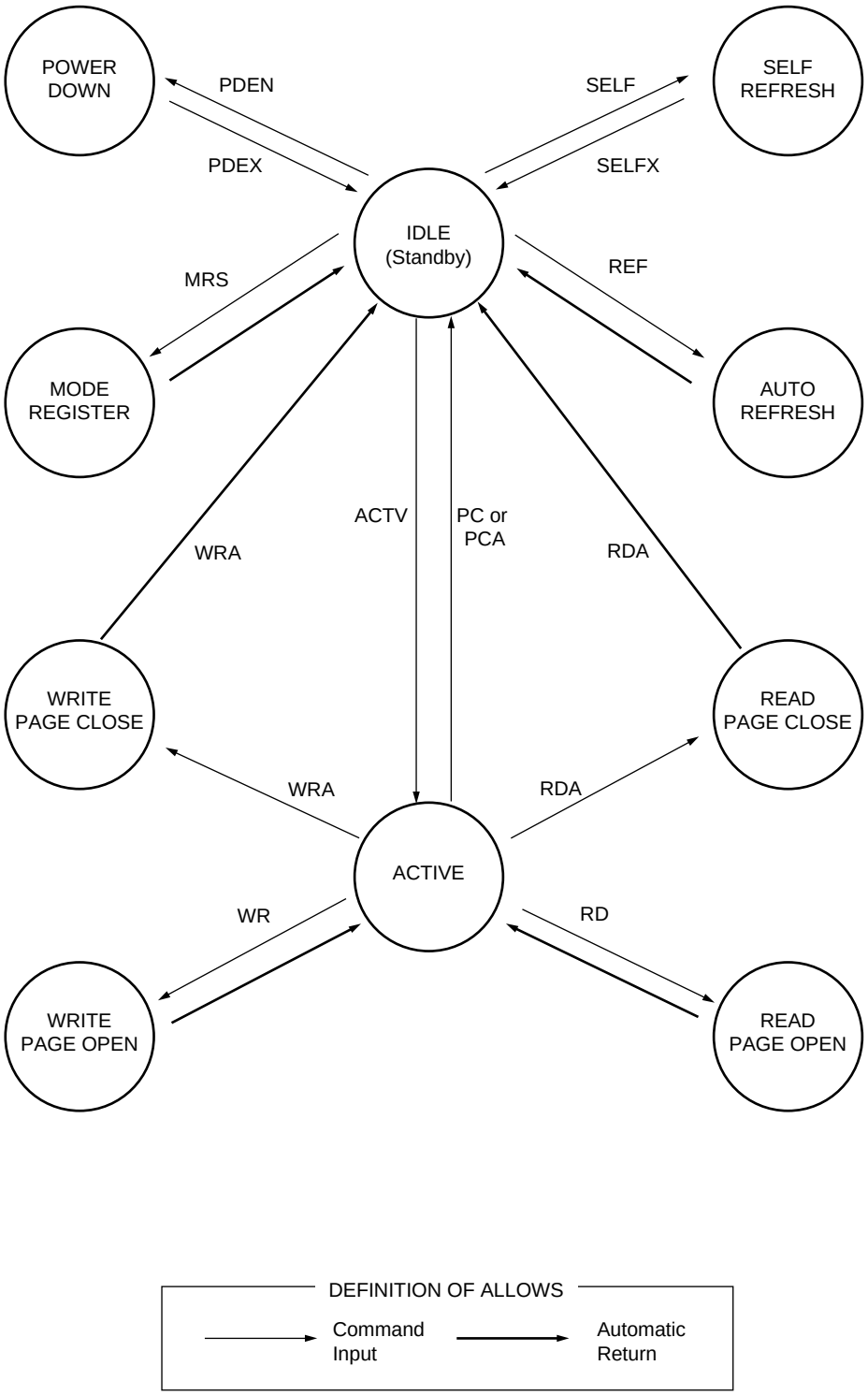
MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTIPLE BANK OPERATION

First command \ Second command (other bank) *9	MRS	ACTV	RD *7	RDA *7	WR *7	WRA *7	PC *8	PCA *1, 8	REF	SELF
MRS	l_{RSC}	l_{RSC}					l_{RSC}	l_{RSC}	l_{RSC}	l_{RSC}
ACTV		l_{RRD} *5	1 *10	1 *3, 10	1 *2, 10	1 *2, 10	1	t_{RAS}		
RD		1 *5	l_{CBD}	l_{CBD} *8	l_{RWL} *2	l_{RWL} *2, 8	1	l_{RPL} *3		
RDA	l_{RDA} *6	1 *5	l_{CBD} *4	l_{CBD} *3	l_{RWL} *2	l_{RWL} *2	1	l_{RDA}	l_{RDA} *6	l_{RDA} *4, 6
WR		1 *5	l_{WRD}	l_{WRD} *3	l_{CBD}	l_{CBD} *3	1	l_{WPL} *3		
WRA	l_{WAL} *6	1 *5	l_{WRD}	l_{WRD} *3	l_{CBD}	l_{CBD}	1	l_{WAL}	l_{WAL} *6	l_{WAL} *6
PC	t_{PCL} *6	1 *5	1 *10	1 *3, 10	1 *2, 10	1 *2, 10	1	1 *3	t_{PCL} *6	t_{PCL} *4, 6
PCA	t_{PCAL}	t_{PCAL}					1	1	t_{PCAL}	t_{PCAL} *4
REF	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	l_{LOCK}	l_{LOCK}					l_{LOCK}	l_{LOCK}	l_{LOCK}	l_{LOCK}

Notes: *1. Assume PCA command does not affect any operation on the other bank(s).
*2. Assume no I/O conflict.
*3. t_{RAS} must be satisfied.
*4. Assume all outputs are in High-Z state.
*5. Assume applicable bank is in idle state.
*6. Assume all other banks are in idle state.
*7. Assume the other bank(s) is in active state and l_{RCD} or l_{RCDW} is satisfied.
*8. Assume the other bank(s) is in active state and t_{RAS} is satisfied.
*9. Second command have to follow the minimum clock latency or delay time of single bank operation in other bank (second command is asserted.)
*10. Assume other banks are not in RD/RDA/WR/WRA state.

Illegal Command.

Fig. 2 - STATE DIAGRAM (Simplified for Single Bank Operation)



■ FUNCTIONAL DESCRIPTION

DDR, Double Data Rate Function

The regular SDRAM read and write cycle have only used the rising edge of external clock input. When clock signal goes to High from Low at the read mode, the read out data will be available at every rising clock edge after the specified latency up to burst length. The MB81N643289 DDR FCRAM features a twice of data transfer rate within a same clock period by transferring data at every rising and falling clock edge. Refer to Figure 3.

FCRAM™

The MB81N643289 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

CLOCK INPUTS (CLK, $\overline{CLK}$)

The MB81N643289 adopts differential clock scheme. CLK is a master clock and its rising edge is used to latch all command and address inputs. $\overline{CLK}$ is a complementary clock input.
The MB81N643289 implements Delay Locked Loop (DLL) circuit. This internal DLL tracks the signal cross point between CLK and $\overline{CLK}$ and generate some clock cycle delay for the output buffer control at Read mode.
The internal DLL circuit requires some Lock-on time for the stable delay time generation. In order to stabilize the delay, a constant stable clock input for t_{LOCK} period is required during the Power-up initialization and a constant stable clock input for t_{LOCK} period is also required after Self-refresh exit as specified t_{LOCK} prior to the any command.

POWER DOWN ($\overline{PD}$)

$\overline{PD}$ is a synchronous input signal and enables power down mode.
When all banks are in idle state, $\overline{PD}$ controls Power Down (PD) and Self-refresh mode. The PD and Self-refresh is entered when $\overline{PD}$ is brought to Low and exited when it returns to High.
During the Power Down and Self-refresh mode, both CLK and $\overline{CLK}$ are disabled after specified time.
$\overline{PD}$ does not have a Clock Suspend function unlike CKE pin of regular SDRAMs, and it is illegal to bring $\overline{PD}$ into Low if any read or write operation is being performed. For the detail, refer to Timing Diagrams.
It is recommended to maintain $\overline{PD}$ to be Low until V_{DD} gets in the specified operating range in order to assure the power-up initialization.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is High, all command signals are negated but internal operation such as burst cycle will not be suspended.

COMMAND INPUTS ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

As well as regular SDRAMs, each combination of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines FCRAM operation. Refer to“ ■FUNCTION TRUTH TABLE”.

BANK ADDRESS (BA_0 to BA_2)

The MB81N643289 has eight internal banks and each bank is organized as 256K words by 32-bit.
Bank selection by BA occurs at Bank Active command (ACTV) followed by read (RD or RDA), write (WR or WRA), and Page Close(PC) command.

ADDRESS INPUTS (A_0 to A_{10})

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix within each bank. A total of twenty address input signals are required to decode such a matrix. The MB81N643289 adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), eleven Row addresses are initially latched as well as three bank addresses and the remainder of seven Column addresses are then latched by a Column address strobe command of either a read command (RD or RDA) or write command (WR or WRA).

DATA STROBE (DQS_0 to DQS_3)

DQS_0 to DQS_3 are bi-directional signal and represent byte 0 to byte 3, respectively. During Read operation, DQS_0 to DQS_3 provides the read data strobe signal that is intended to use input data strobe signal at the receiver circuit of the controller(s). It turns Low before first data is coming out and toggle High to Low or Low to High till end of burst read. Refer to Figure 3 for the timing example.
The CAS Latency is specified to the first Low to High transition of these DQS_0 to DQS_3 output.
During the write operation, DQS_0 to DQS_3 are used to latch write data and Data Mask signals. As well as the behavior of read data strobe, the first rising edge of DQS_0 to DQS_3 input latches first input data and following falling edge of DQS_0 to DQS_3 signal latches second input data. This sequence shall be continued till end of burst count. Therefore, DQS_0 to DQS_3 must be provided from controller that drives write data.
Note that DQS_0 to DQS_3 input signal should not be tristated from High at the end of write mode.

DATA INPUTS AND OUTPUTS (DQ_0 to DQ_{31})

Input data is latched by DQS_0 to DQS_3 input signal and written into memory. After the (CL-1) clock cycle from the Write command, data input is started from the rising edge of DQS. Output data is obtained together with DQS_0 to DQS_3 output signals at programmed read CAS latency.
The polarity of the output data is identical to that of the input. Data is valid after DQS_0 to DQS_3 output signal transitions (t_{QSQ}) as specified in Data Valid Time (t_{QSQV}).

WRITE DATA MASK (DM_0 to DM_3)

DM_0 to DM_3 are active High enable inputs and represent byte 0 to byte 3 respectively. DM_0 to DM_3 have a data input mask function, and are also sampled by DQS_0 to DQS_3 input signal together with input data.
During write cycle, DM_0 to DM_3 provide byte mask function. When DMx = High is latched by a DQS_0 to DQS_3 signal edge, data input at the same edge of DQS_0 to DQS_3 is masked.

During read cycle, the DM_0 to DM_3 inactive and does not have any effect on read operation.
Refer to DM TRUTH TABLE.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access and MB81N643289 read and write operations are burst oriented. The burst mode is implemented by keeping the same Row address and by automatic strobing Column address in every single clock edge till programmed burst length(BL). Access time of burst mode is specified as t_{AC}. The internal column address counter operation is determined by a mode register which defines burst type(BT) and burst count length(BL) of 2, 4 or 8 bits of boundary.

The burst type is sequential only. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to the least significant address(= 0). If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode
2	X X 0	0 – 1
	X X 1	1 – 0
4	X 0 0	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0
	X 1 0	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6

PAGE CLOSE AND PAGE CLOSE OPTION (PC, PCA)

The DDR FCRAM memory core is the same as conventional DRAMs', requiring Page close and refresh operations. Page close rewrites the bit line and to reset the internal Row address line and is executed by the Page close operation (PC or PCA). With the Page close operation, DDR SDRAM will automatically be in standby state after specified precharge time (t_{PCL}).

The Page closed bank is selected by combination of AC and bank address (BA) when Page close command is issued. If AC = High, all banks are Page closed regardless of BA (PCA command). If AC = Low, a bank to be selected by BA is Page closed (PC command).

The auto-pageclose enters Page close mode at the end of burst mode of read or write without Page close command issue. This auto-pageclose is entered by AC = High when a Read (RD) or Write (WR) command is issued.

Refer to "■FUNCTION TRUTH TABLE".

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The MB81N643289 Auto-refresh command (REF) automatically generates Bank Active and Page close command internally. All banks of SDRAM should be Page closed prior to the Auto-refresh command. The Auto-refresh command should also be issued within every 8 µs period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh operation until cancelled by SELFX.

The Self-refresh mode is entered by applying an Auto-refresh command in conjunction with $\overline{PD}$ = Low (SELF). Once MB81N643289 enters the self-refresh mode, all inputs except for $\overline{PD}$ can be either logic high or low level state and outputs will be in a High-Z state. During Self-refresh mode, $\overline{PD}$ = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit Self-refresh mode, $\overline{PD}$ must bring to High for at least 2 clock cycles together with NOP condition.

Refer to Timing Diagram for the detail procedure. It is recommended to issue at least one Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

WARNING: A stable clock for l_{LOCK} period with a constant duty cycle must be supplied prior to applying any command to insure the DLL is locked against the latest device conditions.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted both before the self-refresh entry and after the self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS Latency, and Test Mode Entry (This Test Mode Entry must not be used.) Refer to MODE REGISTER TABLE.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all banks are in idle state and all DQS are in High-Z. The condition of the mode register is undefined after the power-up stage. It is required to set each field at power-up initialization.

Refer to POWER-UP INITIALIZATION below.

Note: The Extended Mode Register Set command (EMRS) and its DLL Enable function of EMRS field is only used at power-on sequence.

POWER-UP INITIALIZATION

The MB81N643289 internal condition at and after power-up will be undefined. Since MB81N643289 adopts the method for two power supplies, which has two different power supply pins for internal core and I/O, it is required to follow the following Power On Sequence to execute read or write operation.

1. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins and attempt to maintain all input signals to be Low state (or at least $\overline{PD}$ to be Low state).
2. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF}.
3. Apply V_{REF}.
4. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200µs.
5. After the minimum of 200µs stable power and clock, apply NOP condition and take $\overline{PD}$ to be High state.
6. Issue Page Close All Banks (PCA) command or Page Close Single Bank (PC) command to every banks.
7. Issue EMRS to enable DLL, DE = Low.
8. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for t_{LOCK}*1 period is required to lock the DLL.
9. Apply minimum of two Auto-refresh command (REF).*2
10. Program the mode register by Mode Register Set command (MRS) with DR = Low.*2

*1: . The t_{LOCK} depends on operating clock period. The t_{LOCK} is counted from “DLL Reset” at step-8 to any command input at step-10.

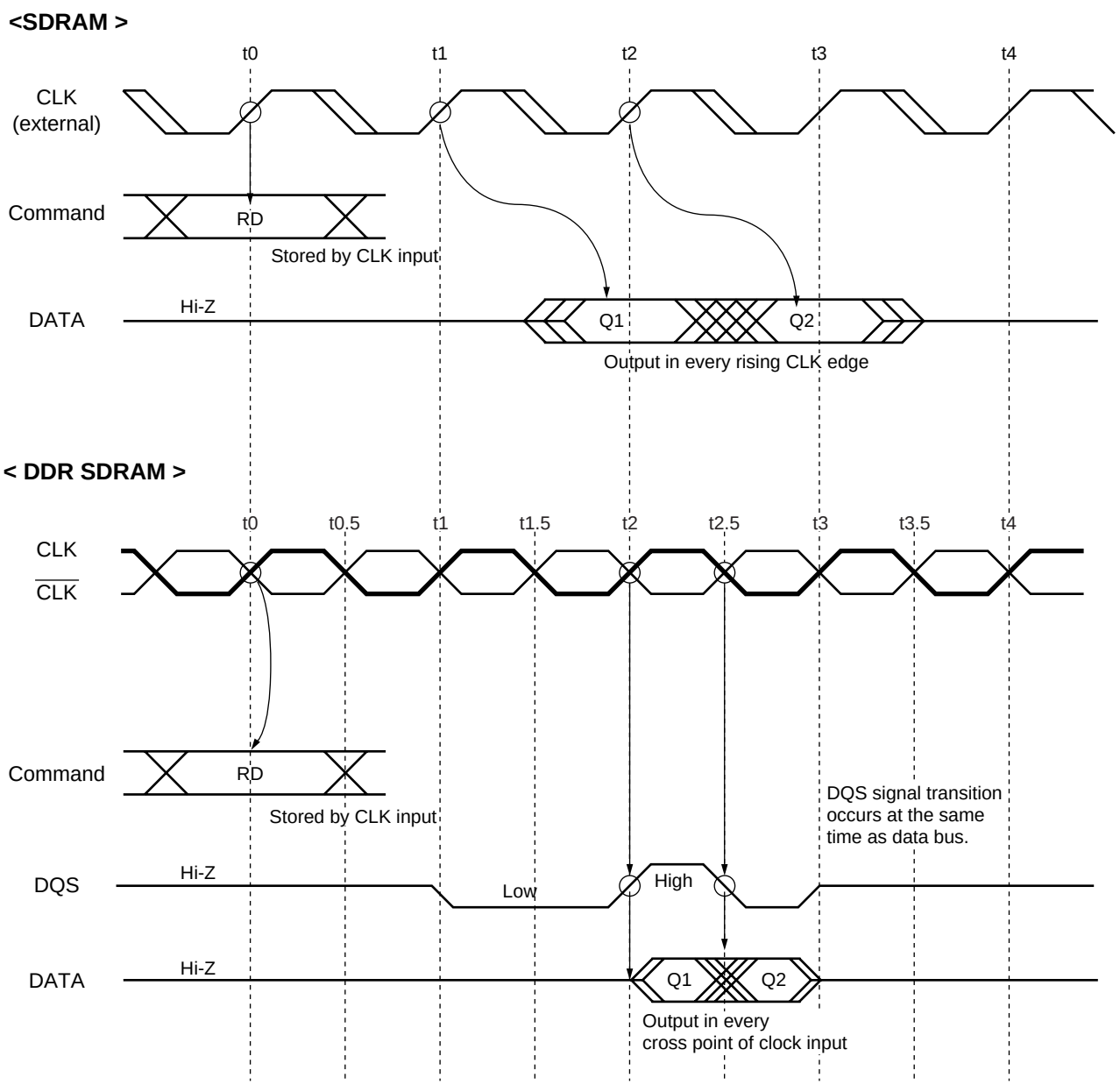
*2: . The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle (REF).

POWER-DOWN

The MB81N643289 uses multiple power supply voltage. It is required to follow the reversed sequence of above Power On Sequence.

1. Take all input signals to be V_{SS} or High-Z.
2. Deapply V_{DDQ}.
3. Deapply V_{DD} after or at the same time as V_{DDQ}.

Fig. 3 - SDRAM READ TIMING EXAMPLE (@ CL=2 & BL=2)



■ MODE REGISTER TABLE

MODE REGISTER SET

ADDRESS	BA_2	BA_1	BA_0	A_{10}	A_9	A_8	A_7	A_6 to A_4	A_3	A_2 to A_0
REGISTER	0*1	0*1	0*1	0	1*2	DR	TE	CL	BT	BL

A_6	A_5	A_4	CAS Latency (CL)
0	0	X	Reserved
0	1	0	2 *5
0	1	1	3 *5
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length (BL)
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	X	X	Reserved

A_7	Test Mode Entry (TE)
0	Normal Operation
1	Test Mode (Used for Supplier Test Mode)

A_3	Burst Type (BT)
0	Sequential (Wrap round, Binary up)
1	Reserved

A_8	DLL RESET (DR)
0	Normal Operation
1	RESET DLL

EXTENDED MODE REGISTER SET (Note *4)

ADDRESS	BA_2	BA_1	BA_0	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
EXTENDED MODE REGISTER	0*3	0*3	1*3	RESERVED *4										DE

A_0	DLL Enable (DE)
0	DLL Enable
1	DLL Disable

*1: A combination of $BA_2 = BA_1 = BA_0 = 0$ (Low) selects standard Mode Register.

*2: This field must be set as 1.

*3: A combination of $BA_2 = BA_1 = 0$ and $BA_0 = 1$ (High) selects Extended Mode Register.

*4: The RESERVED field must be set as 0.

*5: Write latency (WL) = CL-1

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}, V_{DDQ}	–0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	2.0	W
Storage Temperature	T_{STG}	–55 to +125	°C

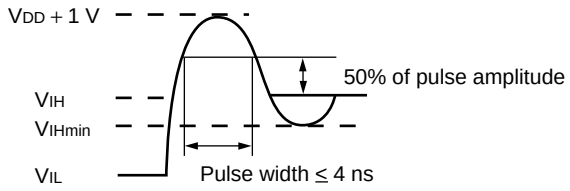
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

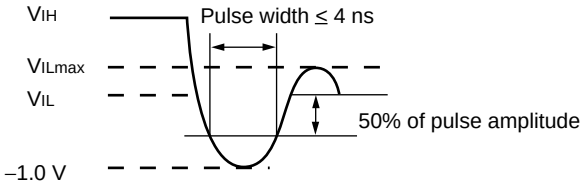
(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	2.3	2.5	2.7	V
		V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input Reference Voltage	*3	V_{REF}	$V_{DDQ}/2 \times 98\%$ (1.15V (Min.))	$V_{DDQ}/2$	$V_{DDQ}/2 \times 102\%$ (1.35V (Max.))	V
Single Ended DC Input High Level		$V_{IH(DC)}$	V_{REF} + 0.25	—	V_{DDQ} + 0.1	V
Single Ended DC Input Low Level		$V_{IL(DC)}$	–0.1	—	V_{REF} – 0.25	V
Single Ended AC Input High Level	*1	$V_{IH(AC)}$	V_{REF} + 0.35	—	V_{DDQ} + 0.1	V
Single Ended AC Input Low Level	*2	$V_{IL(AC)}$	–0.1	—	V_{REF} – 0.35	V
Differential DC Level Input Voltage		$V_{IN(DC)}$	–0.1	—	V_{DDQ} + 0.1	V
Differential DC Level Differential Input Voltage		$V_{SWING(DC)}$	0.50	—	V_{DDQ} + 0.2	V
Differential AC Level Differential Input Voltage		$V_{SWING(AC)}$	0.70	—	V_{DDQ} + 0.2	V
Differential AC Level Input Cross Point Voltage		$V_{X(AC)}$	$V_{DDQ}/2$ – 0.2	$V_{DDQ}/2$	$V_{DDQ}/2$ + 0.2	V
Differential Input Signal Offset Voltage	*4	$V_{ISO(AC)}$	$V_{DDQ}/2$ – 0.2	$V_{DDQ}/2$	$V_{DDQ}/2$ + 0.2	V
Ambient Temperature		T_A	0	—	70	°C

Notes:



*1. Overshoot limit: V_{IH} (Max.)
= V_{DD} + 1.0 V for pulse width ≤ 4 ns acceptable,
pulse width measured at 50% of pulse amplitude.



*2. Undershoot limit: V_{IL} (Min.)
= V_{SS} –1.0V for pulse width ≤ 4 ns acceptable,
pulse width measured at 50% of pulse amplitude.

*3. V_{REF} is expected to track variations in the DC level of V_{DDQ} of the transmitting device.
Peak-to-Peak noise level on V_{REF} may not exceed ± 2% of the supplied DC value.

*4. V_{ISO} means {$V_{IN(CLK)}$ + $V_{IN(\overline{CLK})}$} / 2. Refer to Differential Input Signal Definition.

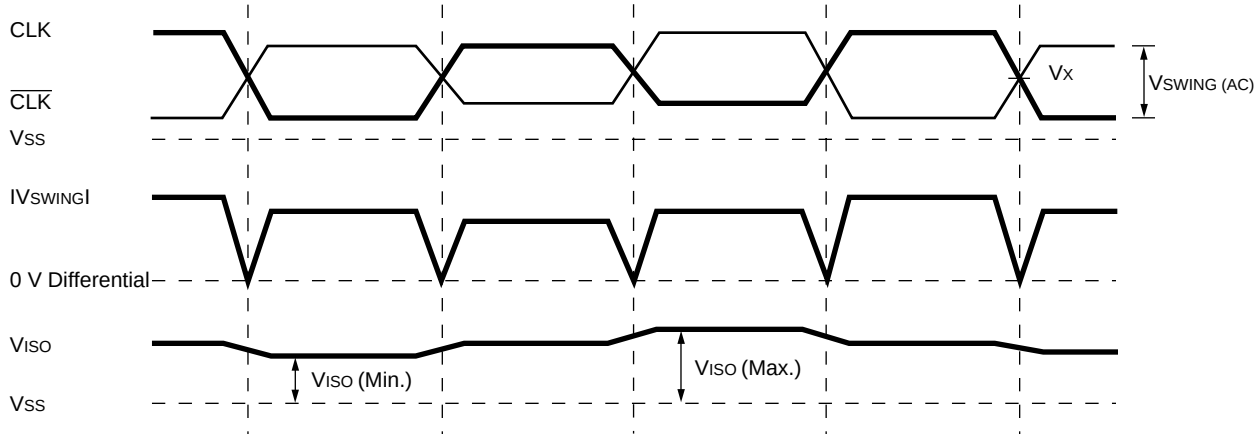
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Differential Input Signal Definition

fig. 4 - Differential Input Signal Offset Voltage (For Clock Input)



■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Address & Control	C_{IN1}	2.5	—	3.5	pF
Input Capacitance, CLK & $\overline{CLK}$	C_{IN2}	2.5	—	3.5	pF
Input Capacitance, DM_0 to DM_3	C_{IN3}	4.0	—	5.5	pF
I/O Capacitance	$C_{I/O}$	4.0	—	5.5	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note *1,*2,*3

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Output Minimum Source DC Current *4		$I_{OH(DC)}$	V_{DDQ} = 2.3V for Min., 2.7V for Max. V_{OH} = V_{DDQ}-0.2V	-4.0	-6.8	mA
Output Minimum Sink DC Current *4		$I_{OL(DC)}$	V_{DDQ} = 2.3V for Min., 2.7V for Max. V_{OL} = +0.2V	4.0	6.8	mA
Input Leakage Current (any input)		I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}; All other pins not under test = 0 V	-10	10	µA
Output Leakage Current		I_{LO}	0 V ≤ V_{IN} ≤ V_{DD}; Data out disabled	-10	10	µA
V_{REF} Current		I_{REF}		-10	10	µA
Operating Current (Average Power Supply Current)	MB81N643289-50	I_{DD1S}	Burst Length = 2 t_{CK} = Min., t_{RC} = Min. for BL = 2 One bank active, Address change up to 3 times during t_{RC} (Min.) 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	450	mA
	MB81N643289-60				385	
Standby Current	MB81N643289-50	I_{DD2N}	$\overline{PD}$ = V_{IH}, t_{CK} = Min. All banks idle, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	85	mA
	MB81N643289-60				75	
Power Down Current		I_{DD2P}	$\overline{PD}$ = V_{IL}, t_{CK} = Min. All banks idle, 0 V ≤ V_{IN} ≤ V_{DD}	—	35	mA
Active Standby Current (Power Supply Current)	MB81N643289-50	I_{DD3N}	$\overline{PD}$ = V_{IH}, t_{CK} = Min. All banks Active, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	235	mA
	MB81N643289-60				200	

(Continued)

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Burst Read Current (Average Power Supply Current)	MB81N643289-50	I_{DD4R}	Burst Length = 4, CAS Latency = 3, All bank active, Gapples data, t_{CK} = Min., 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	510	mA
	MB81N643289-60				430	
Burst Write Current (Average Power Supply Current)	MB81N643289-50	I_{DD4W}	Burst Length = 4, CAS Latency = 3, All bank active, Gapless data, t_{CK} = Min., 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	595	mA
	MB81N643289-60				505	
Auto-refresh Current (Average Power Supply Current)	MB81N643289-50	I_{DD5}	Auto-refresh; t_{CK} = Min., t_{REFC} = Min. 0 V ≤ V_{IN} ≤ V_{IL} (Max.), V_{IH} (Min.) ≤ V_{IN} ≤ V_{DD}	—	320	mA
	MB81N643289-60				270	
Self-refresh Current (Average Power Supply Current)		I_{DD6}	Self-refresh; $\overline{PD}$ = V_{IL}, 0 V ≤ V_{IN} ≤ V_{DD}	—	5	mA

Notes: *1. All voltages referenced to V_{SS}.

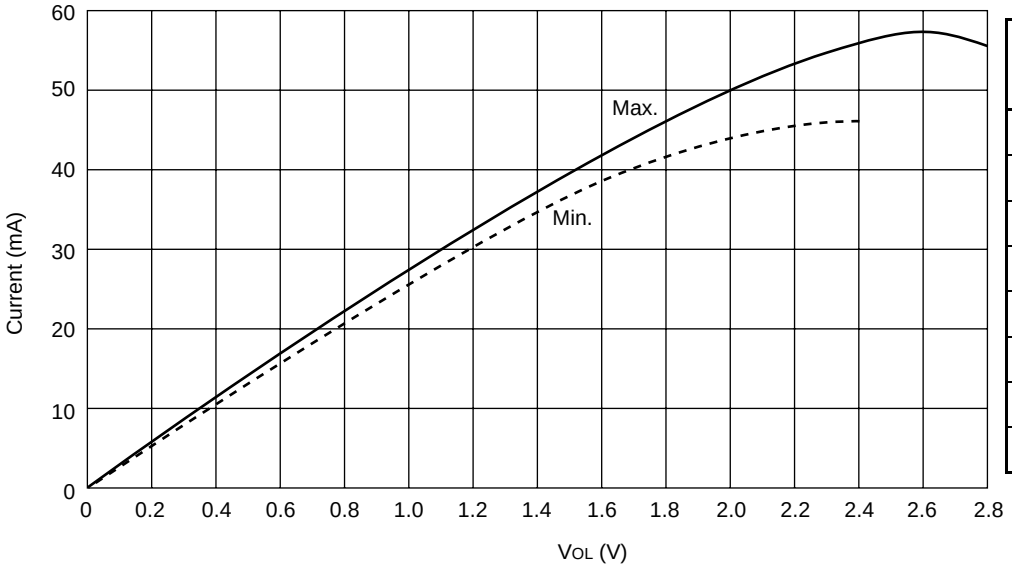
*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.

*3. I_{DD} depends on the output termination or load conditions, clock cycle rate, and number of address and command change within certain period. The specified values are obtained with the output open.

*4. Refer to output characteristics for the detail.

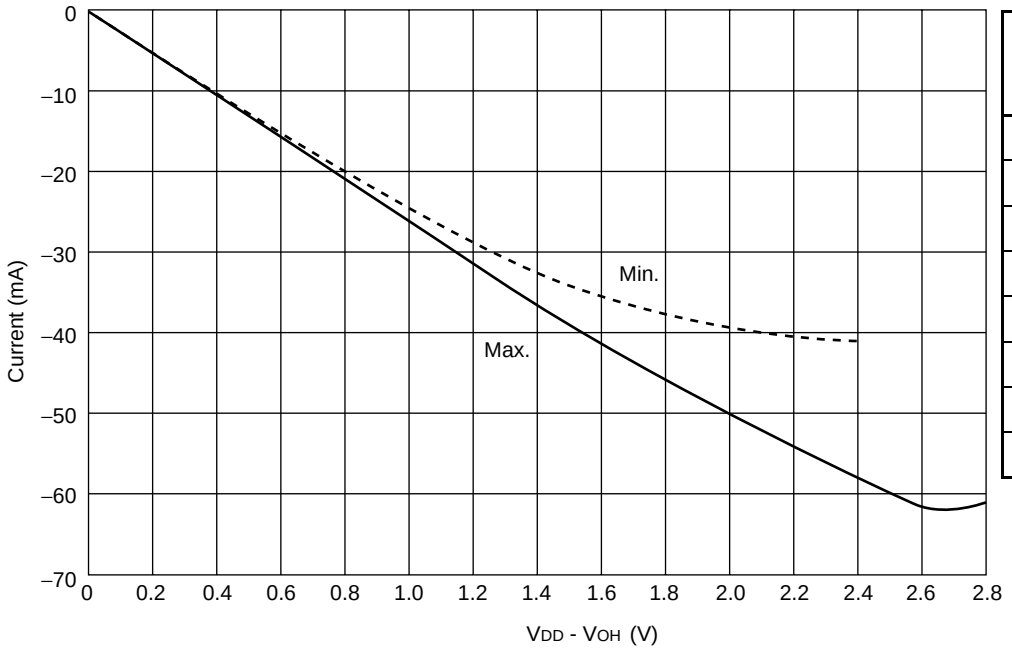
OUTPUT CHARACTERISTICS

Fig. 5 - Pull-down Characteristics



V_{OL} (V)	Current (mA)	
	Min.	Max.
0	0	0
0.4	11.1	11.3
0.8	21.6	22.1
1.2	31.1	32.3
1.6	39.2	41.6
2.0	44.6	49.9
2.4	46.4	56.3
2.8	N/A	55.8

Fig. 6 - Pull-up Characteristics



V_{DD}-V_{OH} (V)	Current (mA)	
	Min.	Max.
0	0	0
0.4	-10.5	-11.0
0.8	-20.1	-21.6
1.2	-28.6	-31.8
1.6	-35.2	-41.6
2.0	-38.7	-50.7
2.4	-40.9	-59.0
2.8	N/A	-60.4

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note *1,*2,*3

AC PARAMETERS (CAS LATENCY DEPENDENT)

Parameter	Symbol		MB81N643289-50		MB81N643289-60		Unit
			Min.	Max.	Min.	Max.	
Clock Period	t_{CK}	CL = 3	5.0	9.0	6.0	10.5	ns
		CL = 2	7.5	10.5	9.0	10.5	

AC PARAMETERS (ABSOLUTE BALES)

Parameter	Notes	Symbol	MB81N643289-50		MB81N643289-60		Unit
			Min.	Max.	Min.	Max.	
Input Setup Time (Except for DQS, DM and DQs)	*4	t_{IS}	1.0	—	1.2	—	ns
Input Hold Time (Except for DQS, DM and DQs)	*4	t_{IH}	1.0	—	1.2	—	ns
Data Input Setup Time	*5	t_{DS}	0.6	—	0.7	—	ns
Data Input Hold Time	*5	t_{DH}	0.6	—	0.7	—	ns
DQS First Input Setup Time (Input Preamble Setup Time)	*4	t_{DSPRES}	0	—	0	—	ns
Input Transition Time	*6	t_T	0.1	0.8	0.1	0.9	ns
Power Down Exit and Self-refresh Exit Time	*4	t_{PDE}	3.0	—	3.6	—	ns

BASE VALUES FOR CLOCK COUNT/LATENCY (Note *7)

Parameter	Notes	Symbol	MB81N643289-50		MB81N643289-60		Unit
			Min.	Max.	Min.	Max.	
Random Cycle Time		t_{RC}	30	—	36	—	ns
Active to Page Close Time		t_{RAS}	20	55000	24	55000	ns
Page Close Single Bank to Active		t_{PCL}	10	—	12	—	ns
Page Close All Bank to Active		t_{PCAL}	20	—	24	—	ns
Auto-refresh Cycle Time	*8	t_{REFC}	60	—	72	—	ns
Auto-refresh Interval	*8	t_{REFI}	—	8.0	—	8.0	µs
Time between Refresh	*8	t_{REF}	—	32	—	32	ms
Pause Time after Power-on	*9	t_{PAUSE}	200	—	200	—	µs

AC PARAMETERS (FREQUENCY DEPENDANT) Note *10

Parameter	Notes	Symbol	Min.	Max.	Unit
Clock High Time	*4	t_{CH}	0.45 × t_{CK}	—	ns
Clock Low Time	*4	t_{CL}	0.45 × t_{CK}	—	ns
DQS Low to High Input Transition Setup Time from CLK	*4, *11	t_{DQSS}	(CL – 1 – 0.25) × t_{CK}	(CL – 1 + 0.25) × t_{CK}	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	*4	t_{DSPREH}	0.25 × t_{CK}	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	0.4 × t_{CK}	—	ns
DQS Last Low Input Hold Time (Input Postamble Hold Time)		t_{DSPST}	0.4 × t_{CK}	—	ns
DQ, DQS, DM Input Pulse Width		t_{DIPW}	0.35 × t_{CK}	—	ns
DQS Input Falling Edge to Clock Setup Time		t_{DSS}	0.2 × t_{CK} (1.5 ns (Min.))	—	ns
DQS Input Falling Edge to Clock Hold Time		t_{DSH}	0.2 × t_{CK} (1.5 ns (Min.))	—	ns
DQS Access Time from Clock	*4	t_{CKQS}	– 0.1 × t_{CK} – 0.2	0.1 × t_{CK} + 0.2	ns
Data Access Time from CLK	*4	t_{AC}	– 0.1 × t_{CK} – 0.2	0.1 × t_{CK} + 0.2	ns
Data Output Valid Time		t_{OH}	– 0.1 × t_{CK} – 0.2	0.1 × t_{CK} + 0.2	ns
DQS Output in Low-Z (Output Preamble Setup Time)	*4, *12	t_{QSLZ}	– 0.1 × t_{CK} – 0.2	—	ns
DQS First Low Output Hold Time (Output Preamble Hold Time)	*4	t_{QSPRE}	0.9 × t_{CK} – 0.2	1.1 × t_{CK} + 0.2	ns
DQS Last Low Output Hold Time (Output Postamble Hold Time)	*4, *13	t_{QSPST}	0.4 × t_{CK} – 0.2	0.6 × t_{CK} + 0.2	ns
DQS Last Low Output in High-Z from CLK to CLK	*4, *13	t_{QSHZ}	—	0.1 × t_{CK} + 0.2	ns
DQS Pulse Width		t_{QSP}	0.4 × t_{CK} – 0.2	—	ns
Data Output Valid Time from DQS		t_{QSQV}	0.4 × t_{CK} – 0.4	—	ns
Data Output skew from DQS	*5	t_{QSQ}	– 0.1 × t_{CK}	0.1 × t_{CK}	ns
DQ Output in Low-Z	*4, *12	t_{LZ}	– 0.1 × t_{CK} – 0.2	—	ns
DQ Output in High-Z	*4, *13	t_{HZ}	– 0.1 × t_{CK} – 0.2	0.1 × t_{CK} + 0.2	ns

EXAMPLE OF FREQUENCY DEPENDANT AC PARAMETERS (@ Minimum t_{CK})

Parameter		Symbol	t_{CK} = 5ns		t_{CK} = 6ns		t_{CK} = 7.5ns		t_{CK} = 9ns		t_{CK} = 10.5ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock High Time		t_{CH}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
Clock Low Time		t_{CL}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
DQS Low to High Input Transition Setup Time from CLK	CL=2	t_{DQSS}	3.8	6.3	4.5	7.5	5.7	9.4	6.8	11.3	7.9	13.2	ns
	CL=3		8.8	11.3	10.5	13.5	13.2	16.9	15.8	20.3	18.4	23.7	
DQS First Low Input Hold Time (Input Preamble Hold Time)		t_{DSPREH}	1.3	—	1.5	—	1.9	—	2.3	—	2.7	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Last Low Input Hold Time (Input Postamble Hold Time)		t_{DSPST}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQ, DQS, DM Input Pulse Width		t_{DIPW}	1.8	—	2.1	—	2.7	—	3.2	—	3.7	—	ns
DQS Input Falling Edge to Clock Setup Time		t_{DSS}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns
DQS Input Falling Edge to Clock Hold Time		t_{DSH}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns
DQS Access Time from Clock		t_{CKQS}	–0.7	0.7	–0.8	0.8	–1.0	1.0	–1.1	1.1	–1.3	1.3	ns
Data Access Time from CLK		t_{AC}	–0.7	0.7	–0.8	0.8	–1.0	1.0	–1.1	1.1	–1.3	1.3	ns
Data Output Valid Time		t_{OH}	–0.7	0.7	–0.8	0.8	–1.0	1.0	–1.1	1.1	–1.3	1.3	ns
DQS Output in Low-Z (Output Preamble Setup Time)		t_{QSLZ}	–0.7	—	–0.8	—	–1.0	—	–1.1	—	–1.3	—	ns
DQS First Low Output Hold Time (Output Preamble Hold Time)		t_{QSPRE}	4.3	5.7	5.2	6.8	6.6	8.5	7.9	10.1	9.3	11.8	ns
DQS Last Low Output Hold Time (Output Postamble Hold Time)		t_{QSPST}	1.8	3.2	2.2	3.8	2.8	4.7	3.4	5.6	4.0	6.5	ns
DQS Last Low Output in High-Z from CLK to CLK		t_{QSHZ}	—	0.7	—	0.8	—	1.0	—	1.1	—	1.3	ns
DQS Pulse Width		t_{QSP}	1.8	—	2.2	—	2.8	—	3.4	—	4.0	—	ns
Data Output Valid Time from DQS		t_{QSQV}	1.6	—	2.0	—	2.6	—	3.2	—	3.8	—	ns
Data Output skew from DQS		t_{QSQ}	–0.5	0.5	–0.6	0.6	–0.8	0.8	–0.9	0.9	–1.1	1.1	ns
DQ Output in Low-Z		t_{LZ}	–0.7	—	–0.8	—	–1.0	—	–1.1	—	–1.3	—	ns
DQ Output in High-Z		t_{HZ}	–0.7	0.7	–0.8	0.8	–1.0	1.0	–1.1	1.1	–1.3	1.3	ns

MINIMUM LATENCY - FIXED VALUES
(The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	BL = 2	BL = 4	BL = 8	Unit
$\overline{RAS}$ (ACT) to $\overline{CAS}$ (Read) Delay (minimum) (Applicable to same bank)	CL = 3	I_{RCD}	3	3	3	t_{CK}
	CL = 2		2	2	2	t_{CK}
$\overline{RAS}$ (ACT) to $\overline{CAS}$ (Write) Delay (minimum) (Applicable to same bank)	CL = 3	I_{RCDW}	1	1	1	t_{CK}
	CL = 2		1	1	1	t_{CK}
Write Command to Read Command Delay Time (Applicable to other bank in page open)	CL = 3	I_{WRD}	2	3	5	t_{CK}
	CL = 2		2	3	5	t_{CK}
Read with Auto-close to Next Command Input Delay (Applicable to same bank)	CL = 3	I_{RDA}	3	4	6	t_{CK}
	CL = 2		3	4	6	t_{CK}
Write with Auto-close Command to Next Command Input Delay (Applicable to same bank)	CL = 3	I_{WAL}	7	8	10	t_{CK}
	CL = 2		6	7	9	t_{CK}
Read to Page Close Command Delay (Applicable to same bank)	CL = 3	I_{RPL}	1	2	4	t_{CK}
	CL = 2		1	2	4	t_{CK}
Write to Page Close Command Delay (Applicable to same bank)	CL = 3	I_{WPL}	5	6	8	t_{CK}
	CL = 2		4	5	7	t_{CK}
$\overline{CAS}$ to $\overline{CAS}$ Delay (Applicable to same bank)	CL = 3	I_{CCD}	1	2	4	t_{CK}
	CL = 2		1	2	4	t_{CK}
$\overline{CAS}$ to $\overline{CAS}$ Bank Delay (Applicable to other bank)	CL = 3	I_{CBD}	1	2	4	t_{CK}
	CL = 2		1	2	4	t_{CK}
Read Command to Write Command Lead Time (Applicable to any bank in page open)	CL = 3	I_{RWL}	3	4	6	t_{CK}
	CL = 2		3	4	6	t_{CK}
Write Command to Read Command Lead time (Applicable to same bank)	CL = 3	I_{WRL}	5	6	8	t_{CK}
	CL = 2		4	5	7	t_{CK}
Mode Register Set Cycle Time	CL = 3	I_{RSC}	2	2	2	t_{CK}
	CL = 2		2	2	2	t_{CK}
Power Down Exit to Next Command Input Delay (Minimum)	CL = 3	I_{PDEX}	2	2	2	t_{CK}
	CL = 2		2	2	2	t_{CK}
Active Command to Next Active (Applicable to other bank)	CL = 3	I_{RRD}	1	1	1	t_{CK}
	CL = 2		1	1	1	t_{CK}
$\overline{PD}$ Low to Command/Address Input Inactive	CL = 3	I_{PD}	1	1	1	t_{CK}
	CL = 2		1	1	1	t_{CK}
Clock Lock-on Time *14	$t_{CK} \leq 7.5$ ns	I_{LOCK}	400	400	400	t_{CK}
	7.5 to $t_{CK(max)}$		630	630	630	t_{CK}

Notes: *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure and stable clock input with constant clock period and with 50% duty cycle.

*2. Access Times assume input slew rate of 1ns/volt between V_{REF}+0.35V to V_{REF}-0.35V, where V_{REF} is V_{DDQ}/2, with 1 resistor and 1 capacitor load conditions. Refer to AC TEST LOAD CIRCUIT.

*3. V_{REF} = 1.25V is a typical reference level for measuring timing of input signals.
Transition times are measured between V_{IH} (min) and V_{IL} (Max.) unless otherwise noted.
Refer to AC TEST CONDITIONS.

*4. This parameter is measured from the cross point of CLK and $\overline{CLK}$ input.

*5. This parameter is measured from signal transition point of DQS input crossing V_{REF} level.

*6. t_T is defined as the transition time between $V_{IH\ (AC)}$(min) and $V_{IL\ (AC)}$(Max.).

*7. All base values are measured from the cross point of the rising edge of CLK and falling edge of $\overline{CLK}$ at the command input to the cross point of same clock input condition for the next command input.
All clock counts (= latency) are calculated by a simple formula:

clock count equals base value divided by clock period (round off to a whole number).

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \text{ (Round off a whole number)}$$

*8. Total of 4096 REF command must be issued within t_{REF}(Max.). t_{REFI} is a reference value for distributed refresh and specifies the time between one REF command to next REF command except for a condition where $\overline{PD}$ = L during Self-Refresh mode.

*9. Specified when the clock input is started on the condition of the stable supply voltage.

*10. This parameter is scalable by actual clock period (t_{CK}) and affected by an abrupt change of duty cycle, jitters on clock input, T_A and level of V_{DD} and V_{DDQ}.
The internal DLL circuit can adjust delay time against the change of following condition :
$T_A \leq 0.1$ °C / 20 ns,
$V_{DD} \leq 1$ mV / 10 ns,
$V_{DDQ} \leq 1$ mV / 10 ns,
if change rate is bigger than these values, frequency dependent AC parameters affected by DLL jitters.

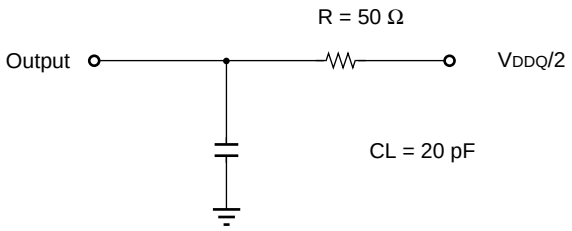
*11. More than 2 signal edge of DQS_0 to DQS_3 should not be input within 1 clock (t_{CK}) cycle.

*12. Low-Z (Low Impedance State) is specified and measured at V_{DD} / 2 ± 200 mV from steady state.

*13. t_{HZ} are specified where output buffer is no longer driven.

*14. Clock period must satisfy specified t_{CK} and it must be stable.
Applicable also if device operating conditions such as supply voltages, case temperature, and/or clock frequency (t_{CK} difference must be 0.2 ns or less) is changed during any operation.

Fig. 7 - EXAMPLE OF AC TEST LOAD CIRCUIT (2.5 V CMOS Source Termination)



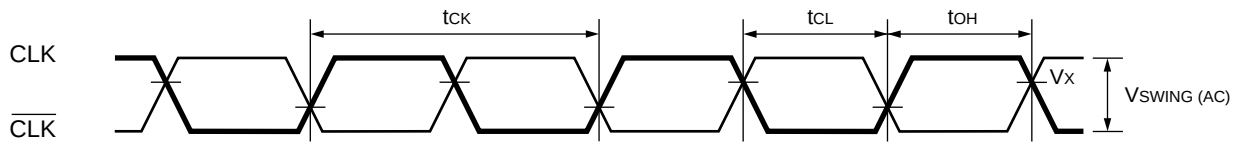
Note: By adding appropriate correlation factors to the test conditions, t_{AC} and t_{OH} measured when the Output is coupled to the Output Load Circuit are within specifications.

AC TEST CONDITIONS

Parameters	Symbol	Value	Unit
Single-end Input			
Input High Level	V_{IH}	V_{REF}+0.35	V
Input Low Level	V_{IL}	V_{REF}-0.35	V
Input Reference Level	V_{REF}	V_{DDQ}/2	V
Input Slew Rate	SLEW	1.0	V/ns
Differential Input (CLK and $\overline{CLK}$)			
Input Reference Level	Vr	$V_{x(AC)}$*	V
Input Level	V_{SWING}	0.7	V
Input Slew Rate	SLEW	1.0	V/ns

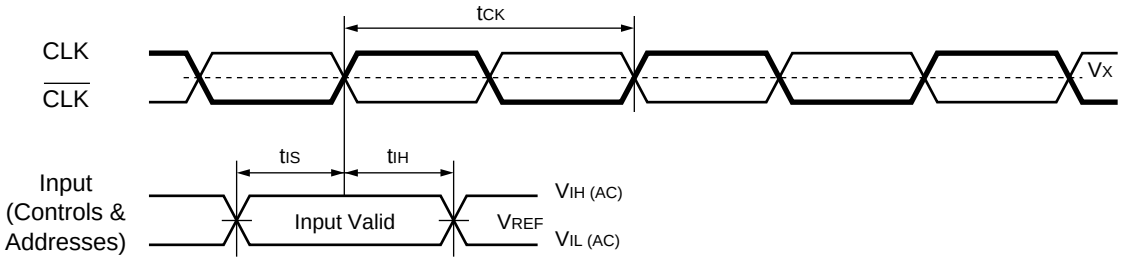
*: V_X means the actual cross point between CLK and $\overline{CLK}$ input.

Fig. 8 - AC TIMING of CLK & $\overline{CLK}$



Note: Reference level for AC timings of clock are the cross point of CLK and $\overline{CLK}$ as specified in V_X.

Fig. 9 - AC TIMING of Command Input & Address



Note: The cross point of CLK and $\overline{CLK}$ (V_X) is used for command and address input.
The reference level of single ended input is V_{REF}.

Fig. 10 - AC TIMING of Write Mode (Data Strobe, Write Data and Data Mask Input)

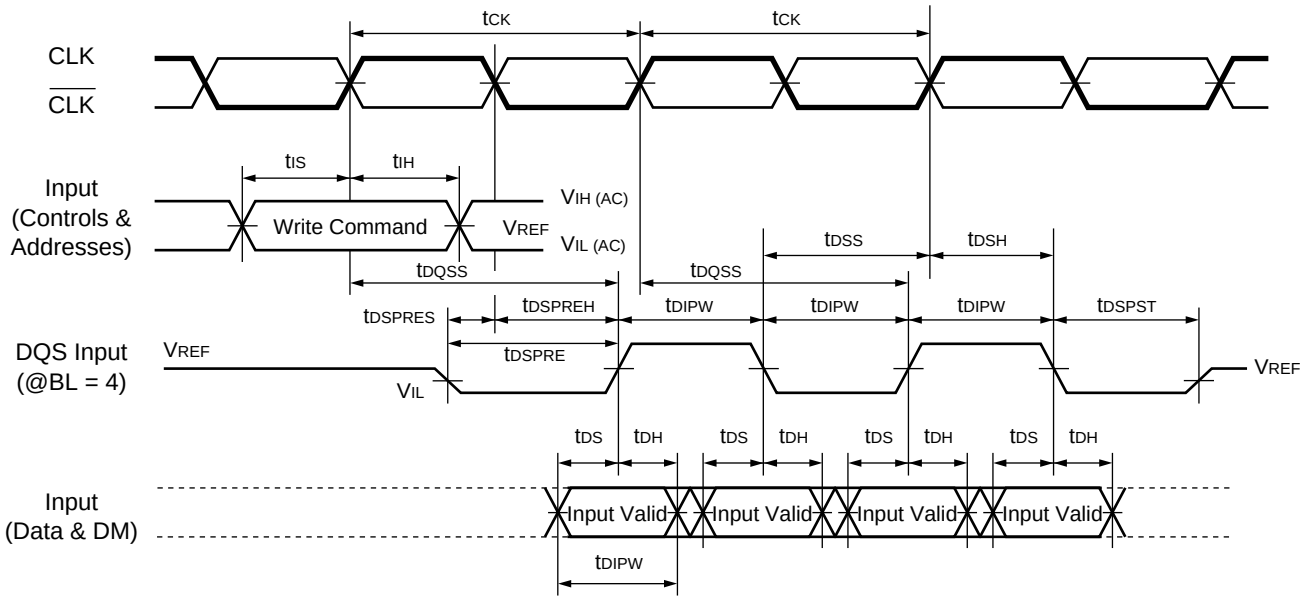
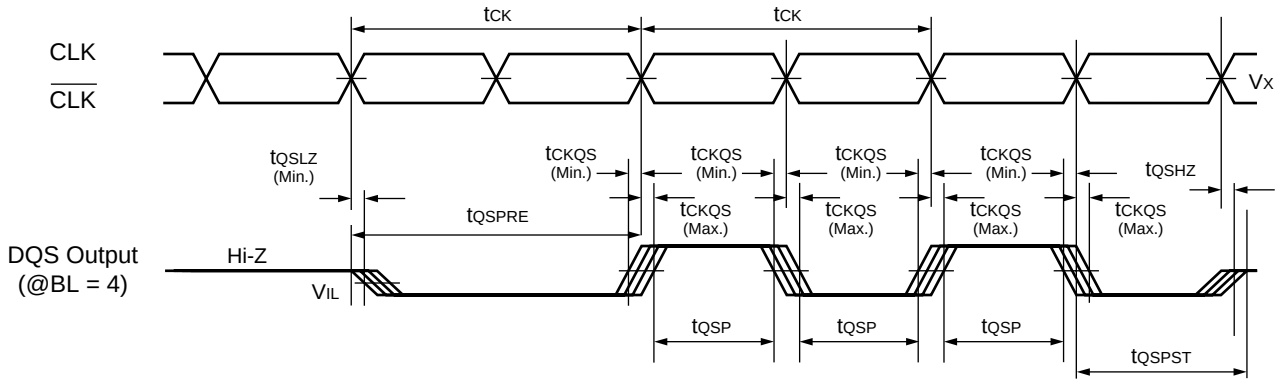
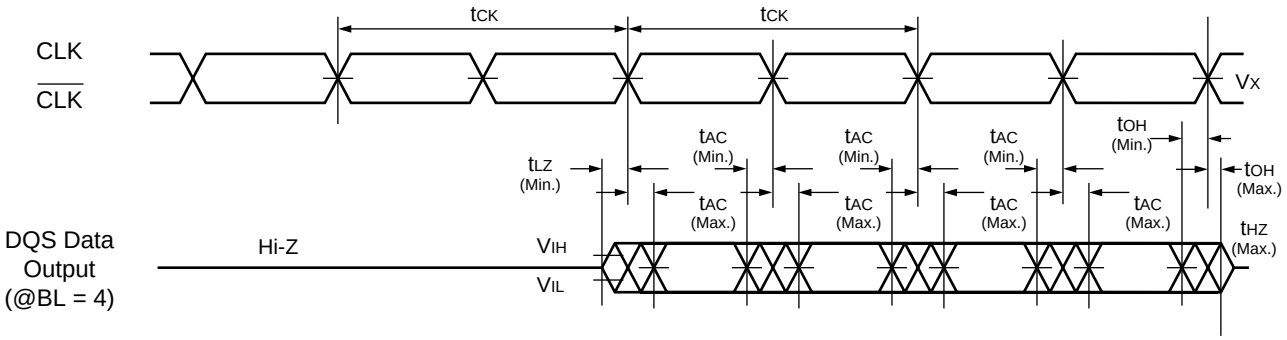


Fig. 11 - AC TIMING of Read Mode (Clock to DQS Output Delay Time)



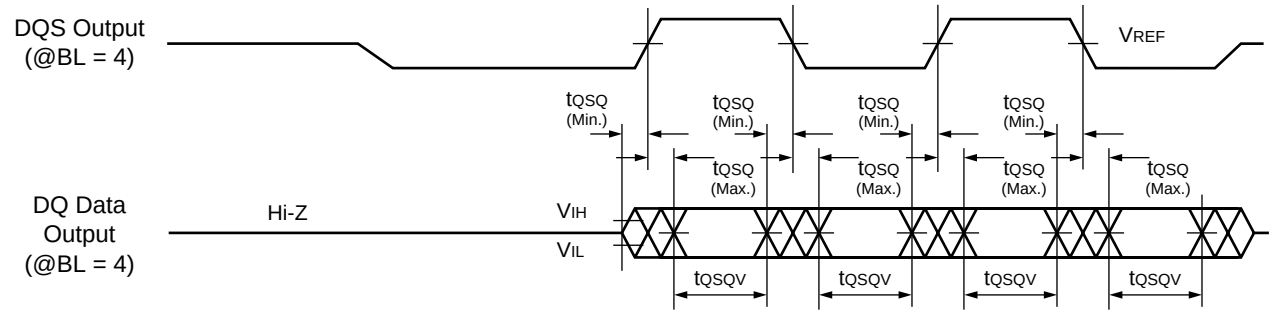
Note: DQS Access time (t_{QSCK}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{QSPST} and t_{QSHZ} specification is defined at where output buffer is no longer driven.

Fig. 12 - AC TIMING of Read Mode (Clock to Data Output Delay Time)



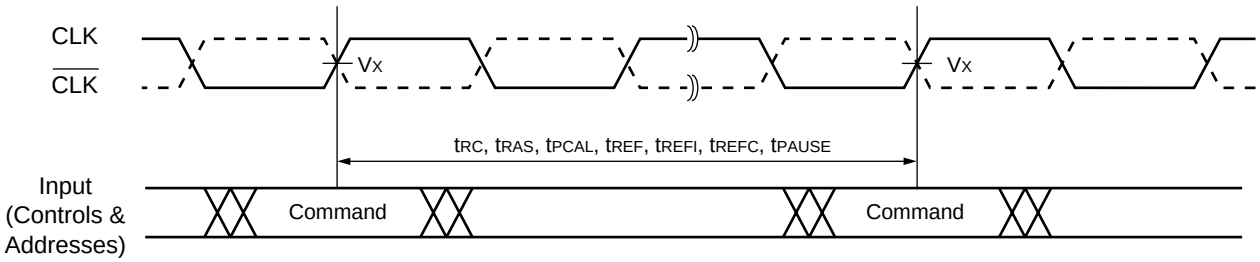
Note: Access time (t_{AC}) is measured from the cross point of clock (V_X) and V_{REF}.
The end of t_{HZ} specification is defined at where output buffer is no longer driven.

Fig. 13 - AC TIMING of Read Mode (DQS Output to Data Output Delay Time)



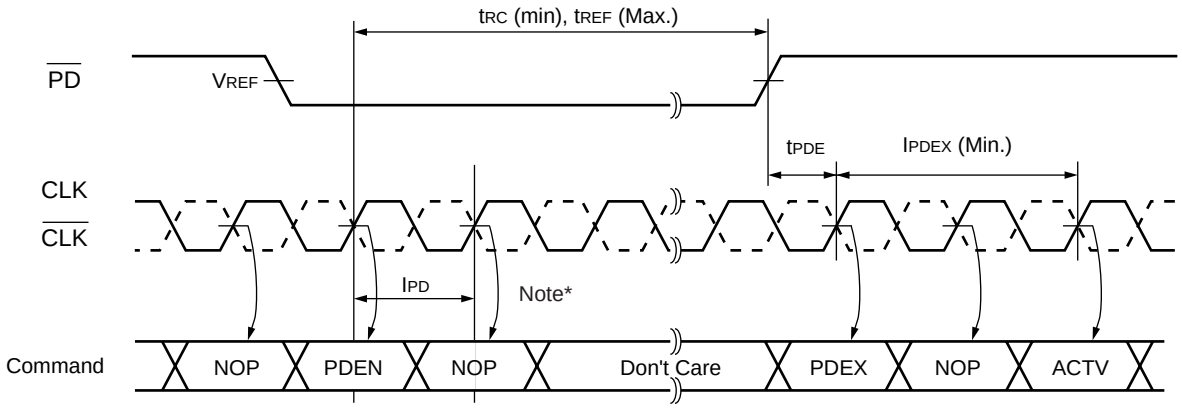
Note: DQS Output Edge to Data Output Edge Skew Time (t_{QSQ}) is measured from $V_{DDQ}/2$ to $V_{DDQ}/2$.

Fig. 14 - AC TIMING, PULSE WIDTH



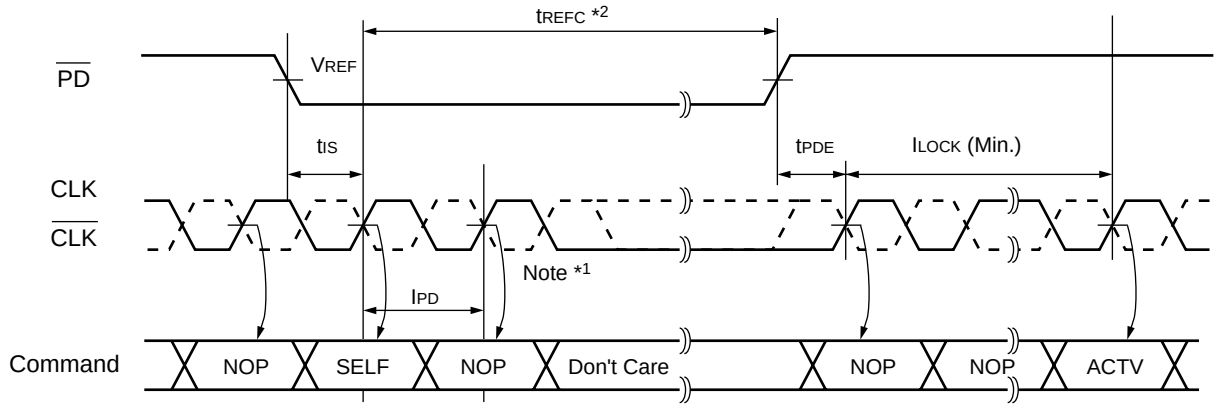
Note: All parameters listed above are measured from the cross point at rising edge of the CLK and falling edge of CLK of one command input to next command input.

Fig. 15 - AC TIMING of Power Down Mode



Note*: Minimum 2 clock cycles is required for complete power down on clock buffer.

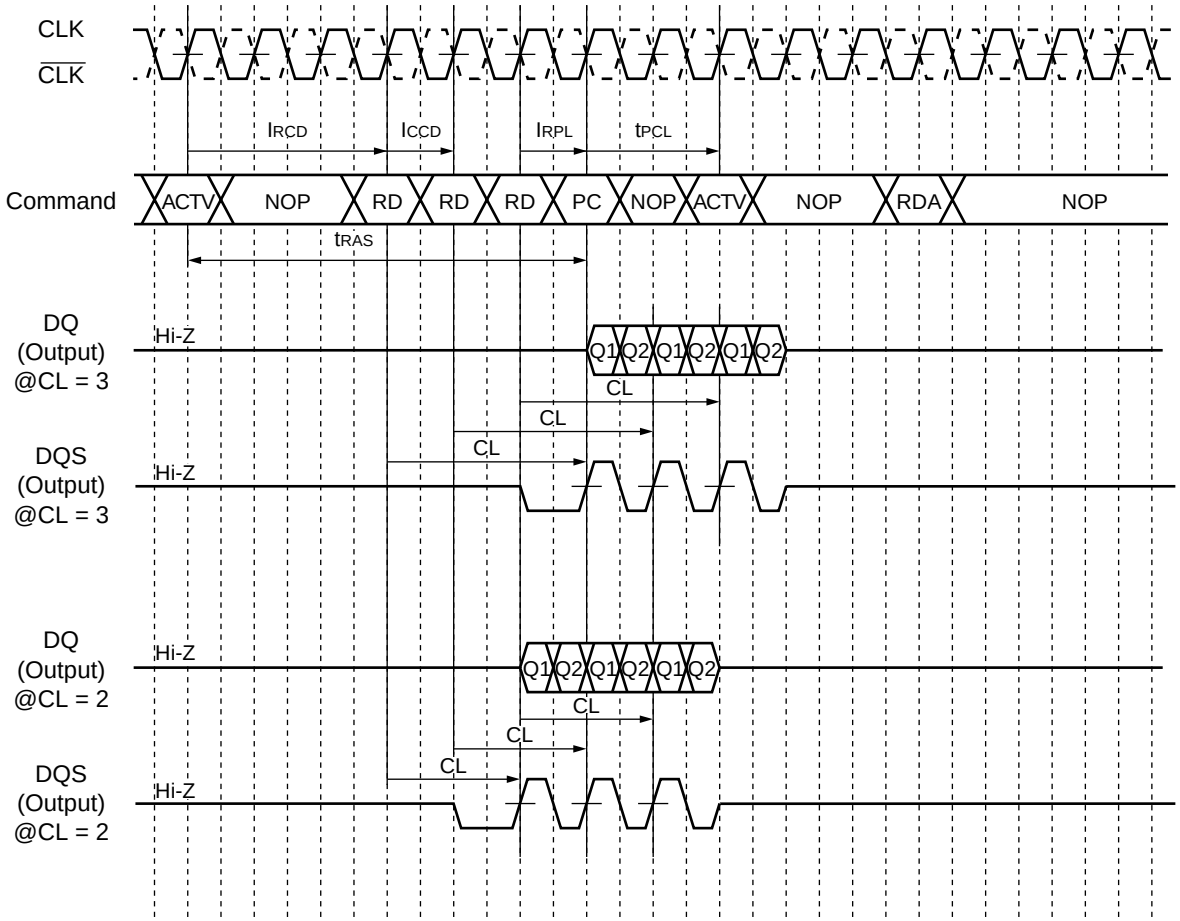
Fig. 16 - AC TIMING of Self-refresh Mode



Note: 1. Minimum 2 clock cycles is required for complete power down on clock buffer.
2. PD must maintain High level and clock must be provided during the I_{LOCK} period. I_{LOCK} must be satisfied before any command input.

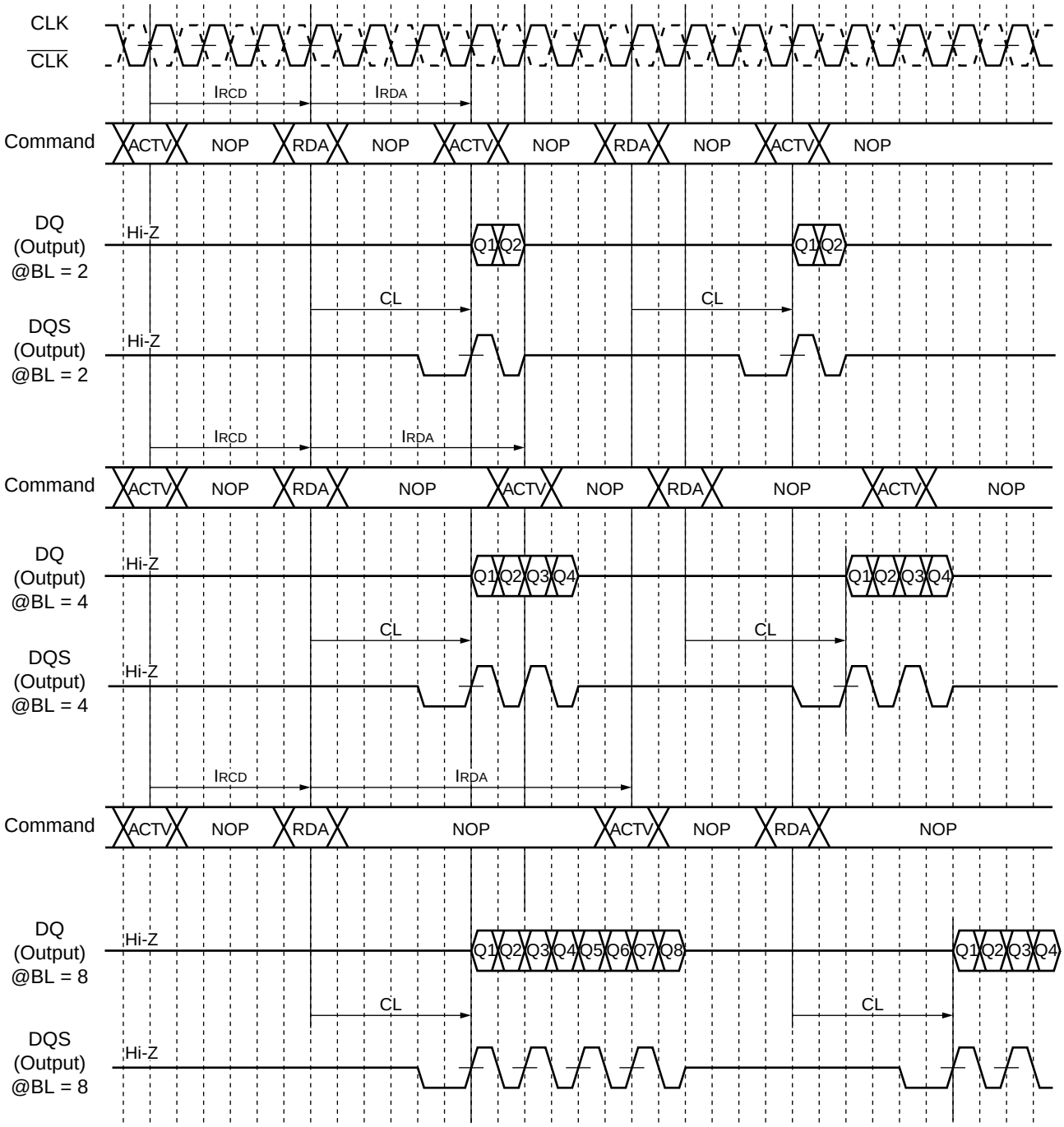
■ TIMING DIAGRAMS

TIMING DIAGRAM - 1: PAGE MODE READ
(Timing assumes Same Bank Access)



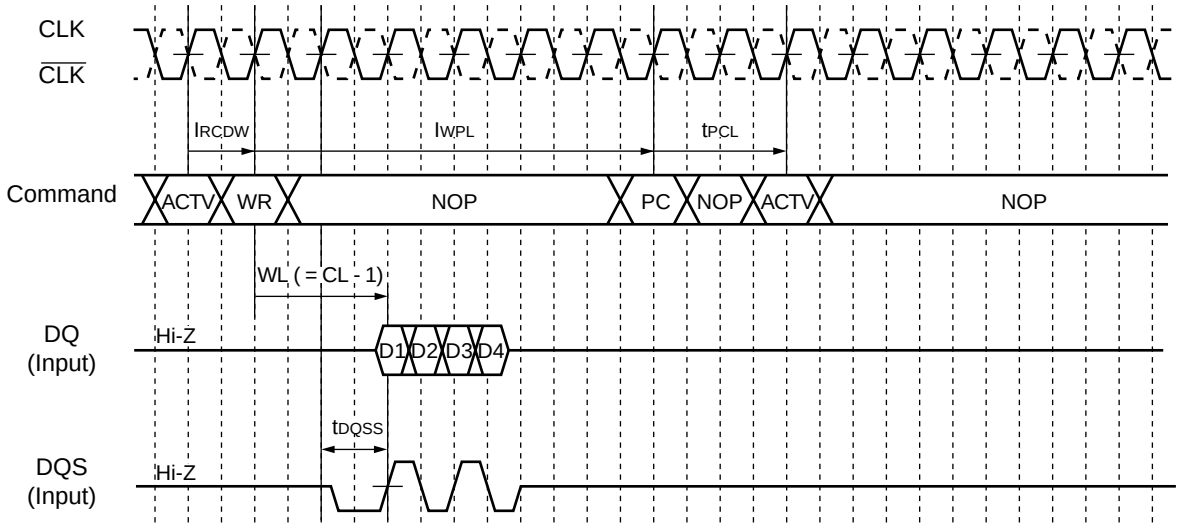
Notes: 1. I_{RCD} :Latency of ACTV to Read command input delay.
2. I_{CCD} :Latency of $\overline{CAS}$ to $\overline{CAS}$ delay (Page cycle time).
3. I_{RPL} :Latency of Read command to Page Close lead time.
4. t_{PCL} :Page Close to next command lead time.

TIMING DIAGRAM - 2: RANDOM READ WITH AUTO-CLOSE
(Timing assumes CL=3, Same Bank Access)



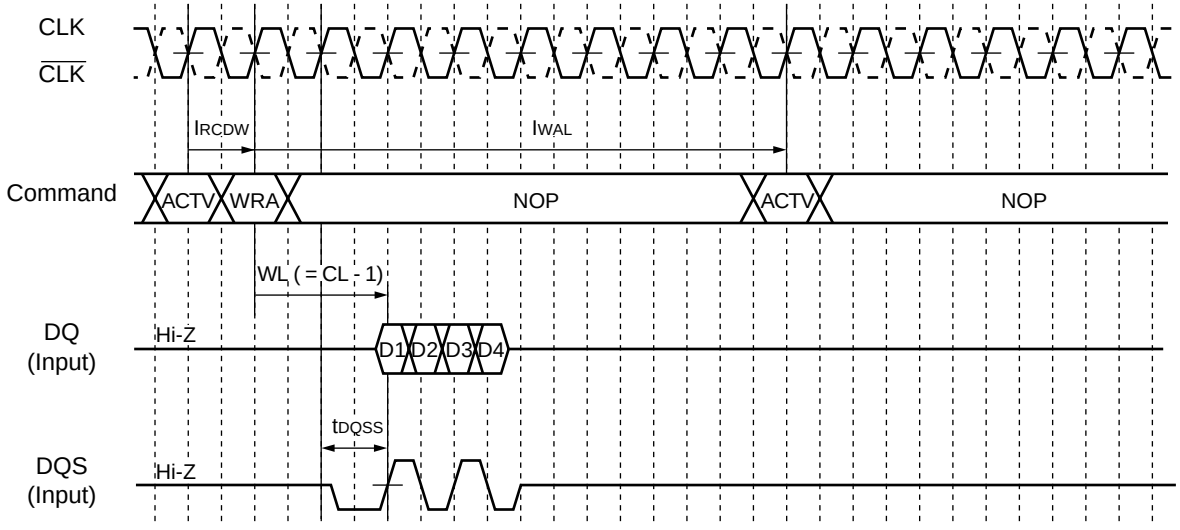
Note: I_{RDA} : Latency of Read with Auto Close command.

TIMING DIAGRAM - 3: RANDOM WRITE
(Timing assumes CL=3, BL=4, Same Bank Access)



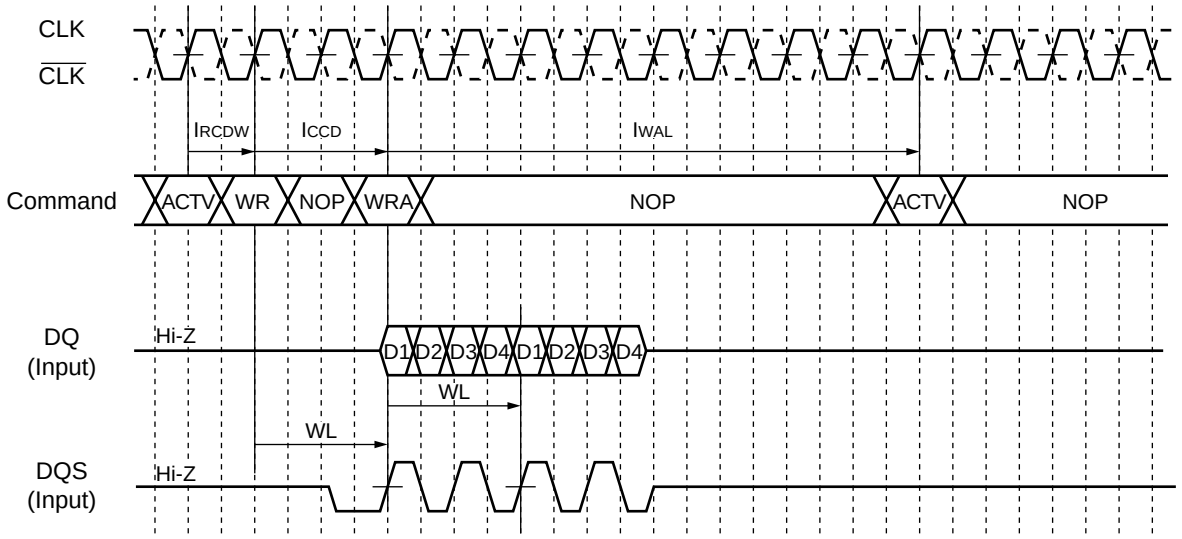
Notes: 1 l_{RCDW} : Latency of ACTV to Write command input delay is minimum 1 clock.
2 l_{WPL} : Latency of Write command to Auto Close command lead time.

TIMING DIAGRAM - 4: RANDOM WRITE WITH AUTO-CLOSE
(Timing assumes CL=3, BL=4, Same Bank Access)

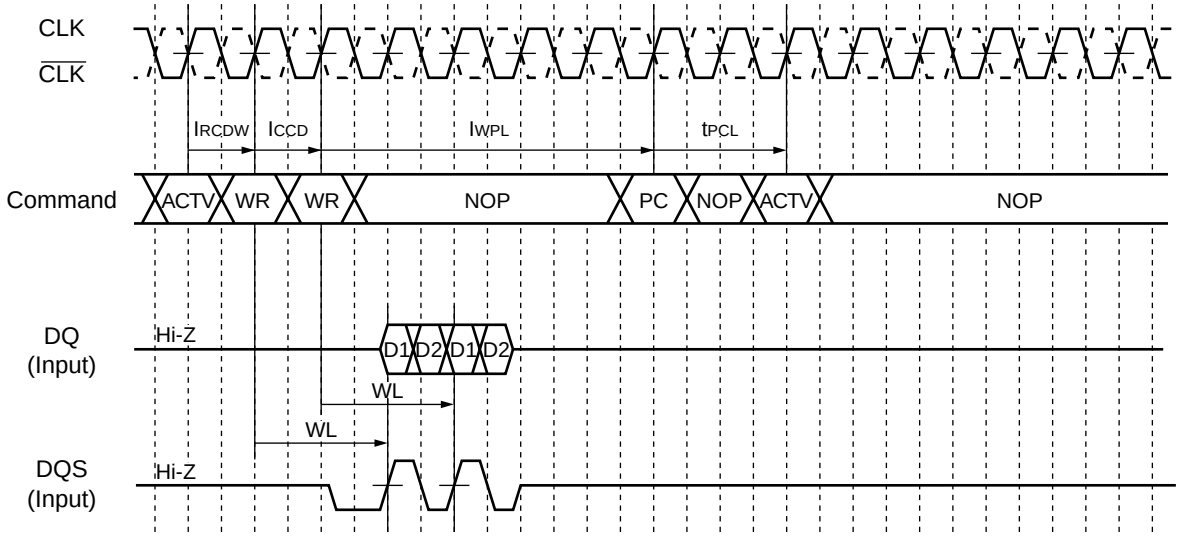


Note: l_{WAL} : Latency Write with Auto Close command to next Active command lead time.

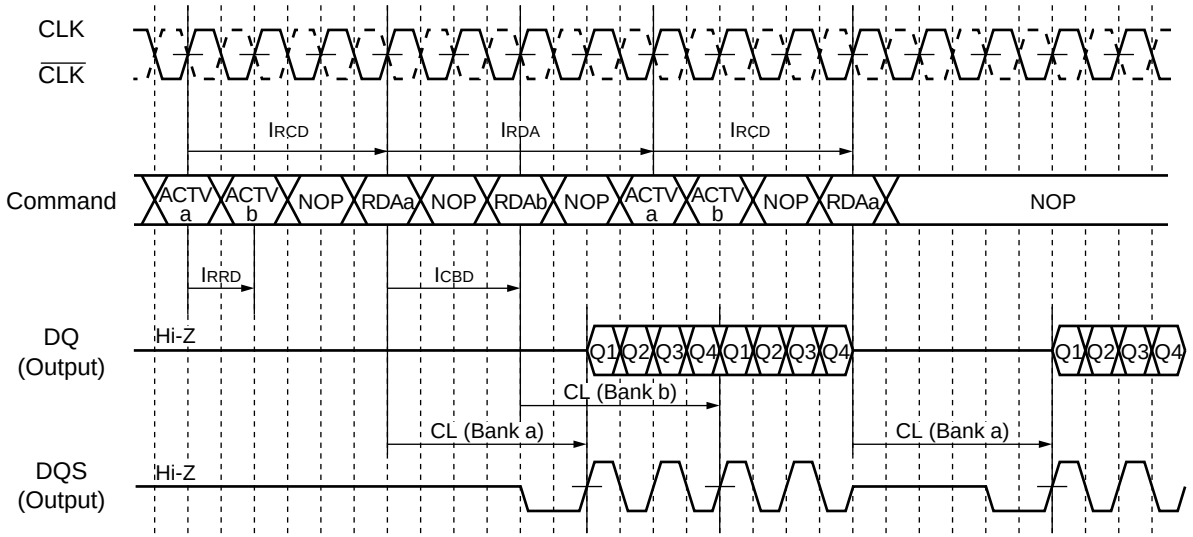
TIMING DIAGRAM - 5: PAGE MODE WRITE
(Timing assumes CL=3, BL=4, Same Bank Access)



TIMING DIAGRAM - 6: PAGE MODE WRITE
(Timing assumes CL=3, BL=2, Same Bank Access)

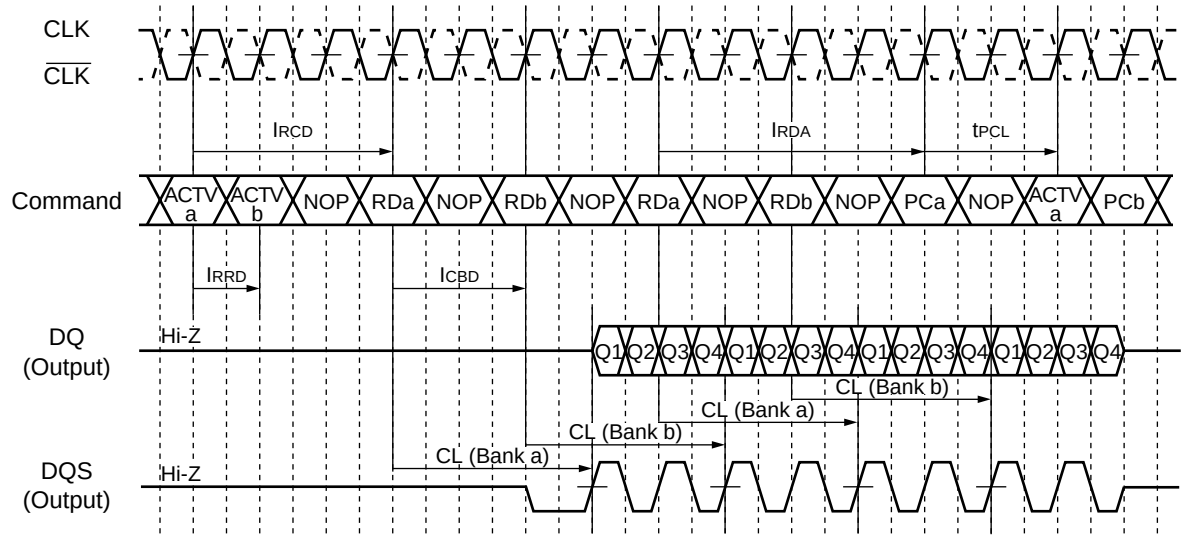


TIMING DIAGRAM - 7: RANDOM READ
(Timing assumes CL=3, BL=4, Multiple Bank Access)

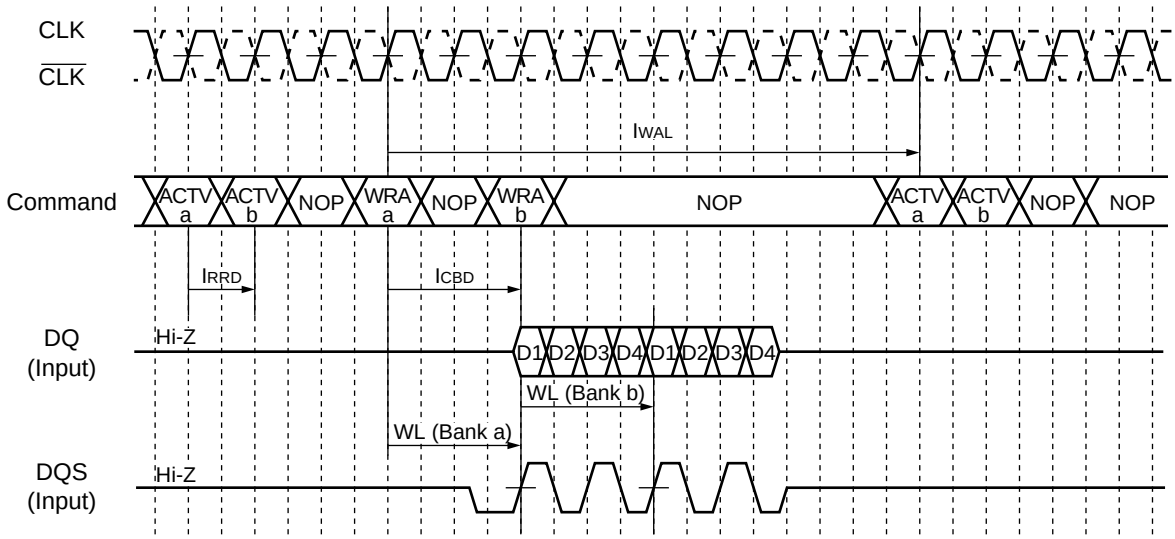


Notes: 1 I_{CBD} : Latency of $\overline{CAS}$ to $\overline{CAS}$ Bank Delay
2 I_{RRD} : Latency of Active command to next Active command.

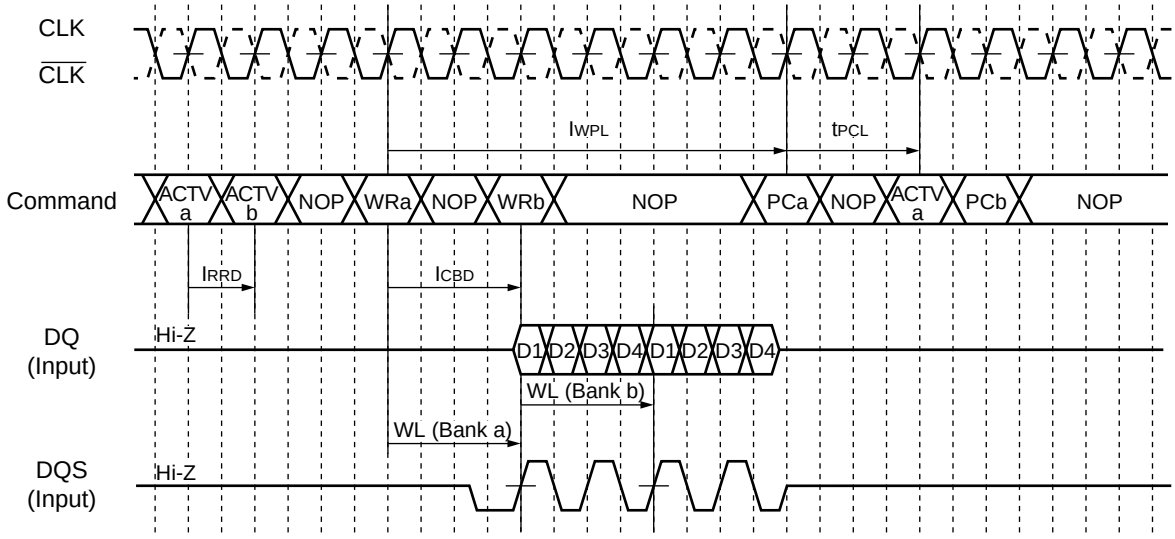
TIMING DIAGRAM - 8: RANDOM READ
(Timing assume CL=3, BL=4, Multiple Bank Access)



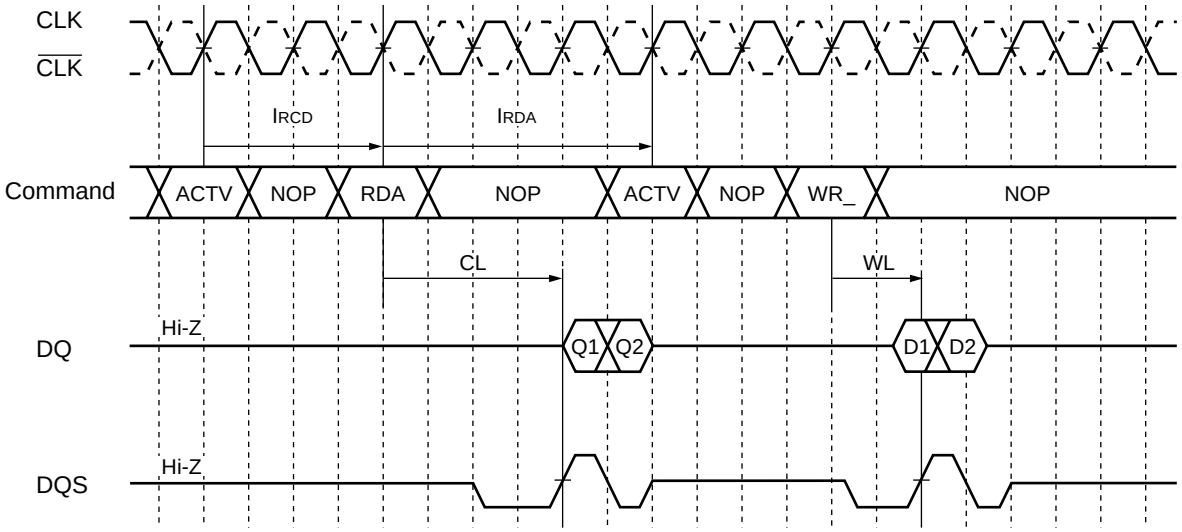
TIMING DIAGRAM - 9: RANDOM WRITE
(Timing assumes CL=3, BL=4, Multiple Bank Access)



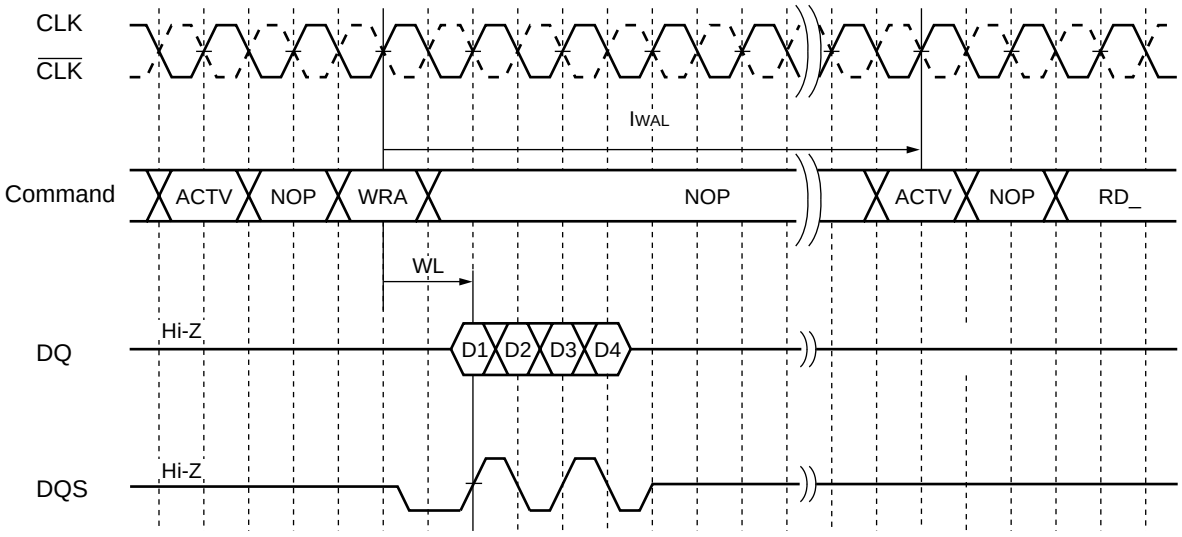
TIMING DIAGRAM - 10: RANDOM WRITE
(Timing assumes CL=3, BL=4, Multiple Bank Access)



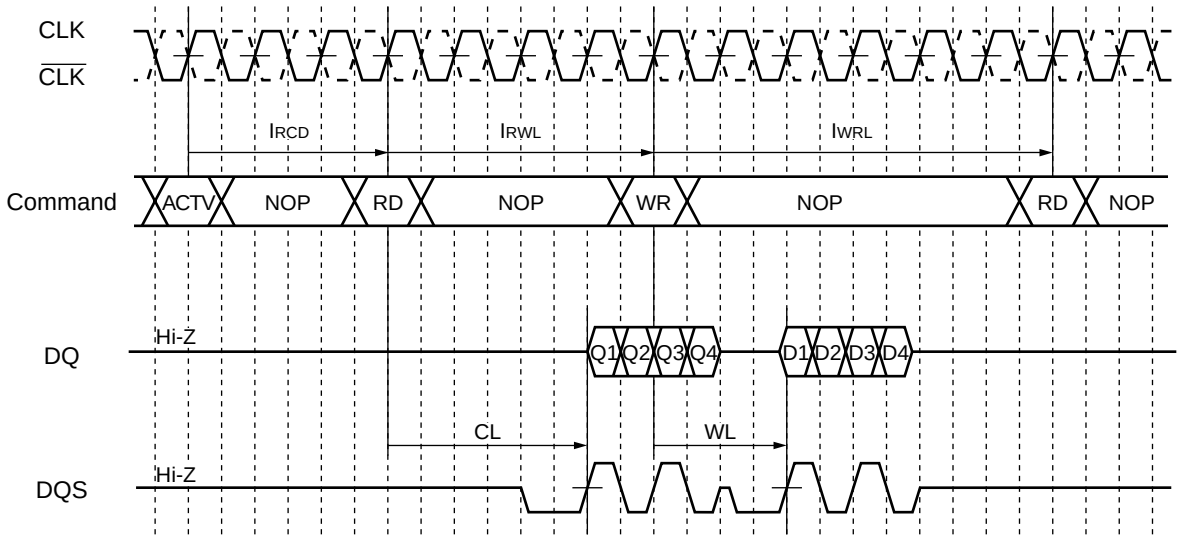
TIMING DIAGRAM - 11: RANDOM READ / WRITE
(Timing assumes CL=2, BL=2, Same Bank Access)



TIMING DIAGRAM - 12: RANDOM READ / WRITE
(Timing assumes CL=2, BL=4, Same Bank Access)

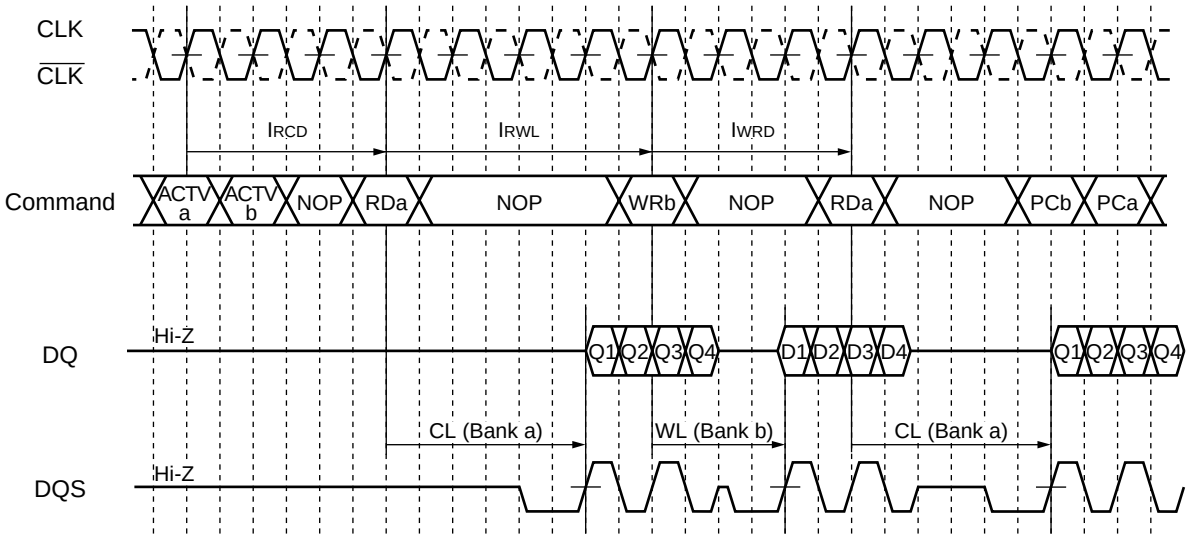


TIMING DIAGRAM - 13: PAGE MODE READ / WRITE
(Timing assumes CL=3, BL=4, Same Bank Access)



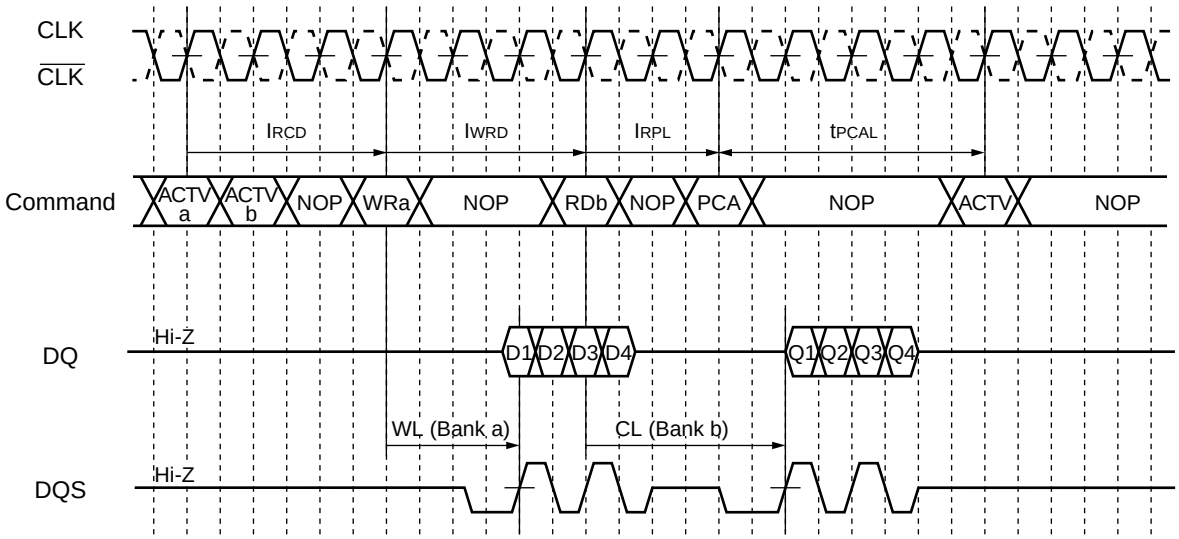
Notes: 1. I_{RWL} : Latency of Read to Write command.
2. I_{WRL} : Latency of Read to Write command in same bank.

TIMING DIAGRAM - 14: PAGE MODE READ / WRITE
(Timing assumes CL=3, BL=4, Multiple Bank Access)

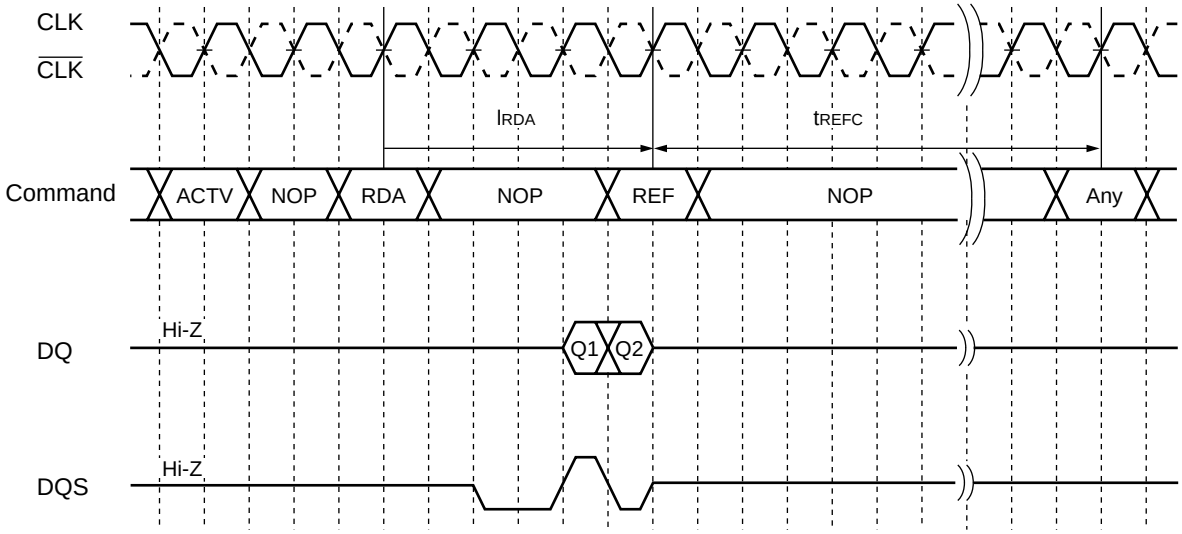


Notes: 1. I_{WRD} : Latency of Write to Read command in different bank.
2. Data Strobe Input must be applied after or before output of DQS is in High-Z.

TIMIN DIAGRAM - 15: PAGE MODE READ / WRITE
(Timing assumes CL=3, BL=4, Multiple Bank Access)

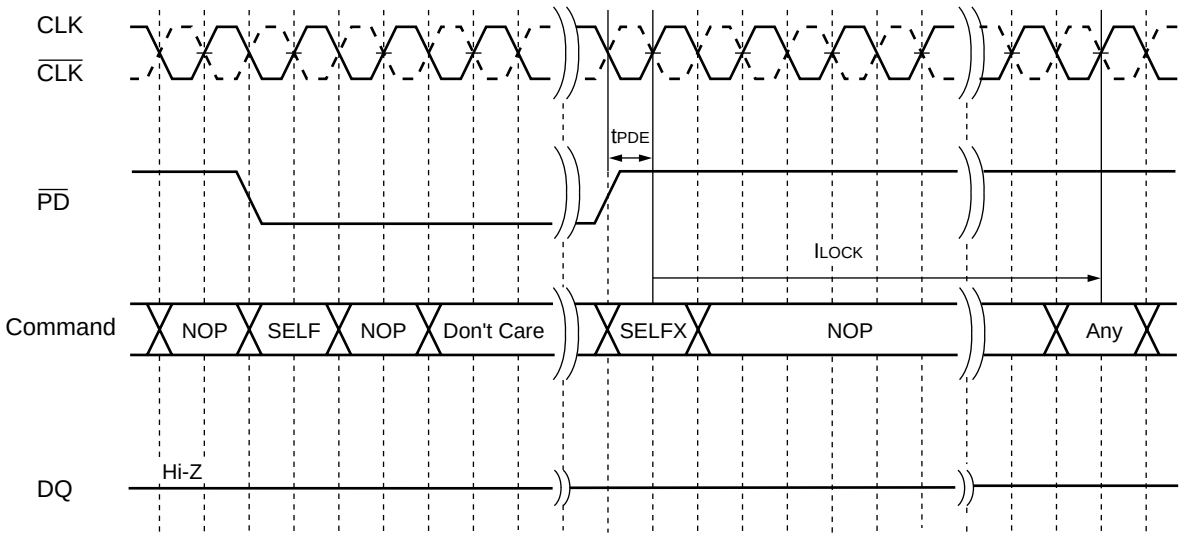


TIMING DIAGRAM - 16: AUTO-REFRESH
(Timing assumes CL=2, BL=2)

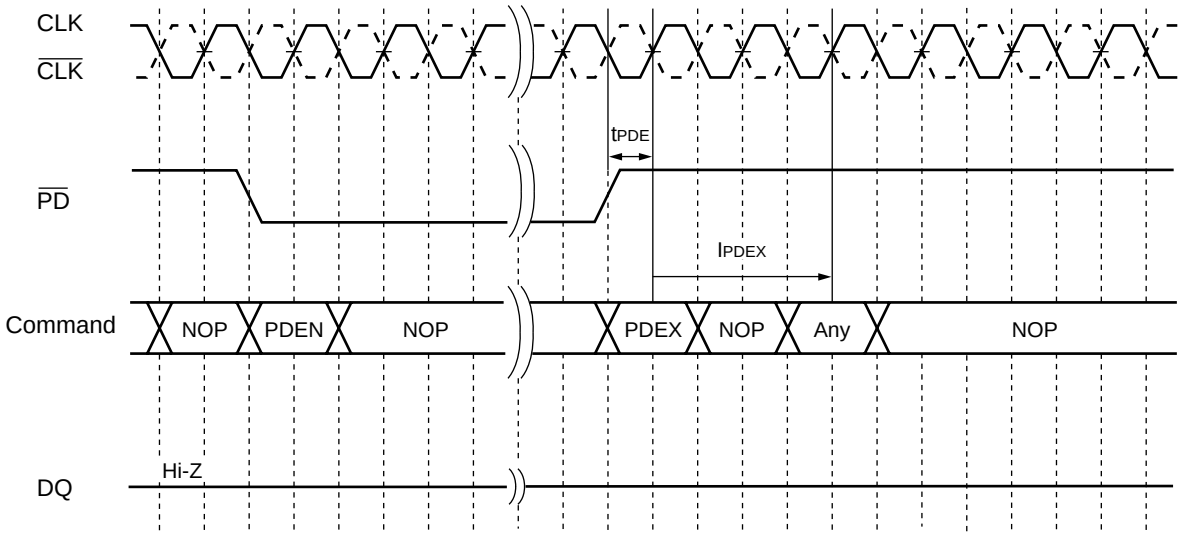


Note: Refresh command can be issued all banks has been closed.

TIMING DIAGRAM - 17: SELF-REFRESH
(Timing assumes CL=2)

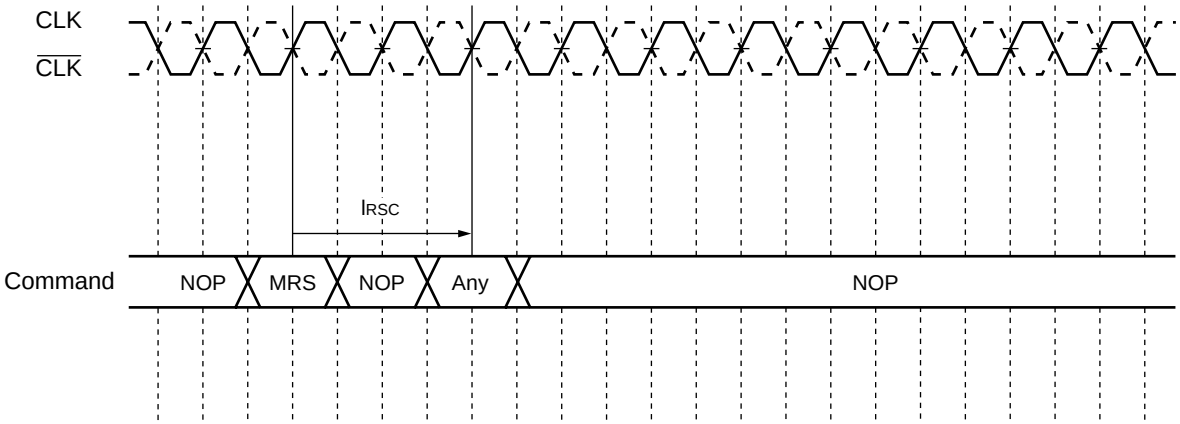


TIMING DIAGRAM - 18: POWER DOWN
(Timing assumes any CL)



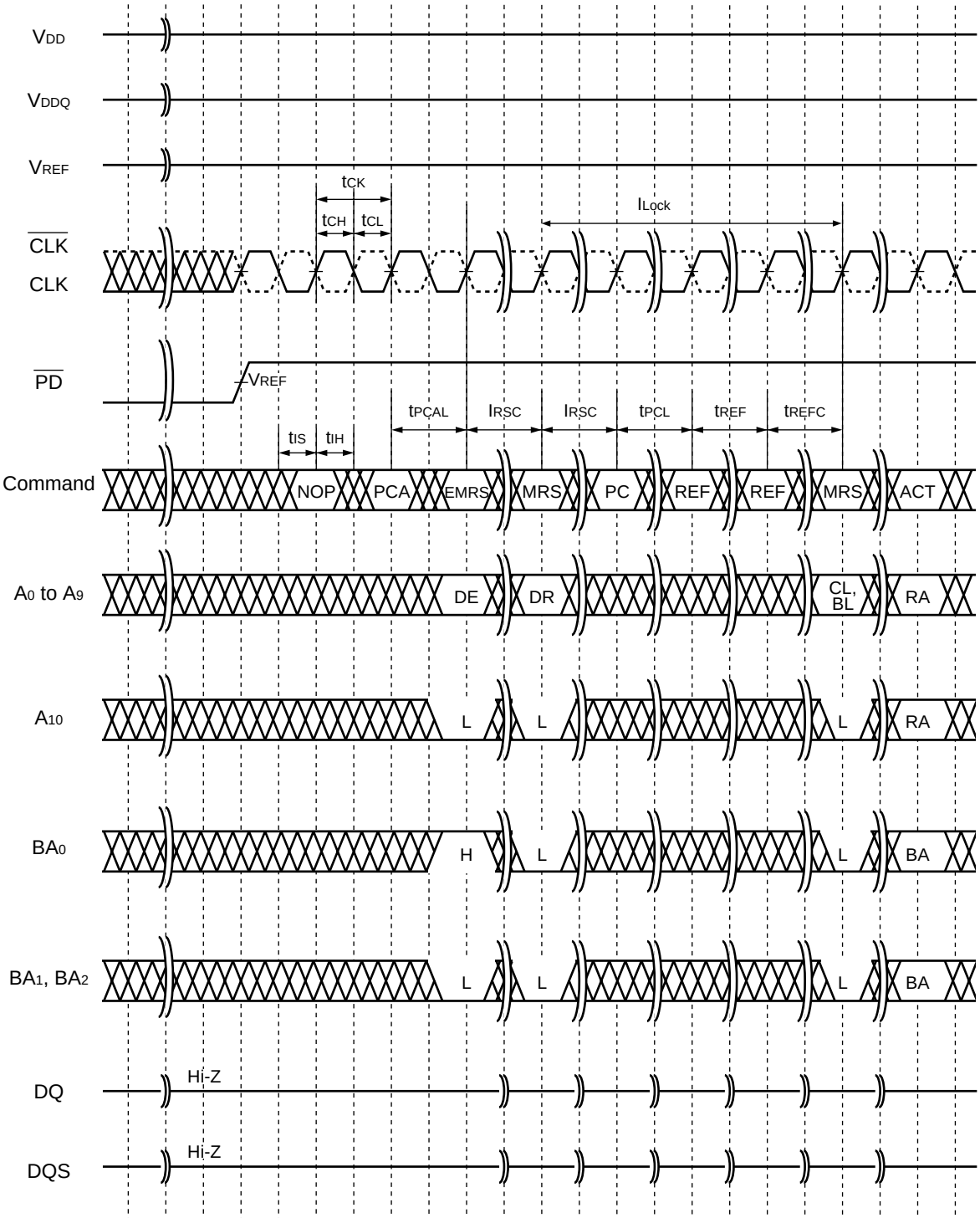
Note: I_{PDEX} : Latency of Power Down Exit to next command input delay.
t_{REF} must be satisfied for burst refresh and t_{AREF} must be satisfied for distributed refresh.

TIMING DIAGRAM - 19: MODE REGISTER SET
(Timing assumes any CL and frequency)



Note: l_{RSC} : Latency of Mode Register Set to next command lead time.

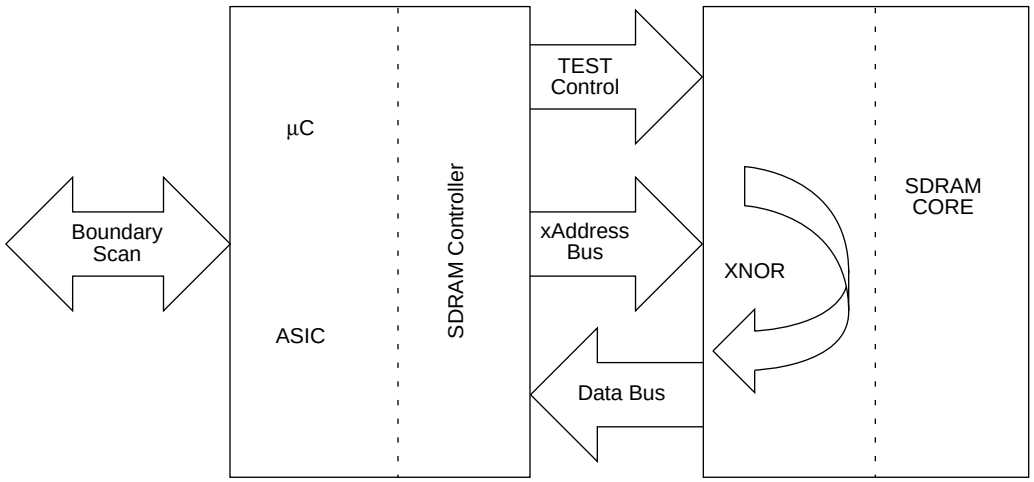
TIMING DIAGRAM - 20: POWER-UP INITIALIZATION



■ SCITT TEST MODE

ABOUT SCITT

SCITT (Static Component Interconnection Test Technology) is an XNOR circuit based test technology that is used for testing interconnection between SDRAM and SDRAM controller on the printed circuit boards. SCITT provides inexpensive board level test mode in combination with boundary-scan. The basic idea is simple, consider all output of SDRAM as output of XNOR circuit and each output pin has a unique mapping on the input of SDRAM. The ideal schematic block diagram is as shown below.



TEST Control : $\overline{CAS}$, $\overline{CS}$, $\overline{PD}$
xAddress Bus : A_0 to A_{10}, BA_0 to BA_2, $\overline{RAS}$, DM_0 to DM_3, CLK, $\overline{CLK}$, $\overline{WE}$
Data Bus : DQ_0 to DQ_{31}, DQS_0 to DQS_3

It is static and provides easy test pattern that result in a high diagnostic resolution for detecting all open/short faults.

SCITT TEST SEQUENCE

The followings are the SCITT test sequence. SCITT Test can be executed after power-on and prior to Precharge command in "■FUNCTIONAL DESCRIPTION POWER-UP INITIALIZATION". Once Precharge command is issued to SDRAM, it never get back to SCITT Test Mode during regular operation unless reset power supply for the purpose of a fail-safe way in get in and out of test mode.

1. Maintain all input signals (except CLK,$\overline{CLK}$) to be Low state (or at least $\overline{PD}$ to be Low state) and maintain CLK and $\overline{CLK}$ to be complementary state (CLK = H,$\overline{CLK}$ = L or CLK = L,$\overline{CLK}$ = H).
2. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins.
3. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF}.
4. Apply V_{REF}.
5. Maintain stable power for a minimum of 100µs.
6. Enter SCITT test mode.
7. Execute SCITT test.
8. Exit from SCITT mode.

It is required to follow Power On Sequence to execute read or write operation.

9. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200µs.
10. After the minimum of 200µs stable power and clock, apply NOP condition and take $\overline{PD}$ to be High state.
11. Issue Page Close All Banks (PCA) command or Page Close Single Bank (PC) command to every banks.
12. Issue EMRS to enable DLL, DE = Low.
13. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for t_{LOCK}*1 period is required to lock the DLL.
14. Apply minimum of two Auto-refresh command (REF).*2
15. Program the mode register by Mode Register Set command (MRS) with DR = Low.*2

The 6,7,8 steps define the SCITT mode available. It is possible to skip these steps if necessary (Refer to "■ FUNCTIONAL DESCRIPTION POWER-UP INITIALIZATION").

Notes: *1. The t_{LOCK} depends on operating clock period. The t_{LOCK} is counted from "DLL Reset" at step-13 to any command input at step-15.

*2. The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle.

COMMAND TRUTH TABLE Note *1

	Control			Input						Output	
	$\overline{CAS}$	$\overline{CS}$	$\overline{PD}$	$\overline{WE}$	$\overline{RAS}$	A_0 to A_{10}, BA_0 to BA_2	DM_0 to DM_3	CLK	$\overline{CLK}$	DQ_0 to DQ_{31}	DQS_0 to DQS_3
SCITT mode entry	H→L *2	L	L	X	X	X	X	H L	L H	X	X
SCITT mode exit	L→H *3	H *5	L *5	X	X	X	X	X	X	X	X
SCITT mode output enable *4	L	L	H	V	V	V	V	V	V	V	V

Notes: *1. L = Logic Low, H = Logic High, V = Valid, X = either L or H
*2.The SCITT mode entry command assumes the first $\overline{CAS}$ falling edge with $\overline{CS}$ = $\overline{PD}$ = L and CLK, $\overline{CLK}$ signals are complementary after power on.
*3. The SCITT mode exit command assumes the first $\overline{CAS}$ rising edge after the test mode entry.
*4. Refer the test code table.
*5. $\overline{CS}$ = H or $\overline{PD}$ = L is necessary to disable outputs in SCITT mode exit.

TEST CODE TABLE

DQ_0 to DQ_{31} and DQS_0 to DQS_3 output data is static and is determined by following logic during the SCITT mode operation.

$DQ_0 = \overline{RAS}$ xnor A_0
$DQ_1 = \overline{RAS}$ xnor A_1
$DQ_2 = \overline{RAS}$ xnor A_2
$DQ_3 = \overline{RAS}$ xnor A_3
$DQ_4 = \overline{RAS}$ xnor A_4
$DQ_5 = \overline{RAS}$ xnor A_5
$DQ_6 = \overline{RAS}$ xnor A_6
$DQ_7 = \overline{RAS}$ xnor A_7
$DQ_8 = \overline{RAS}$ xnor A_8
$DQ_9 = \overline{RAS}$ xnor A_9
$DQ_{10} = \overline{RAS}$ xnor A_{10}
$DQ_{11} = \overline{RAS}$ xnor BA_1
$DQ_{12} = \overline{RAS}$ xnor BA_0
$DQ_{13} = \overline{RAS}$ xnor BA_2
$DQ_{14} = \overline{RAS}$ xnor DM_0
$DQ_{15} = \overline{RAS}$ xnor DM_1
$DQ_{16} = \overline{RAS}$ xnor DM_2
$DQ_{17} = \overline{RAS}$ xnor DM_3
$DQ_{18} = \overline{RAS}$ xnor CLK
$DQ_{19} = \overline{RAS}$ xnor $\overline{CLK}$
$DQ_{20} = \overline{RAS}$ xnor $\overline{WE}$
$DQ_{21} = A_0$ xnor A_1
$DQ_{22} = A_0$ xnor A_2
$DQ_{23} = A_0$ xnor A_3
$DQ_{24} = A_0$ xnor A_4
$DQ_{25} = A_0$ xnor A_5
$DQ_{26} = A_0$ xnor A_6
$DQ_{27} = A_0$ xnor A_7
$DQ_{28} = A_0$ xnor A_8
$DQ_{29} = A_0$ xnor A_9
$DQ_{30} = A_0$ xnor A_{10}
$DQ_{31} = A_0$ xnor BA_0
$DQS_0 = A_0$ xnor BA_1
$DQS_1 = A_0$ xnor BA_2
$DQS_2 = A_0$ xnor DM_0
$DQS_3 = A_0$ xnor DM_1

- EXAMPLE OF TEST CODE TABLE

Input bus																						Output bus																																			
$\overline{RAS}$	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	BA_0	BA_1	BA_2	DM_0	DM_1	DM_2	DM_3	CLK	$\overline{CLK}$	$\overline{WE}$	DQ_0	DQ_1	DQ_2	DQ_3	DQ_4	DQ_5	DQ_6	DQ_7	DQ_8	DQ_9	DQ_{10}	DQ_{11}	DQ_{12}	DQ_{13}	DQ_{14}	DQ_{15}	DQ_{16}	DQ_{17}	DQ_{18}	DQ_{19}	DQ_{20}	DQ_{21}	DQ_{22}	DQ_{23}	DQ_{24}	DQ_{25}	DQ_{26}	DQ_{27}	DQ_{28}	DQ_{29}	DQ_{30}	DQ_{31}	DQS_0	DQS_1	DQS_2	DQS_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
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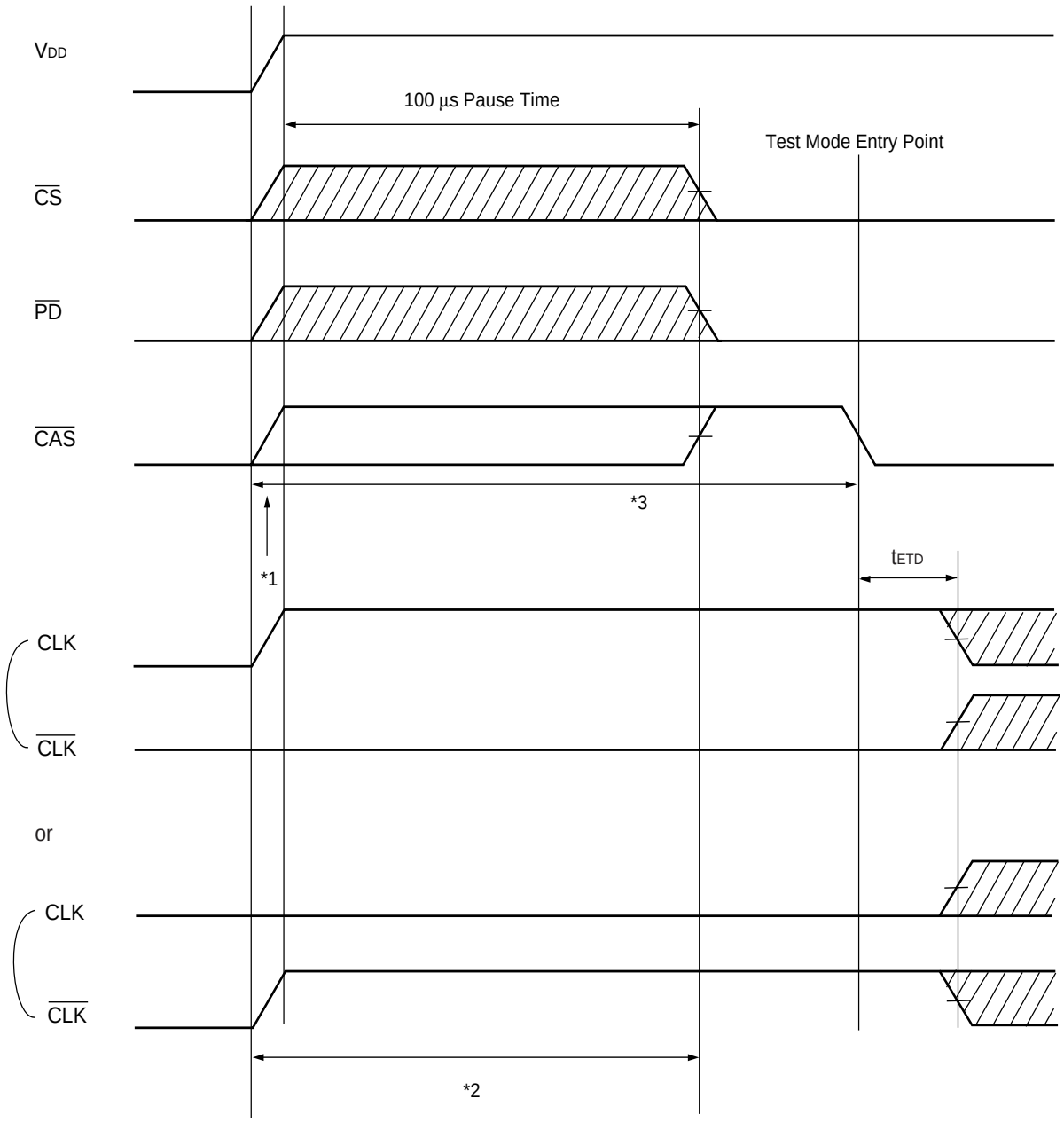
0 = input Low, 1 = input High, L = output Low, H = output High

AC SPECIFICATION

Parameter	Description	Minimum	Maximum	Units
t_{TS}	Test mode entry set up time	10	—	ns
t_{TH}	Test mode entry hold time	10	—	ns
t_{EPD}	Test mode exit to power on sequence delay time	10	—	ns
t_{TLZ}	$\overline{CS}$, CKE to output in Low-Z time	0	—	ns
t_{THZ}	$\overline{CS}$, CKE to output in High-Z time	0	20	ns
t_{TCA}	Test mode access time from control signals (clock enable & chip select)	—	40	ns
t_{TIA}	Test mode Input access time	—	20	ns
t_{TOH}	Test mode Output Hold time	0	—	ns
t_{ETD}	Test mode entry to test delay time	10	—	ns
t_{TIH}	Test mode input hold time	30	—	ns

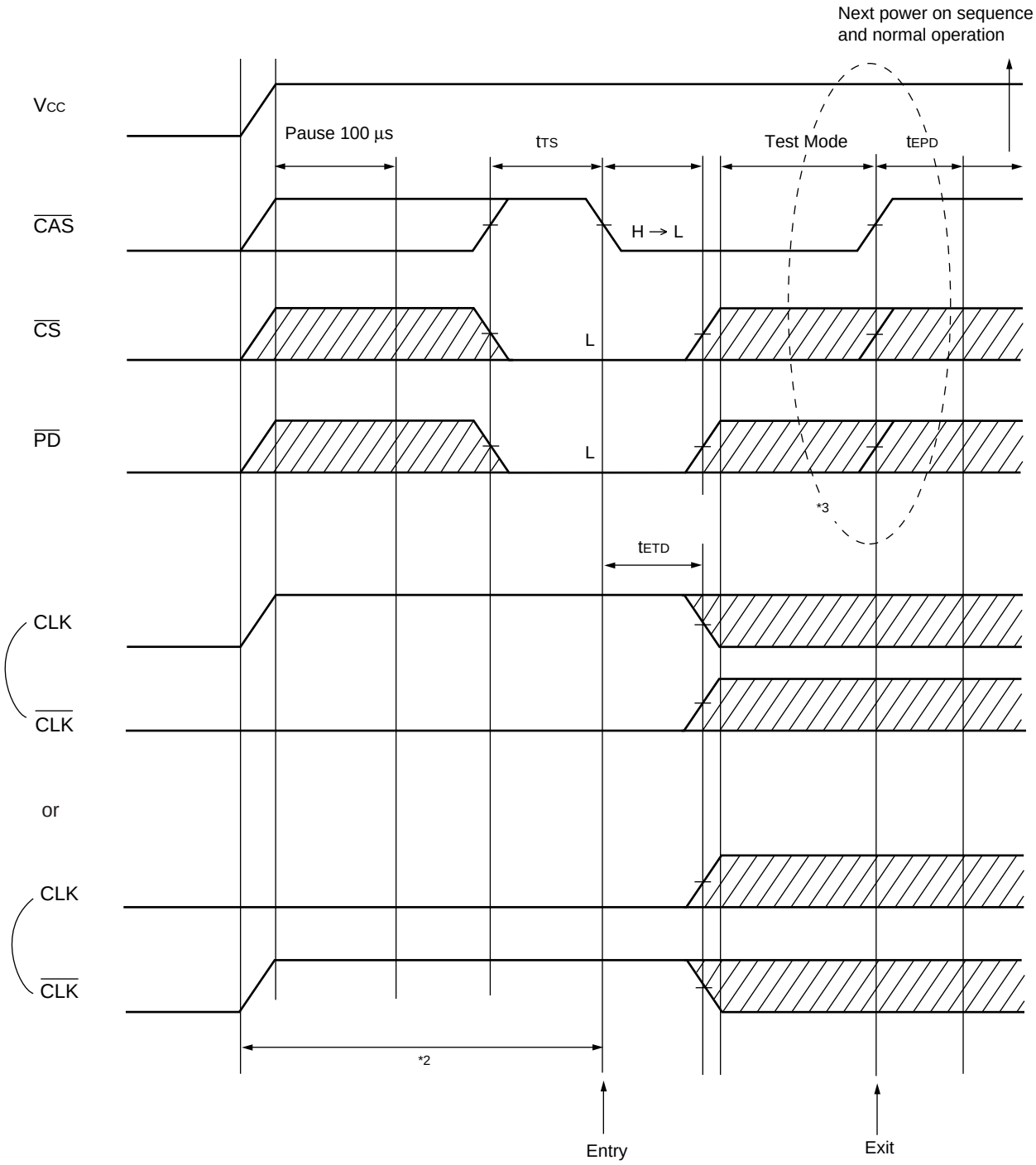
TIMING DIAGRAMS

TIMING DIAGRAM - 1: POWER-UP TIMING DIAGRAM



Notes: *1. $\overline{CAS}$ shall be staid either High or Low at power on.
*2. All output buffers maintains in High-Z state regardless of the state of control signals except for $\overline{CAS}$ as long as the above timing is maintained.
*3. $\overline{CAS}$ must not be brought from High to Low.

TIMING DIAGRAM - 2: SCITT TEST ENTRY AND EXIT *1

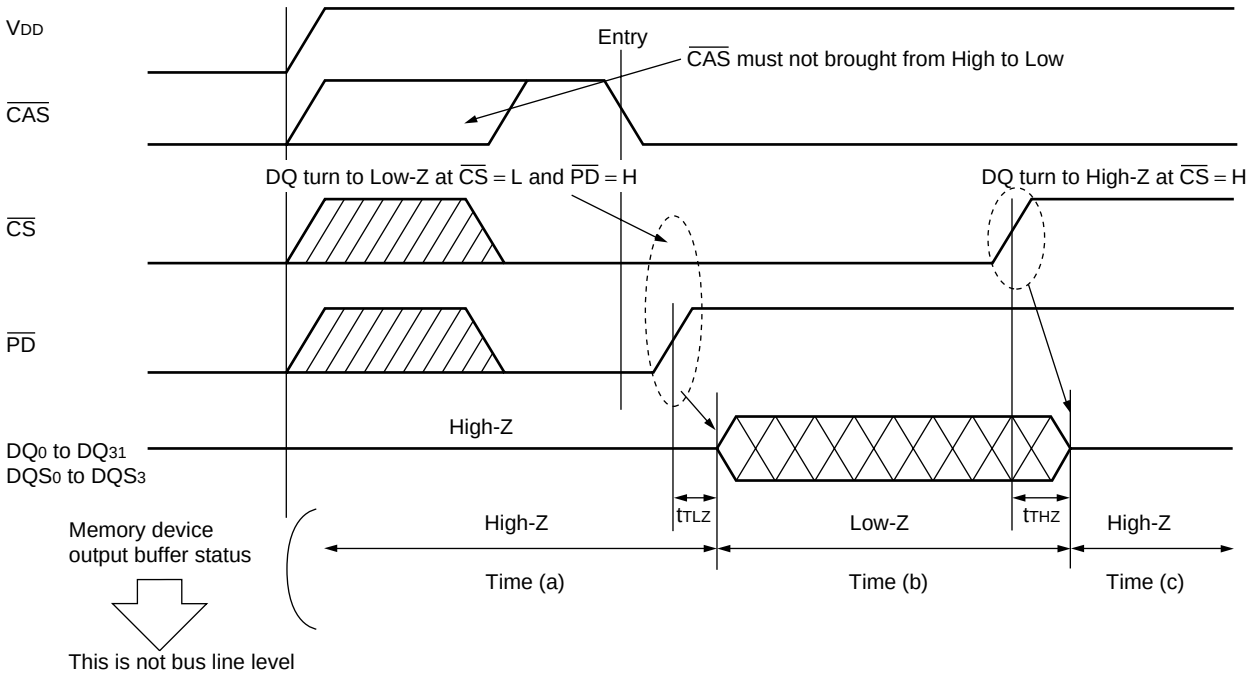


Notes: *1. If entry and exit operation have not been done correctly, $\overline{CAS}$, $\overline{CS}$, $\overline{PD}$ pins will have some problems.

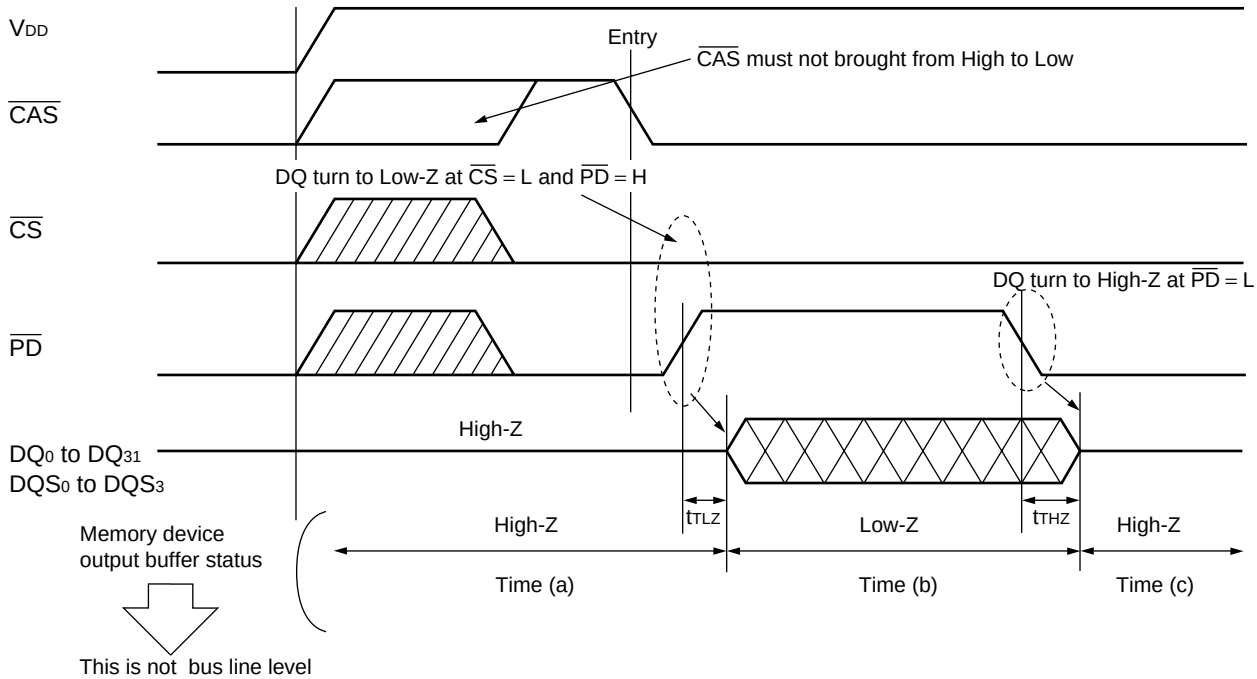
*2. PC or PCA commands must not be asserted. Test mode is terminated by those commands.

*3. Outputs must be disabled by $\overline{CS}$ = H or $\overline{PD}$ = L before Exit.

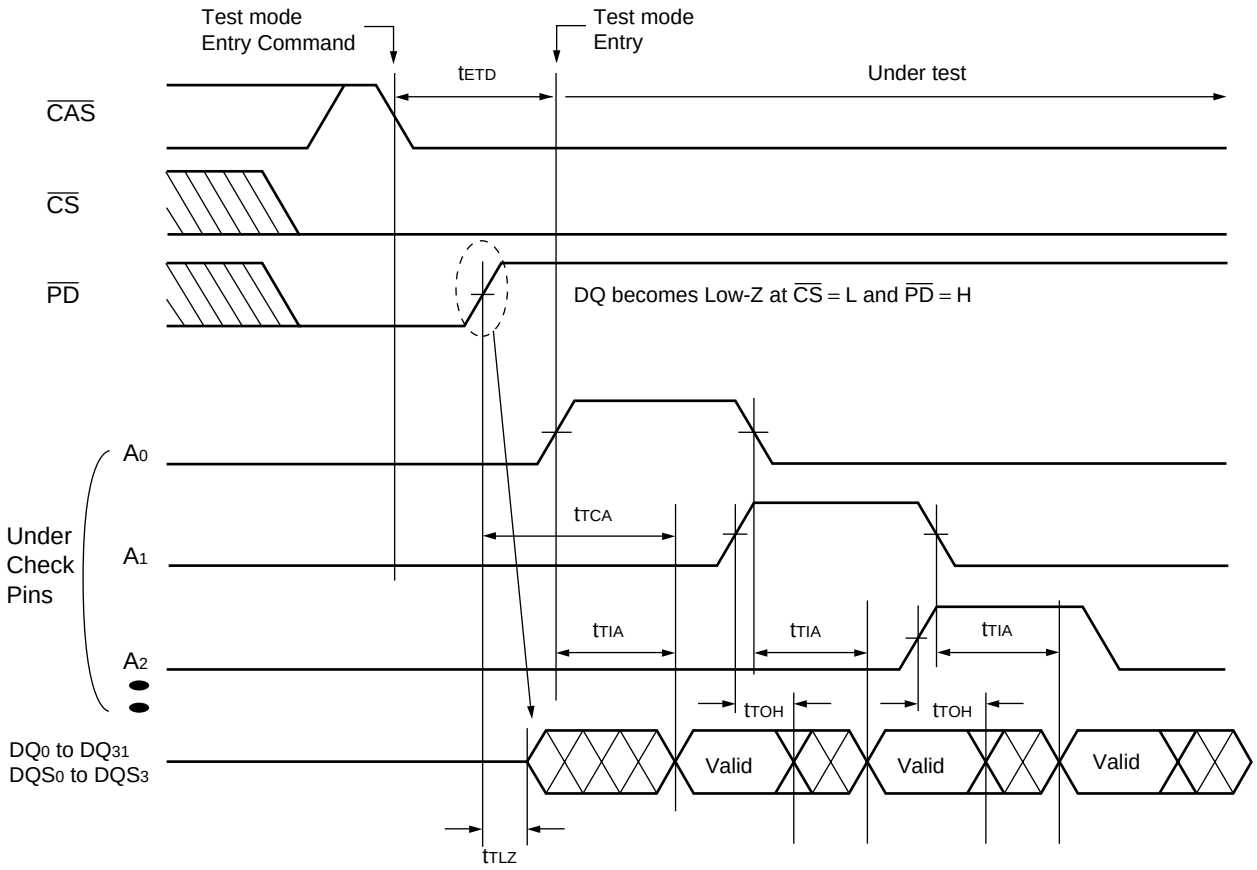
TIMING DIAGRAM - 3: OUTPUT CONTROL (1)



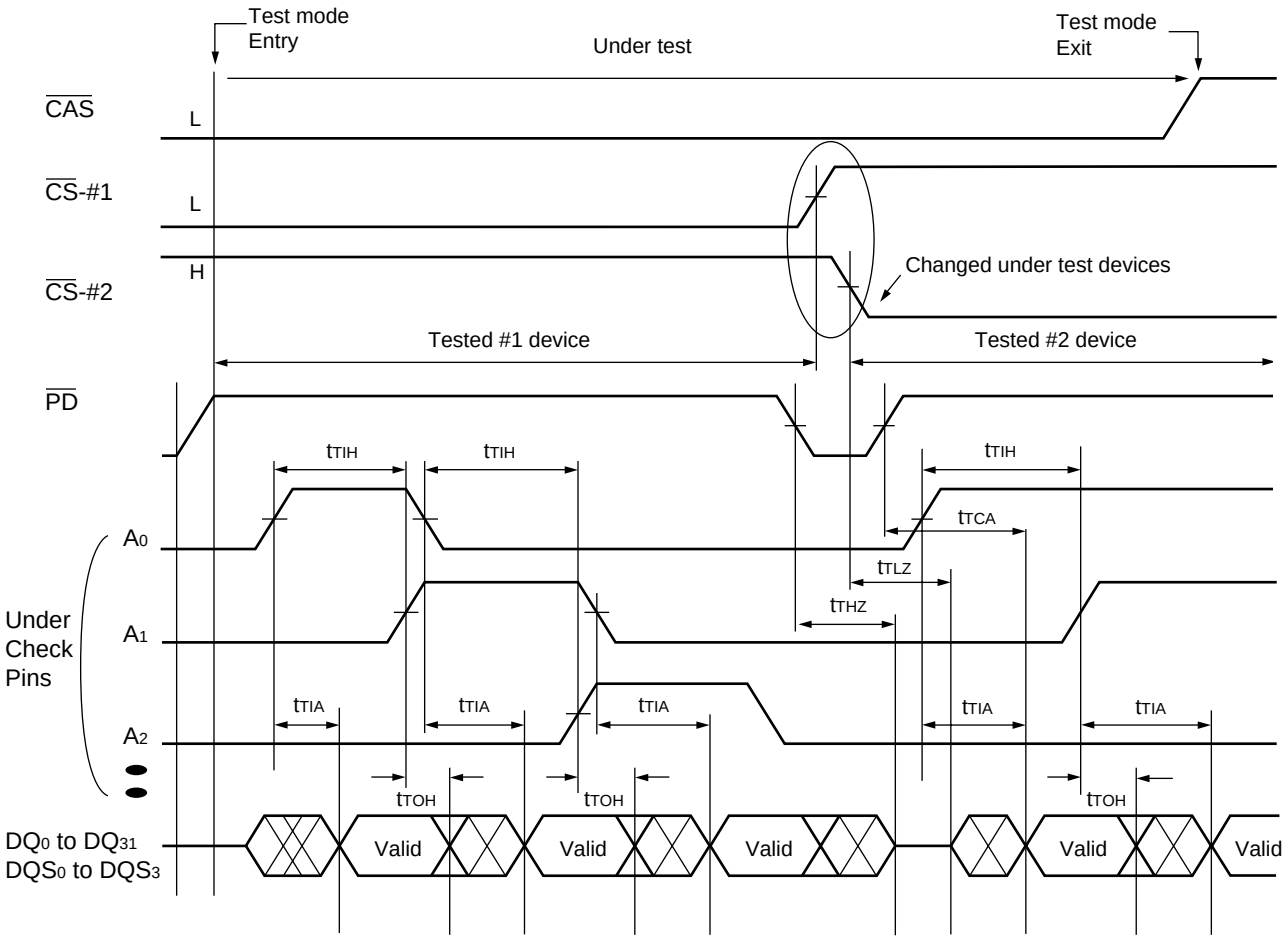
TIMING DIAGRAM - 4: OUTPUT CONTROL (2)



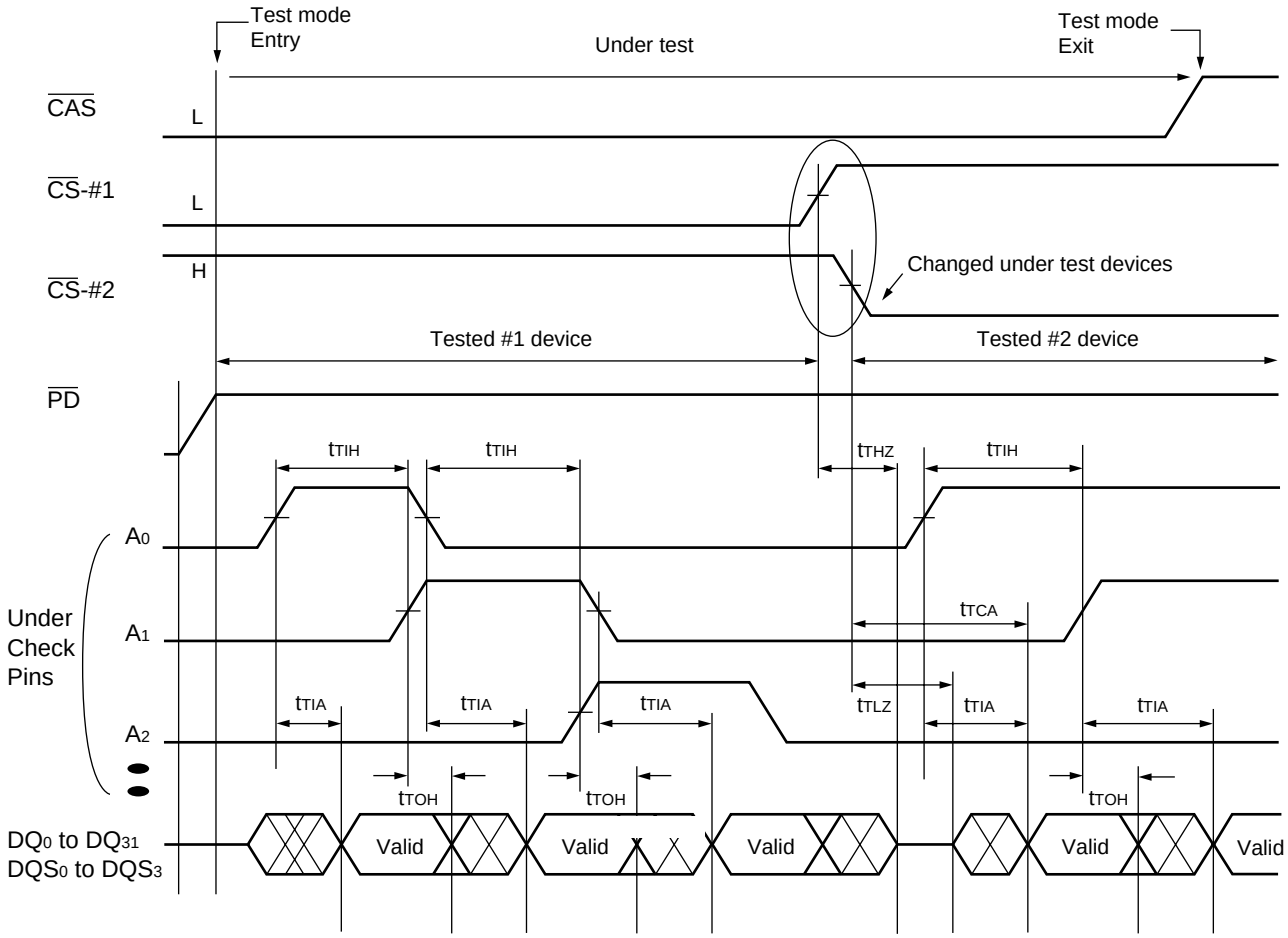
TIMING DIAGRAM - 5: TEST TIMING (1)



TIMING DIAGRAM - 6: TEST TIMING (2)



TIMING DIAGRAM - 7: TEST TIMING (3)



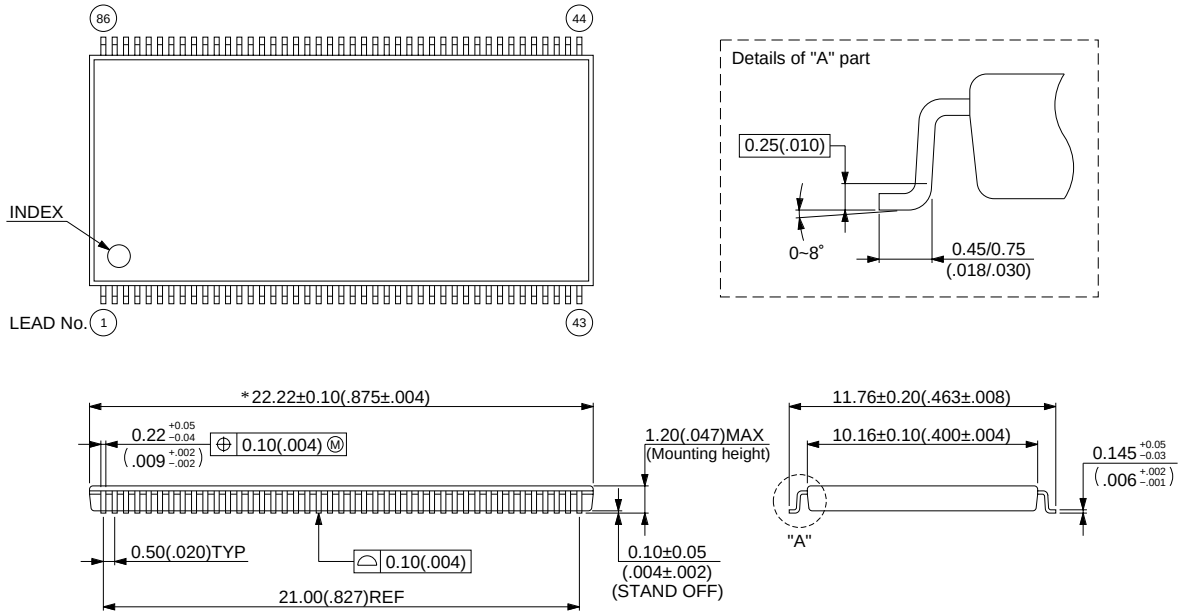
■ ORDERING INFORMATION

Part number	Package	Remarks
MB81N643289-50FN	86-pin plastic TSOP(II) (FPT-86P-M01)	—
MB81N643289-60FN		

■ PACKAGE DIMENSIONS

86-pin plastic TSOP (II)
(FPT-86P-M01)

*: Resin protrusion.(Each side: 0.15 (.006) Max.)



Dimensions in mm (inches)

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