MEMORY

CMOS

2 × 512 K × 16 BIT SINGLE DATA RATE I/F FCRAM™

Consumer/Embedded Application Specific Memory

MB81E161622-10/-12

CMOS 2-Bank × 524,288-Word × 16 Bit
Fast Cycle Random Access Memory (FCRAM) with Single Data Rate

■ DESCRIPTION

The Fujitsu MB81E161622 is a Fast Cycle Random Access Memory (FCRAM*) containing 16,777,216 memory cells accessible in a 16-bit format. The MB81E161622 features a fully synchronous operation referenced to a positive edge clock, whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB81E161622 is utilized using a Fujitsu advanced FCRAM core technology and designed to improve the random access performance and the complexity of controlling regular synchronous DRAM (SDRAM) which require many wait state due to long latency constraints.

The MB81E161622 is ideally suited for various embedded/consumer applications including digital AVs, printers and file storage where a large band width memory is needed.

* : FCRAM is a trademark of Fujitsu Limited, Japan.

■ PRODUCT LINEUP

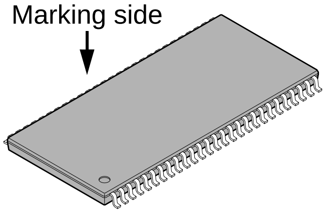
Parameter		MB81E161622	
		-10	-12
Clock Frequency @CL = 2		100 MHz Max.	84 MHz Max.
Burst Mode Cycle Time	CL = 1	15 ns Min.	20 ns Min.
	CL = 2	10 ns Min.	12 ns Min.
Access Time From Clock	CL = 1	10 ns Max.	14 ns Max.
	CL = 2	6 ns Max.	7 ns Max.
$\overline{\text{RAS}}$ Cycle Time		30 ns Min.	36 ns Min.
Operating Current (I_{CC1})		130 mA Max.	120 mA Max.
Power Down Mode Current (I_{CC2P})		0.6 mA Max.	
Self-refresh Current (I_{CC6})		0.6 mA Max.	

■ FEATURES

- Single +3.3 V Supply ±0.3 V tolerance
- LVTTL compatible I/O interface
- Two-bank operation
- Programmable burst type, burst length, and CAS latency
- 4 K refresh cycles every 64 ms
- Auto- and Self-refresh
- CKE power down mode
- Output Enable and Input Data Mask

■ PACKAGE

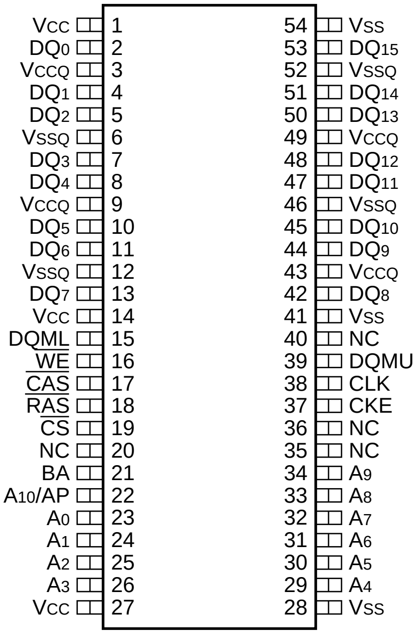
54-pin Plastic TSOP (II) Package



(FPT-54P-M02)
(Normal Bend)

■ PIN ASSIGNMENT

54-Pin TSOP (II)
(TOP VIEW)
< Normal Bend : FPT-54P-M02 >



(Marking side)

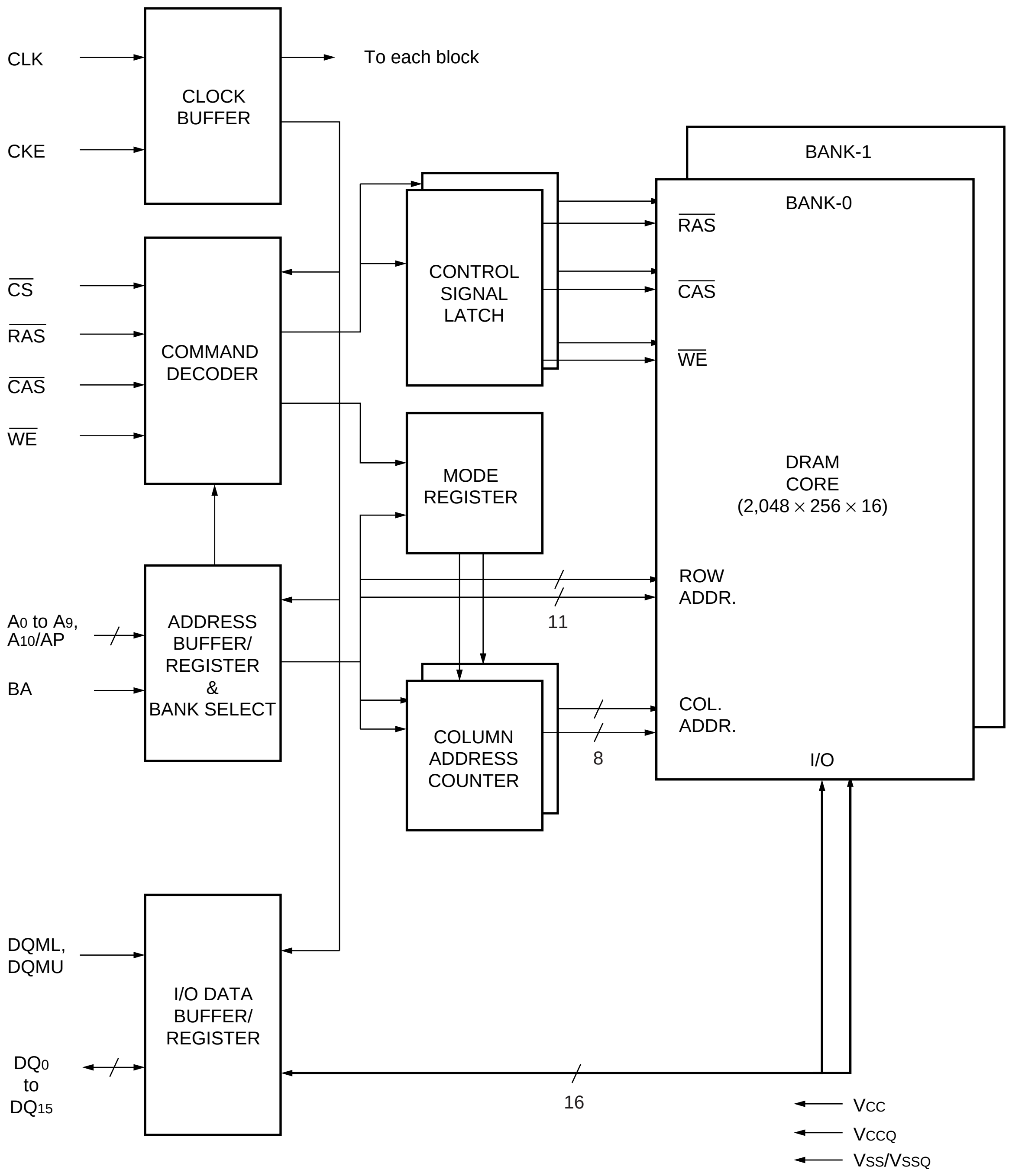
■ PIN DESCRIPTIONS

Symbol	Function
V_{CC}, V_{CCQ}	Supply Voltage
V_{SS}, V_{SSQ} *	Ground
DQ_0 to DQ_{15}	Data I/O • Lower Byte : DQ_0 to DQ_7 • Upper Byte : DQ_8 to DQ_{15}
DQML, DQMU	DQ MASK
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$	Chip Select
BA	Bank Select
AP	Auto Precharge Enable
A_0 to A_{10}	Address Input • Row : A_0 to A_{10} • Column : A_0 to A_7
CKE	Clock Enable
CLK	Clock Input
NC	No Connection

*: These pins are connected internally in the chip.

■ BLOCK DIAGRAM

Fig. 1 – MB81E161622 BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE *1

• COMMAND TRUTH TABLE *2, *3, *4

Function	Com-mand	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	A_{10} (AP)	A_9, A_8	A_7 to A_0
		n-1	n								
Device Deselect *5	DESL	H	X	H	X	X	X	X	X	X	X
No Operation *5	NOP	H	X	L	H	H	H	X	X	X	X
Burst Stop	BST	H	X	L	H	H	L	X	X	X	X
Read *6	READ	H	X	L	H	L	H	V	L	X	V
Read with Auto-precharge *6	READA	H	X	L	H	L	H	V	H	X	V
Write *6	WRIT	H	X	L	H	L	L	V	L	X	V
Write with Auto-precharge *6	WRITA	H	X	L	H	L	L	V	H	X	V
Bank Active *7	ACTV	H	X	L	L	H	H	V	V	V	V
Precharge Single Bank *8	PRE	H	X	L	L	H	L	V	L	X	X
Precharge All Banks *8	PALL	H	X	L	L	H	L	X	H	X	X
Mode Register Set *8, 9	MRS	H	X	L	L	L	L	L	L	V	V

*1: V = Valid, L = Logic Low, H = Logic High, X = either L or H.

*2: All commands assumes no CSUS command on previous rising edge of clock.

*3: All commands are assumed to be valid state transitions.

*4: All inputs are latched on the rising edge of the clock.

*5: The NOP and DESL commands have the same effect on the part. Unless specifically noted, NOP will represent both NOP and DESL commands in later descriptions.

*6: The READ, READA, WRIT and WRITA commands should be issued only after the corresponding bank has been activated (ACTV command) . Refer to “STATE DIAGRAM” in section “■ FUNCTIONAL DESCRIPTION.”

*7: The ACTV command should be issued only after the corresponding bank has been precharged (PRE or PALL command) .

*8: Required after power up. Refer to “POWER-UP INITIALIZATION” in section “■ FUNCTIONAL DESCRIPTION.”

*9: The MRS command should be issued only after all banks have been precharged (PRE or PALL command) and DQ is in High-Z. Refer to “STATE DIAGRAM” in section “■ FUNCTIONAL DESCRIPTION.”

• DQM TRUTH TABLE

Function	Command	CKE		DQML	DQMU
		n-1	n		
Data Write/Output Enable for Lower Byte	ENBL L	H	X	L	X
Data Write/Output Enable for Upper Byte	ENBL U	H	X	X	L
Data Mask/Output Disable for Lower Byte	MASK L	H	X	H	X
Data Mask/Output Disable for Upper Byte	MASK U	H	X	X	H

Note : DQML and DQMU controls DQ_{0-7} and DQ_{8-15}, respectively.

• CKE TRUTH TABLE

Current State	Function	Com-mand	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	A_9 to A_0
			n-1	n							
Bank Active	Clock Suspend Mode Entry *1	CSUS	H	L	X	X	X	X	X	X	X
Any (Except Idle)	Clock Suspend Continue *1		L	L	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		L	H	X	X	X	X	X	X	X
Idle	Auto-refresh Command *2	REF	H	H	L	L	L	H	X	X	X
Idle	Self-refresh Entry *2, *3	SELF	H	L	L	L	L	H	X	X	X
Self Refresh	Self-refresh Exit *4	SELFX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Power Down Entry *3	PD	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Power Down	Power Down Exit		L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X

*1: The CSUS command requires that at least one bank is active. Refer to “STATE DIAGRAM” in section “■ FUNCTIONAL DESCRIPTION.”

*2: The REF and SELF commands should be issued only after all banks have been precharged (PRE or PALL command) . Refer to “STATE DIAGRAM” in section “■ FUNCTIONAL DESCRIPTION.”

*3: The SELF and PD commands should be issued only after the last read data have been appeared on DQ.

*4: The CKE should be held High during t_{REFC}.

- **OPERATION COMMAND TABLE (Applicable to single bank)**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*1
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}	
	L	L	H	L	BA, AP	PRE	NOP	
	L	L	H	L	AP	PALL	NOP	*1
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*3, *5
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC})	*3, *6
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	Precharge	
	L	L	H	L	AP	PALL	Precharge	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP	*4
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge → Idle	
	L	L	H	L	AP	PALL	Terminate Burst, Precharge → Idle	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*4
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge → Idle	
	L	L	H	L	AP	PALL	Terminate Burst, Precharge → Idle	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Read with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	Illegal	*2
	L	L	H	L	AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Write with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge → Idle)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	Illegal	*2
	L	L	H	L	AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	X	BST	NOP (Idle after t_{RP})	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE	NOP	
	L	L	H	L	AP	PALL	NOP	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})	
	L	H	H	H	X	NOP	NOP (Bank Active after t_{RCD})	
	L	H	H	L	X	BST	NOP (Bank Active after t_{RCD})	*1
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*2
	L	L	H	H	BA, RA	ACTV	Illegal	*2
	L	L	H	L	BA, AP	PRE/	Illegal	*2
	L	L	H	L	AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Notes
Refreshing	H	X	X	X	X	DESL	NOP (Idle after t_{REFC})	
	L	H	H	X	X	NOP/BST	NOP (Idle after t_{REFC})	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after t_{RSC})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RSC})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

ABBREVIATIONS :

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

*1: Entry may affect other bank.

*2: Illegal to the bank in specified state; entry may be legal to the bank specified by BA, depending on the state of that bank.

*3: Illegal if any bank is not idle.

*4: Must satisfy bus contention, bus turn around, and/or write recovery requirements.
Refer to “TIMING DIAGRAM -11 & -12” in section “■ TIMIMG DIAGRAMS.”

*5: The SELF command should be issued only after the last read data has been appeared on DQ.

*6: The MRS command should be issued only when all DQ are in Hi-Z.

Note: All entries in OPERATION COMMAND TABLE assume that the CKE was High during the proceeding clock cycle and the current clock cycle.
Illegal means that the device operation and/or data-integrity are not guaranteed. If used, power up sequence will be asserted after power shut down.

- **COMMAND TRUTH TABLE FOR CKE**

Current State	CKE (n-1)	CKE (n)	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Addr	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{REFC})	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{REFC})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after t_{REFC}	
	H	H	L	H	H	H	X	Idle after t_{REFC}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	*1
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle	
	L	H	L	H	H	H	X		
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	
	L	H	L	L	X	X	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	H	H	X	X	Illegal	

(Continued)

(Continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Notes
All Banks Idle	H	H	H	X	X	X	V	Refer to the Operation Command Table.	
	H	H	L	H	X	X	V	Refer to the Operation Command Table.	
	H	H	L	L	H	X	V	Refer to the Operation Command Table.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	V	Refer to the Operation Command Table.	
	H	L	H	X	X	X	X	Power Down	
	H	L	L	H	H	H	X	Power Down	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh	*2
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active Bank Activating Read/Write Read with Auto-precharge/ Write with Auto-precharge	H	H	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	X	X	X	X	X	X	Invalid	
Clock Suspend	H	X	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	Illegal	

*1: CKE should be held High for t_{REFC} period.

*2: The SELF command should be issued only after the last data has been appeared on DQ.

Note: All entries in “COMMAND TRUTH TABLE FOR CKE” are specified at CKE (n) state and CKE input from CKE (n–1) to CKE (n) state must satisfy the corresponding setup and hold time for CKE.

■ FUNCTIONAL DESCRIPTION

SDRAM BASIC FUNCTION

Three major differences between SDRAMs and conventional DRAMs are : a synchronized operation, a burst mode, and a mode register.

The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for synchronization, while a DRAM is basically asynchronous memory although it has been using two clocks, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Each operation of a DRAM is determined by their timing phase differences while each operation of the SDRAM is determined by commands and all operations are referenced to a rising edge of a clock. Fig 2 shows the basic timing diagram differences between SDRAMs and DRAMs.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column address for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode registe**r is to configure the SDRAM operation and function into desired system conditions. MODE REGISTER TABLE shows how the SDRAM can be configured for system requirements by mode register programming.

FCRAM™

The MB81E161622 utilizes FCRAM core technology. The FCRAM is an acronym for Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

CLOCK (CLK) and CLOCK ENABLE (CKE)

All input and output signals of the SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a rising edge of a CLK. All outputs are validated by the CLK. A CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged) , the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

CHIP SELECT ($\overline{\text{CS}}$)

A $\overline{\text{CS}}$ enables all command inputs, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and address inputs. When the $\overline{\text{CS}}$ is High, command signals are negated but internal operations such as a burst cycle will not be suspended. If such a control isn't needed, the $\overline{\text{CS}}$ can be tied to ground level.

COMMAND INPUT ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$)

Unlike a conventional DRAM, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ do not directly imply SDRAM operations, such as Row address strobe by $\overline{\text{RAS}}$. Instead, each combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ inputs in conjunction with $\overline{\text{CS}}$ input at the rising edge of the CLK determines SDRAM operations. Refer to "■ FUNCTIONAL TRUTH TABLE."

ADDRESS INPUT (A_0 to A_{10})

Address input selects an arbitrary location of a total of 524,288 words of each memory cell matrix. A total of nineteen address input signals are required to decode such a matrix. The SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV) , eleven Row addresses are initially latched and the remainder of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or a Write command (WRIT or WRITA) .

BANK SELECT (BA)

This SDRAM has two banks and each bank contains 512 K words by 16-bit.
Bank selection by A_{11} occurs at Bank Active command (ACTV) followed by read (READ or READA) , write (WRIT or WRITA) , and precharge commands (PRE or PALL) .

DATA INPUTS AND OUTPUTS (DQ_0 to DQ_{15})

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input :

t_{RAC} ; from the bank active command when t_{RCD} (Min.) is satisfied. (This parameter is reference only.)
t_{CAC} ; from the read command when t_{RCD} is greater than t_{RCD} (Min.) at CL = 1.
t_{AC} ; from the clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of input data. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}) .

DATA I/O MASK (DQML/DQMU)

DQML and DQMU are an active high enable input and have an output disable and input mask functions. During burst cycle and when DQML/DQMU = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on the burst type.

BURST MODE OPERATION

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatically strobing column address. Access time and cycle time of Burst mode is specified as t_{CAC}/t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and the burst count length of 1, 2, 4 or 8 bits of boundary. In order to terminate or move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required :

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after l_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

BURST TYPE

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps around to the least significant address (= 0) . The interleave mode is a scrambled decoding scheme for A_0 through A_2. If the first access of column address is even (0) , the next address will be odd (1) , or vice-versa.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode	Interleave
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same row. If burst mode reaches the end of column address, then it wraps around to the first column address (= 0) and continues to count until interrupted by the new read (READ) /write (WRIT) , precharge (PRE) , or burst stop (BST) commands. The selection of Auto-precharge option is illegal during the full column burst operation.

The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When a read mode is interrupted by the BST command, the output will be in High-Z.
For the detailed rule, please refer to “TIMING DIAGRAM-8” in section “■ TIMING DIAGRAMS.”
When a write mode is interrupted by the BST command, the data to be applied at the same time with the BST command will be ignored.

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

The SDRAM memory core is the same as a conventional DRAM’s, requiring precharge and refresh operations. Precharge rewrites the bit line and reset the internal Row address line and is executed by the Precharge command (PRE) . With the Precharge command, the SDRAM will automatically be in standby state after precharge time (t_{RP}) .

The precharged bank is selected by combination of AP and A_{11} when the Precharge command is asserted. If AP = High, all banks are precharged regardless of BA (PALL) . If AP = Low, a bank to be selected by A_{11} is precharged (PRE) .
The auto-precharge enters precharge mode at the end of burst mode of read or write without the Precharge command assertion.
This auto precharge is entered by AP = High when a read or write command is asserted. Refer to “■ FUNCTIONAL TRUTH TABLE.”

AUTO-REFRESH (REF)

The Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates the Precharge command internally. All banks of the SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 15.6 µs or a total 4096 refresh commands within a 64 ms period.

SELF-REFRESH ENTRY (SELF)

The Self-refresh function provides automatic refresh by an internal timer as well as the Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF) . Once the SDRAM enters the self-refresh mode, all inputs except for CKE will be “don’t care” (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. The SELF command should be issued only after the last read data has been appeared on DQ.

Note : When the burst refresh method is used, a total of 4096 auto-refresh commands must be asserted within 4 ms prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit the Self-refresh mode, apply minimum t_{CKSP} after CKE brought high, and then the No operation command (NOP) or the Deselect command (DESL) should be asserted within one t_{RC} period. The CKE should be held High within one t_{RC} period after t_{CKSP}. Refer to “Timing Diagram-16” in section “■ TIMING DIAGRAMS” for the detail.

It is recommended to assert an Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

Note : When the burst refresh method is used, a total of 4096 auto-refresh commands must be asserted within 4 ms after the Self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of the SDRAM provides a variety of operations. The register consists of three operation fields; Burst Length, Burst Type, and CAS latency. Refer to “■ MODE REGISTER TABLE.”

The mode register can be programmed by the Mode Register Set command (MRS) . Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power) . The MRS command should be issued only when DQ is in Hi-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of the SDRAM. Refer to “POWER-UP INITIALIZATION” below.

POWER-UP INITIALIZATION

The SDRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply the power and start the clock. Attempt to maintain either the NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 100 µs.
3. Precharge all banks by the Precharge (PRE) or Precharge All command (PALL) .
4. Assert minimum of 2 Auto-refresh commands (REF) .
5. Program the mode register by the Mode Register Set command (MRS) .

In addition, it is recommended that DQM and CKE track V_{CC} to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 2 Auto-refresh commands (REF) .

Fig. 2 – BASIC TIMING FOR CONVENTIONAL DRAM vs. SYNCHRONOUS DYNAMIC RAM

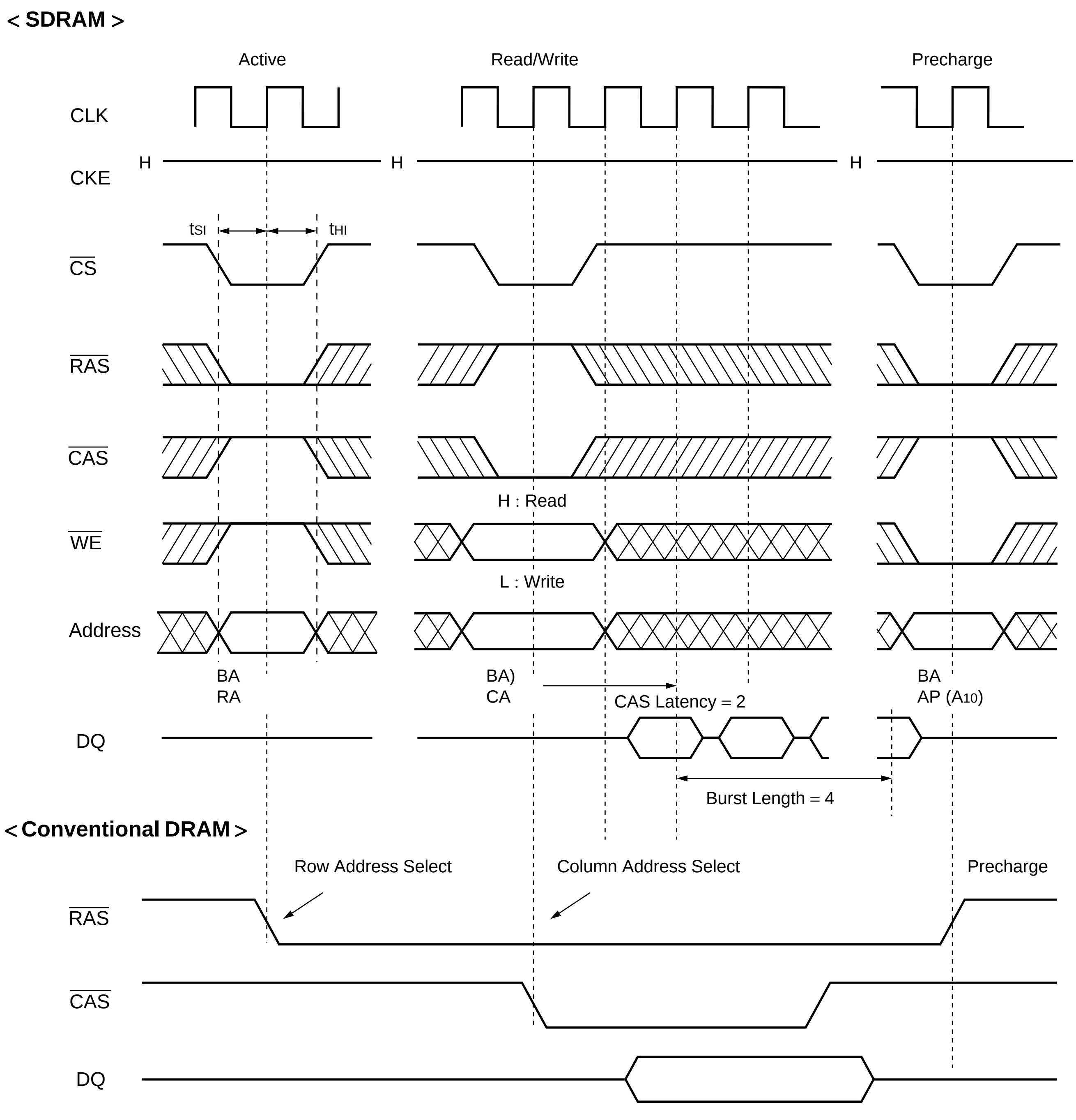
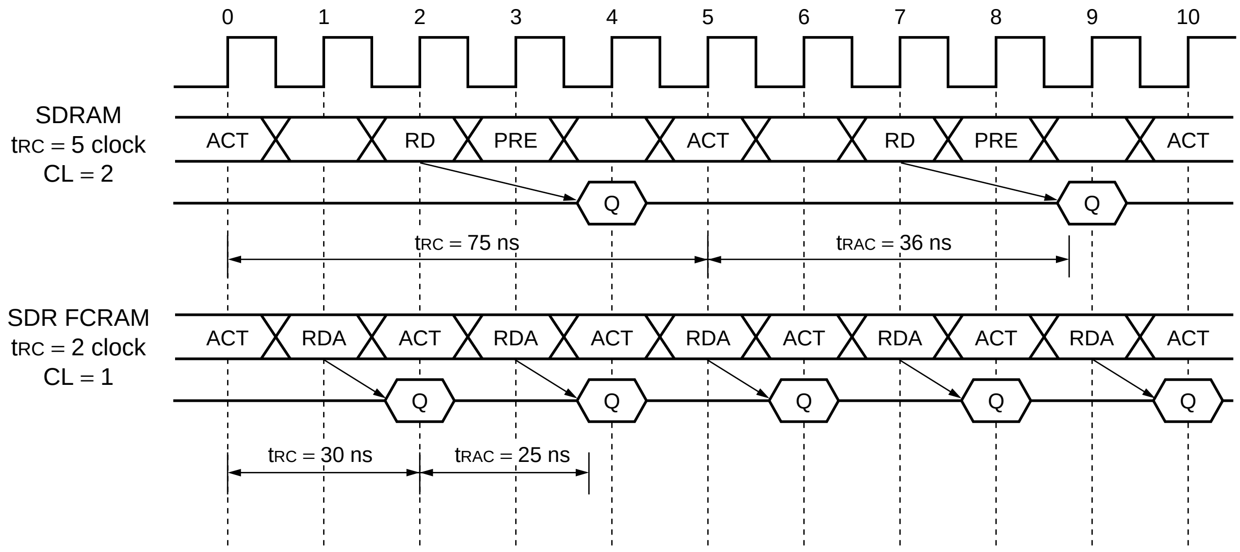
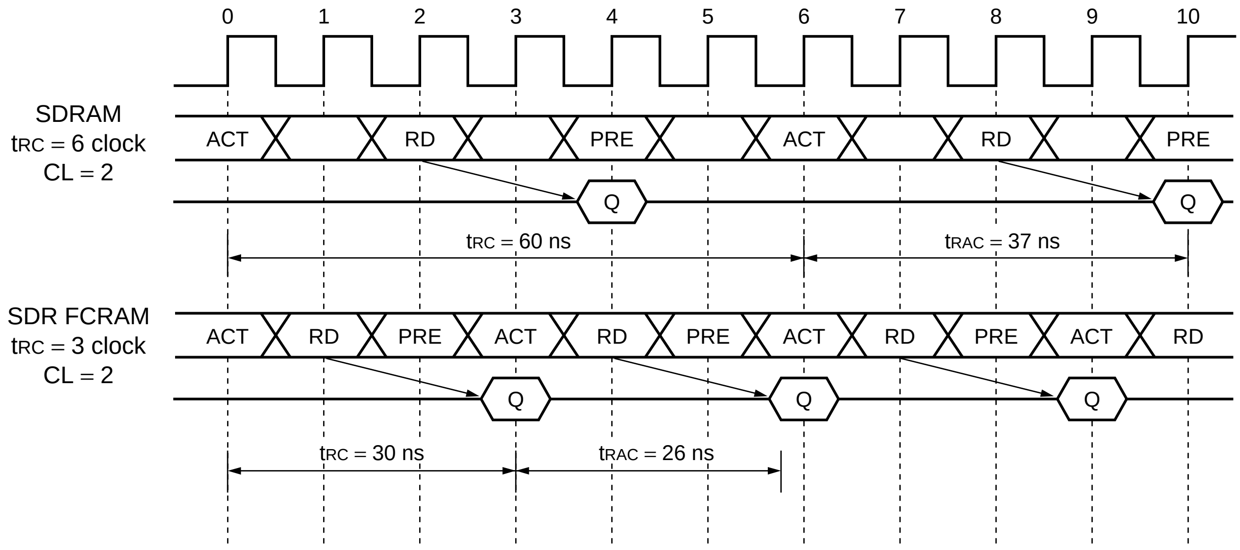


Fig. 3 – TIMING COMPARISON BETWEEN SDRAM AND SDR FCRAM

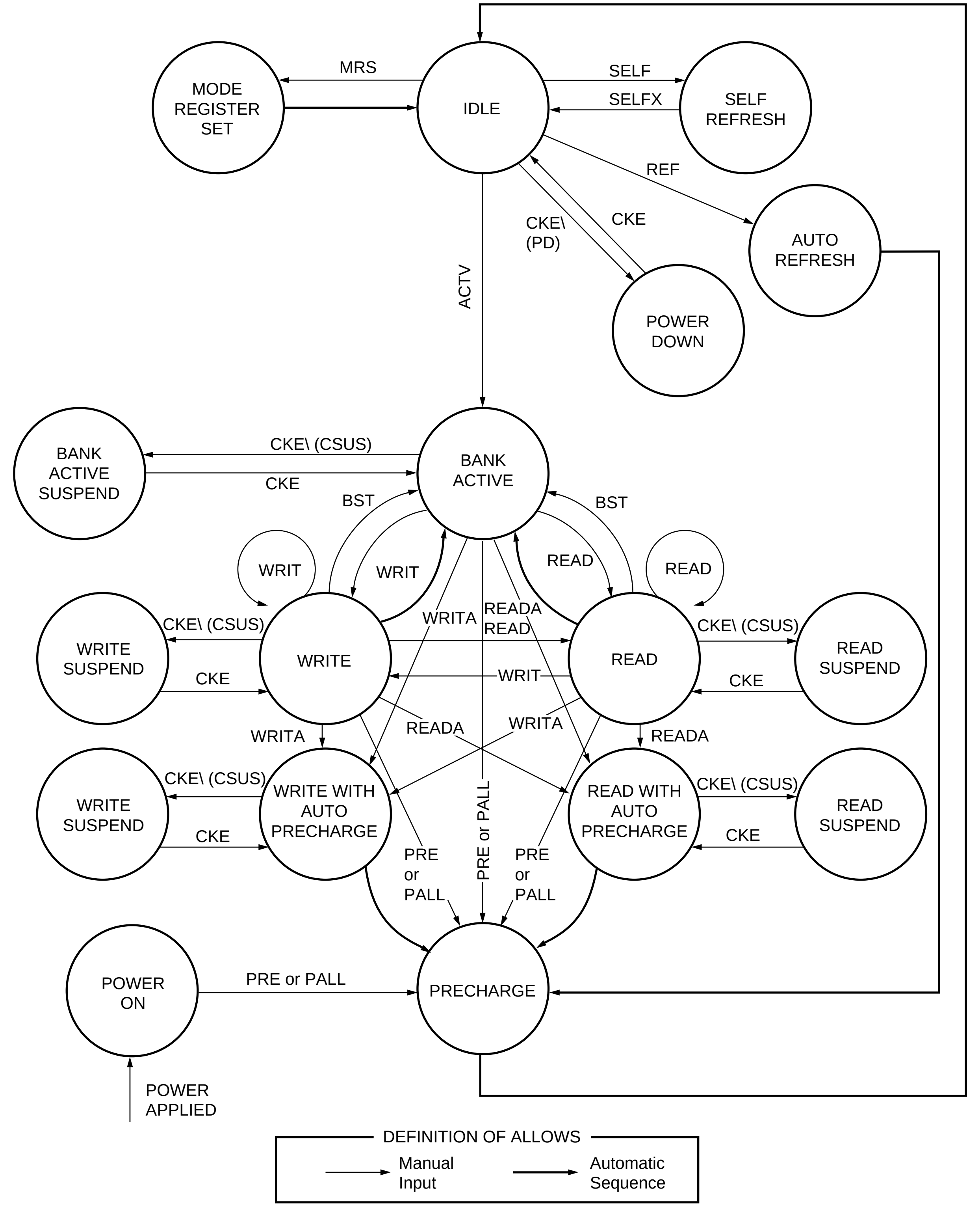


Example of Random Cycle Operation @ 67 MHz



Example of Random Cycle Operation @ 100 MHz

Fig. 4 – STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)



Note: CKE\ means CKE goes Low-level from High-level

■ BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

Second command (same bank) / First command	MRS	ACTV	READ	*3 READA	WRIT	*3 WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	▨	▨	▨	▨	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	▨	▨	t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}	▨	▨	1
READ	▨	▨	1	1	*4 1	*4 1	*3 1	*3 1	▨	▨	1
READA	*1 CL + BL	CL + BL-1	▨	▨	▨	▨	*3 CL + BL-1	*3 CL + BL-1	*1 CL + BL-1	*1 CL + BL-1	▨
WRIT	▨	▨	t_{WR}	t_{WR}	1	1	*3 t_{DPL}	*3 t_{DPL}	▨	▨	1
WRITA	*1 BL-1 + t_{DAL}	BL-1 + t_{DAL}	▨	▨	▨	▨	*3 BL-1 + t_{DAL}	*3 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	▨
PRE	*1, *2 t_{RP}	t_{RP}	▨	▨	▨	▨	1	*3 1	*1 t_{RP}	*1, *5 t_{RP}	1
PALL	*2 t_{RP}	t_{RP}	▨	▨	▨	▨	1	1	t_{RP}	*5 t_{RP}	1
REF	t_{REFC}	t_{REFC}	▨	▨	▨	▨	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}	▨	▨	▨	▨	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

*1: Assume all banks are in idle state.

*2: Assume output is in High-Z state.

*3: Assume t_{RAS} (Min.) is satisfied.

*4: Assume no I/O conflict.

*5: Assume the last data have been appeared on DQ.

▨ Illegal Command.

■ MULTI BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

Second command (other bank) / First command	MRS	ACTV	*4 READ	*4, *5 READA	*4 WRIT	*4, *5 WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	▨	▨	▨	▨	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	▨	*1 t_{RRD}	*6 1	*6 1	*6 1	*6 1	*5, *6 1	*6 t_{RAS}	▨	▨	1
READ	▨	*1, *3 1	1	1	*8 1	*8 1	*5 1	*5 1	▨	▨	1
READA	*1 CL + BL	*1, *3 1	*5 1	*5 1	*5, *8 1	*5, *8 1	*5 1	*5 CL + BL-1	*1 CL + BL-1	*1 CL + BL-1	▨
WRIT	▨	*1, *3 1	1	1	1	1	*5 1	*5 t_{DPL}	▨	▨	1
WRITA	*1 BL-1 + t_{DAL}	*1, *3 1	*5 1	*5 1	*5 1	*5 1	*5 1	*5 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	▨
PRE	*1, *2 t_{RP}	*1, *3 1	*6 1	*6 1	*6 1	*6 1	*5, *6 1	*6 1	*1 t_{RP}	*1, *7 t_{RP}	1
PALL	*2 t_{RP}	t_{RP}	▨	▨	▨	▨	1	1	t_{RP}	*7 t_{RP}	1
REF	t_{REFC}	t_{REFC}	▨	▨	▨	▨	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}	▨	▨	▨	▨	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

*1: Assume all banks are in idle state.

*2: Assume output is in High-Z state.

*3: t_{RRD} (Min.) of other bank (the second command will be asserted) is satisfied.

*4: Assume other bank is in active, read or write state.

*5: Assume t_{RAS} (Min.) is satisfied.

*6: Assume other banks are not in READA/WRITA state.

*7: Assume the last data have been appeared on DQ.

*8: Assume no I/O conflict.

▨ Illegal Command.

■ MODE REGISTER TABLE

MODE REGISTER SET

BA	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	0	0	0	0	CL			BT	BL			MODE REGISTER

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT = 0	BT = 1 *
0	0	0	1	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_3	Burst Type
0	Sequential (Wrap around, Binary-up)
1	Interleave (Wrap around, Binary-up)

*: BL = 1 and Full Column are not applicable to the interleave mode.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Voltage of V_{CC} Supply Relative to V_{SS}	V_{CC}, V_{CCQ}	–0.5	to +4.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	to +4.6	V
Short Circuit Output Current	I_{OUT}	–50	to +50	mA
Power Dissipation	P_D	—	1.3	W
Storage Temperature	T_{STG}	–55	to +125	°C

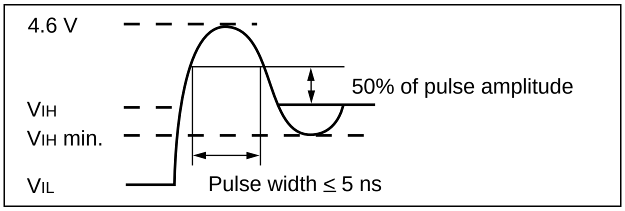
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

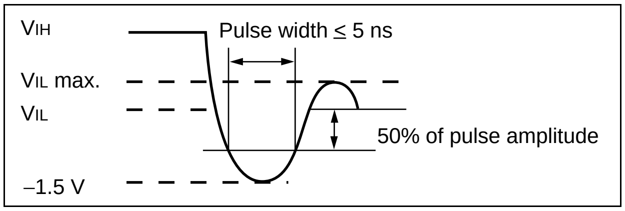
(Referenced to V_{SS})

Parameter	Notes	Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage		V_{CC}, V_{CCQ}	3.0	3.3	3.6	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage	*1	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Low Voltage	*2	V_{IL}	–0.5	—	0.8	V
Ambient Temperature		Ta	0	—	+70	°C

*1: Overshoot limit : V_{IH} (Max.)
= 4.6 V for pulse width ≤ 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.



*2: Undershoot limit : V_{IL} (Min.)
= V_{SS} – 1.5 V for pulse width ≤ 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

(Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Except for CLK	C_{IN1}	2.5	—	5.0	pF
Input Capacitance for CLK	C_{IN2}	2.5	—	4.0	pF
I/O Capacitance	$C_{I/O}$	4.0	—	6.5	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Output High Voltage		$V_{OH\ (DC)}$	$I_{OH} = -2$ mA	2.4	—	V
Output Low Voltage		$V_{OL\ (DC)}$	$I_{OL} = 2$ mA	—	0.4	V
Input Leakage Current (Any Input)		I_{LI}	$0\ V \leq V_{IN} \leq V_{CC}$; All other pins not under test = 0 V	–5	5	µA
Output Leakage Current		I_{LO}	$0\ V \leq V_{IN} \leq V_{CC}$; Data out disabled	–5	5	µA
Operating Current (Average Power Supply Current)	MB81E161622-10	I_{CC1}	Burst Length = 4 t_{RC} = Min. for BL = 4 t_{CK} = Min. One bank active Output pin open Addresses changed up to one time during t_{CK} (Min.) $0\ V \leq V_{IN} \leq V_{IL}$ Max. V_{IH} Min. $\leq V_{IN} \leq V_{CC}$	—	130	mA
	MB81E161622-12				120	
Precharge Standby Current (Power Supply Current)		I_{CC2P}	CKE = V_{IL} All banks idle, t_{CK} = Min. Power down mode $0\ V \leq V_{IN} \leq V_{IL}$ Max. V_{IH} Min. $\leq V_{IN} \leq V_{CC}$	—	0.6	mA
		I_{CC2PS}	CKE = V_{IL}, All banks idle CLK = V_{IH} or V_{IL} Power down mode $0\ V \leq V_{IN} \leq V_{IL}$ Max. V_{IH} Min. $\leq V_{IN} \leq V_{CC}$	—	0.6	mA
Precharge Standby Current (Power Supply Current)		I_{CC2N}	CKE = V_{IH} , All banks idle t_{CK} = 15 ns NOP command only, Input signals (except to CMD) are changed one time during 30 ns $0\ V \leq V_{IN} \leq V_{IL}$ Max. V_{IH} Min. $\leq V_{IN} \leq V_{CC}$	—	20	mA
		I_{CC2NS}	CKE = V_{IH} All banks idle CLK = V_{IH} or V_{IL} Input signal are stable $0\ V \leq V_{IN} \leq V_{IL}$ Max. V_{IH} Min. $\leq V_{IN} \leq V_{CC}$	—	2	mA

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Active Standby Current (Power Supply Current)		I_{CC3P}	CKE = V_{IL} Any bank active t_{CK} = Min. 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	1	mA
		I_{CC3PS}	CKE = V_{IL} Any bank active CLK = V_{IH} or V_{IL} 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	1	mA
		I_{CC3N}	CKE = V_{IH} Any bank active t_{CK} = 15 ns NOP command only, Input signals (except to CMD) are changed one time during 30 ns 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	20	mA
		I_{CC3NS}	CKE = V_{IH} Any bank active CLK = V_{IH} or V_{IL} Input signals are stable 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	2	mA
Burst mode Current (Average Power Supply Current)	MB81E161622-10	I_{CC4}	t_{CK} = Min. Burst Length = 4 Output pin open All-banks active Gapless data 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	100	mA
	MB81E161622-12				90	
Refresh Current #1 (Average Power Supply Current)	MB81E161622-10	I_{CC5}	Auto-refresh; t_{CK} = Min. t_{REFC} = Min. 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	80	mA
	MB81E161622-12				70	
Refresh Current #2 (Average Power Supply Current)		I_{CC6}	Self-refresh; t_{CK} = Min. CKE ≤ 0.2 V 0 V ≤ V_{IN} ≤ V_{IL} Max. V_{IH} Min. ≤ V_{IN} ≤ V_{CC}	—	0.6	mA

Notes: 1. All voltages are referenced to V_{SS}.
2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
3. I_{CC} depends on output termination, load conditions, clock rate, number of address and/or command change within certain period. The specified values are obtained with the output open.

2. AC Characteristics

(At recommended operating conditions unless otherwise noted.) Note *1, *2, and *3

Parameter	Notes		Symbol	MB81E161622-10		MB81E161622-12		Unit
				Min.	Max.	Min.	Max.	
Clock Period		CL = 1	t_{CK1}	15	—	20	—	ns
		CL = 2	t_{CK2}	10		12		ns
Clock High Time	*4		t_{CH}	3	—	4	—	ns
Clock Low Time	*4		t_{CL}	3	—	4	—	ns
Input Setup Time	*4		t_{SI}	2	—	2	—	ns
Input Hold Time except for CKE	*4		t_{HI}	1	—	1.5	—	ns
$\overline{\text{RAS}}$ Access Time	*5		t_{RAC}	—	25	—	34	ns
$\overline{\text{CAS}}$ Access Time	*4, 6		t_{CAC}	—	10	—	14	ns
Access Time from Clock (t_{CK} = Min.)	*4, 6, 7	CL = 1	t_{AC1}	—	10	—	14	ns
		CL = 2	t_{AC2}		6		7	ns
Output in Low-Z	*4		t_{LZ}	0	—	0	—	ns
Output in High-Z	*4, 8	CL = 1	t_{HZ1}	3	10	3	14	ns
		CL = 2	t_{HZ2}		6		7	ns
Output Hold Time	*4, 6		t_{OH}	3	—	3	—	ns
Time between Auto-Refresh command interval	*5		t_{REFI}	—	15.6	—	15.6	µs
Time between Refresh			t_{REF}	—	64	—	64	ms
Transition Time	*4		t_{T}	0.5	10	0.5	10	ns
CKE Setup Time for Power Down Exit Time	*4		t_{CKSP}	3	—	3	—	ns

BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter	Notes	Symbol	MB81E161622				Unit
			-10		-12		
			Min.	Max.	Min.	Max.	
$\overline{\text{RAS}}$ Cycle Time	*9	t_{RC}	30	—	36	—	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	10	—	12	—	ns
$\overline{\text{RAS}}$ Active Time		t_{RAS}	15	110000	20	110000	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time		t_{RCD}	10	—	12	—	ns
Write Recovery Time		t_{WR}	10	—	12	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ Bank Active Delay Time		t_{RRD}	10	—	12	—	ns
Data-in to Precharge Lead Time		t_{DPL}	10	—	12	—	ns
Data-in to Active/ Refresh Command Period	CL = 1	t_{DAL1}	15	—	20	—	ns
	CL = 2	t_{DAL2}	20	—	24	—	ns
Refresh Cycle Time		t_{REFC}	50	—	60	—	ns
Mode Resister Set Cycle Time		t_{RSC}	10	—	12	—	ns

CLOCK COUNT FORMULA Note *10

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}}$$ (Round up to a whole number)

LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81E161622 -10	MB81E161622 -12	Unit
CKE to Clock Disable		l_{CKE}	1	1	cycle
DQM to Output in High-Z		l_{DQZ}	2	2	cycle
DQM to Input Data Delay		l_{DQD}	0	0	cycle
Last Output to Write Command Delay		l_{OWD}	2	2	cycle
Write Command to Input Data Delay		l_{DWD}	0	0	cycle
Precharge to Output in High-Z Delay	CL = 1	l_{ROH1}	1	1	cycle
	CL = 2	l_{ROH2}	2	2	cycle
Burst Stop Command to Output in High-Z Delay	CL = 1	l_{BSH1}	1	1	cycle
	CL = 2	l_{BSH2}	2	2	cycle
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay (Min.)		l_{CCD}	1	1	cycle
$\overline{\text{CAS}}$ Bank Delay (Min.)		l_{CBD}	1	1	cycle

*1: AC characteristics are measured after following the POWER-UP INITIALIZATION procedure.

*2: AC characteristics assume $t_T = 1$ ns and 50 Ω of terminated load.

*3: 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (Min.) and V_{IL} (Max.) . Refer to Fig. 5.

*4: If input signal transition time (t_T) is longer than 1 ns; [(t_T / 2) – 0.5] ns should be added to t_{CAC} (Max.) , t_{AC} (Max.) , t_{HZ} (Max.) , and t_{CKSP} (Min.) spec values, [(t_T / 2) – 0.5] ns should be subtracted from t_{LZ} (Min.) , t_{HZ} (Min.) , and t_{OH} (Min.) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min.) , t_{CL} (Min.) , t_{SI} (Min.) , and t_{HI} (Min.) spec values.

*5: This value is for reference only.

*6: Measured under AC test load circuit shown in Fig. 4.

*7: t_{AC} also specifies the access time at burst mode except for first access at CL = 1.

*8: Specified where output buffer is no longer driven.

*9: t_{RC} (Min.) is not sum of t_{RAS} (Min.) and t_{RP} (Min.) . Actual clock count of t_{RC} (l_{RC}) must satisfy t_{RC} (Min.) , t_{RAS} (Min.) and t_{RP} (Min.) .

*10: All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula : clock count equals base value divided by clock period (round up to a whole number) .

Fig. 5 – OUTPUT LOAD CIRCUIT

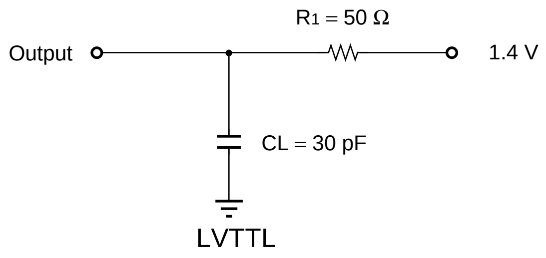
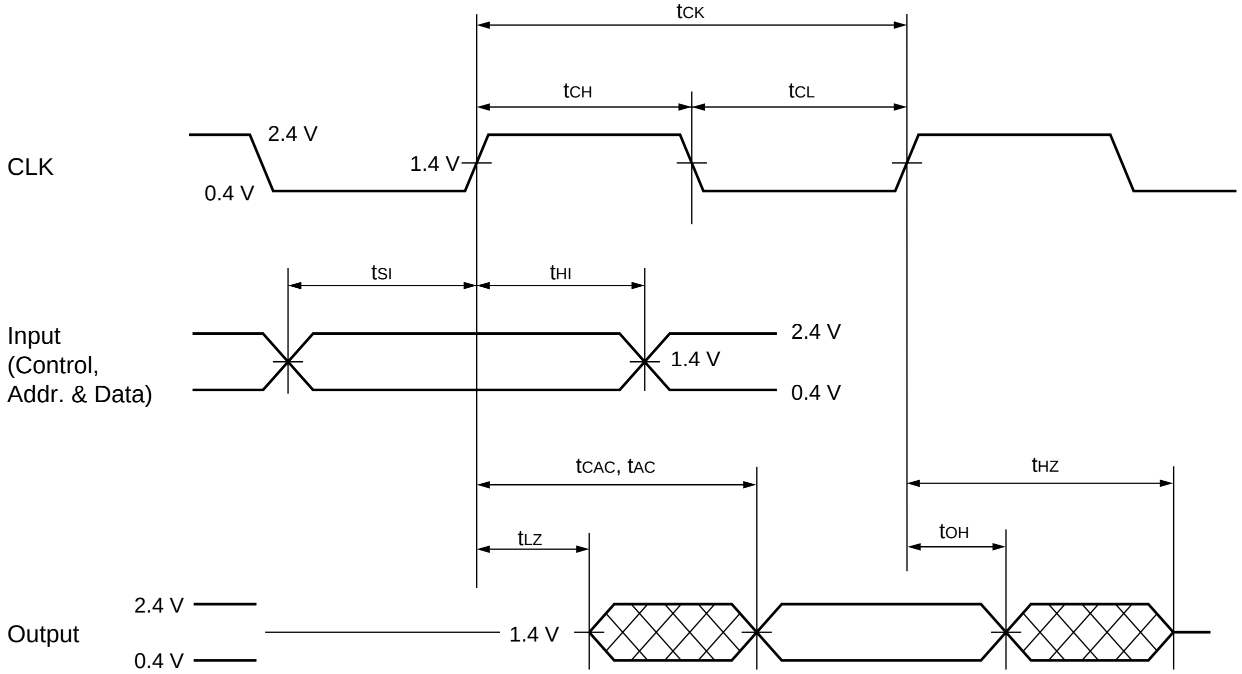


Fig. 6 – TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME



Note : Reference level of input signal is 1.4 V for LVTTL.
Access time is measured at 1.4 V for LVTTL.
AC characteristics are also measured in this condition.

Fig. 7 – TIMING DIAGRAM, DELAY TIME FOR POWER DOWN EXIT

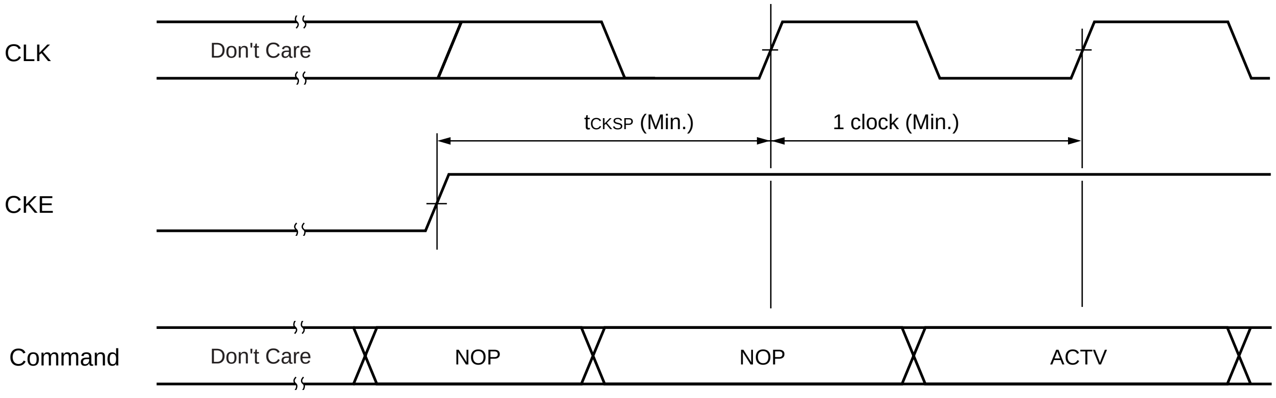
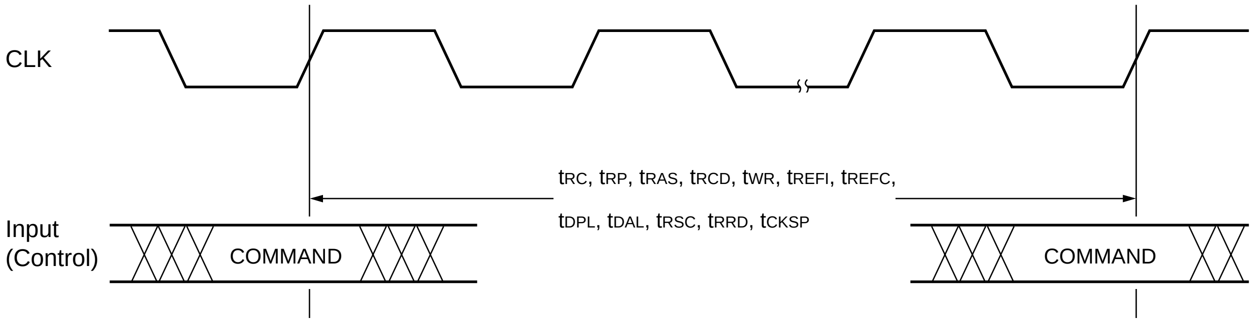
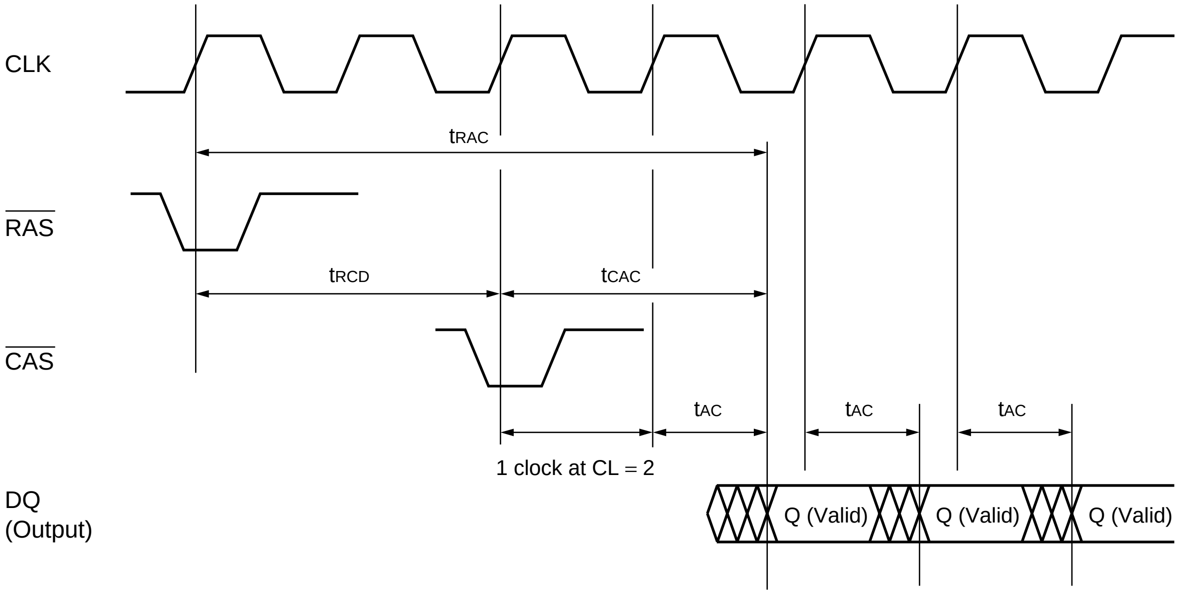


Fig. 8 – TIMING DIAGRAM, PULSE WIDTH



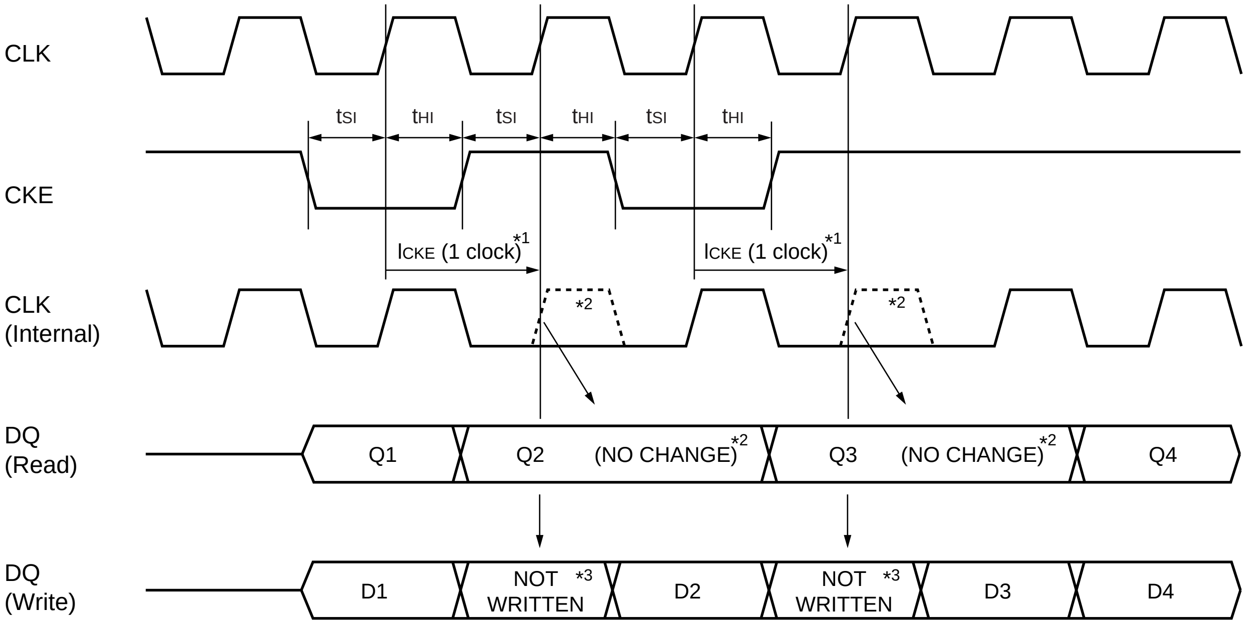
Note : These parameters are a limit value of the rising edge of the clock from one command input to the next input. t_{CKSP} is the latency value from the rising edge of the CKE. Measurement reference voltage is 1.4 V.

Fig. 9 – TIMING DIAGRAM, ACCESS TIME



■ TIMING DIAGRAMS

TIMING DIAGRAM – 1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)

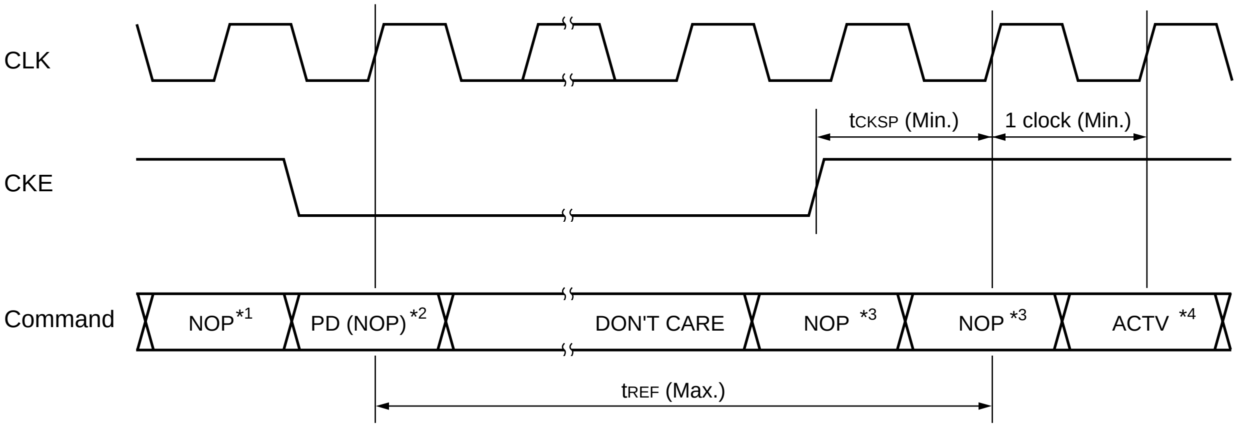


*1: The latency of the CKE (l_{CKE}) is one clock.

*2: During the read mode, burst counter will not be incremented/decremented at the next clock of the CSUS command. Output data remains the same data.

*3: During the write mode, data at the next clock of the CSUS command is ignored.

TIMING DIAGRAM – 2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT



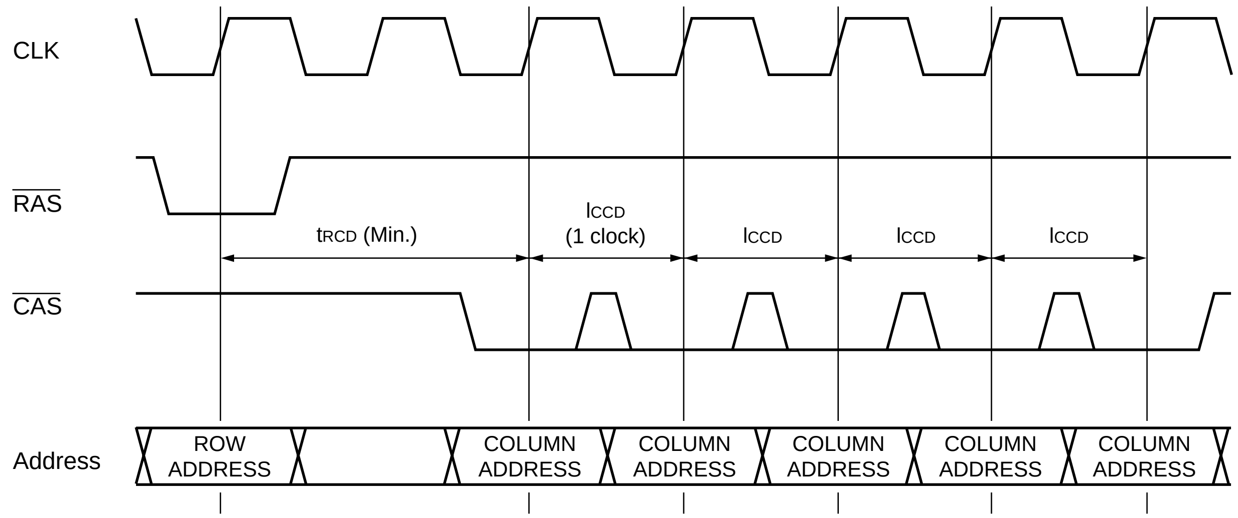
*1: The Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.

*2: The Precharge command can be posted in conjunction with CKE after the last read data has been appeared on DQ.

*3: It is recommended to apply the NOP command in conjunction with CKE.

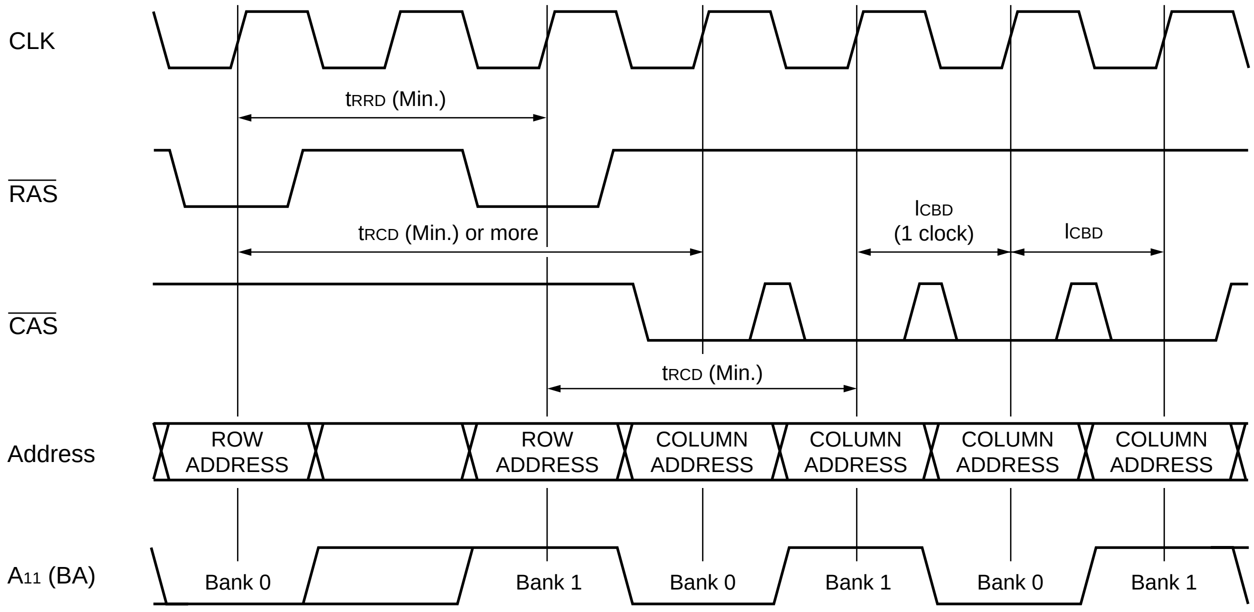
*4: The ACTV command can be latched after t_{CKSP} (Min.) + 1 clock (Min.) .

TIMING DIAGRAM – 3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



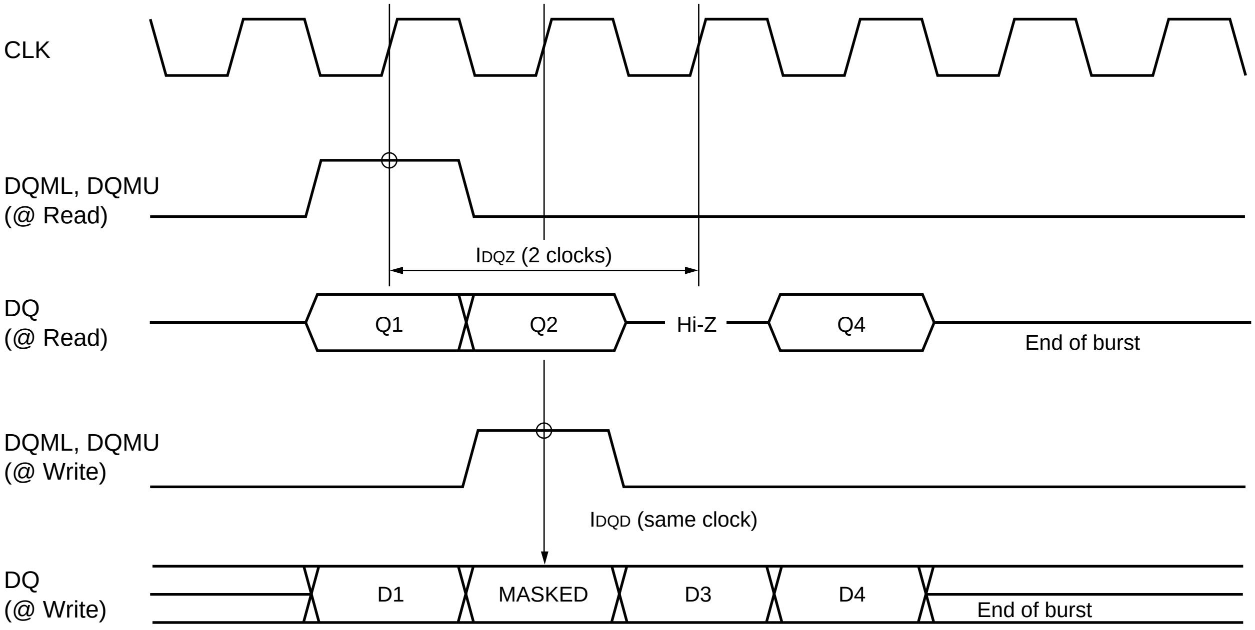
Note : $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay can be one or more clock period.

TIMING DIAGRAM – 4 : DIFFERENT BANK ADDRESS INPUT DELAY

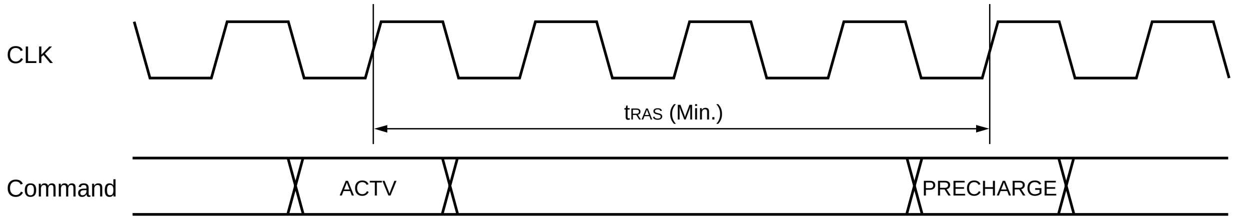


Note : $\overline{\text{CAS}}$ Bank delay can be one or more clock period.

TIMING DIAGRAM – 5 : DQMU, DQML - INPUT MASK AND OUTPUT DISABLE (@ BL = 4)

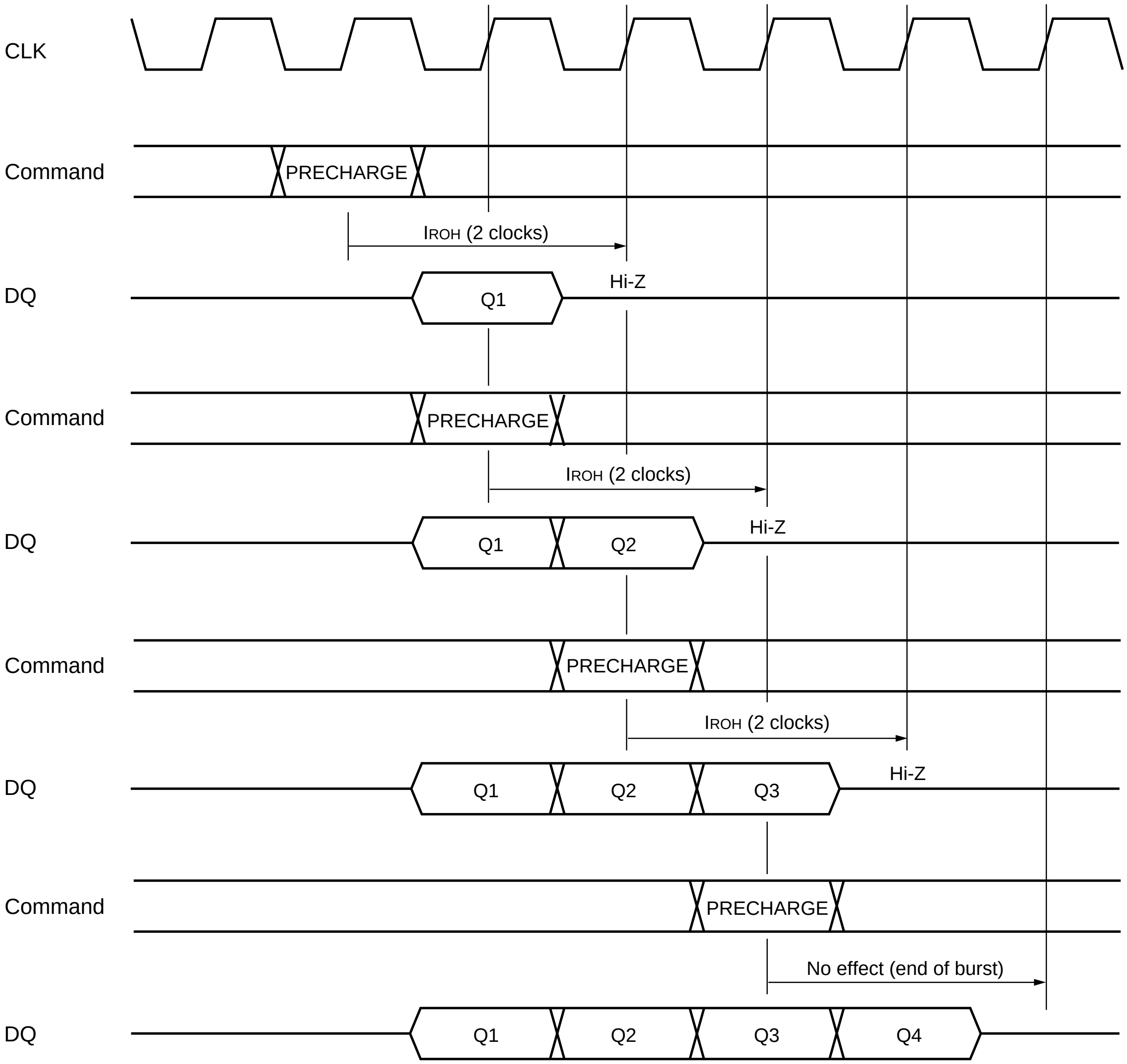


TIMING DIAGRAM – 6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)



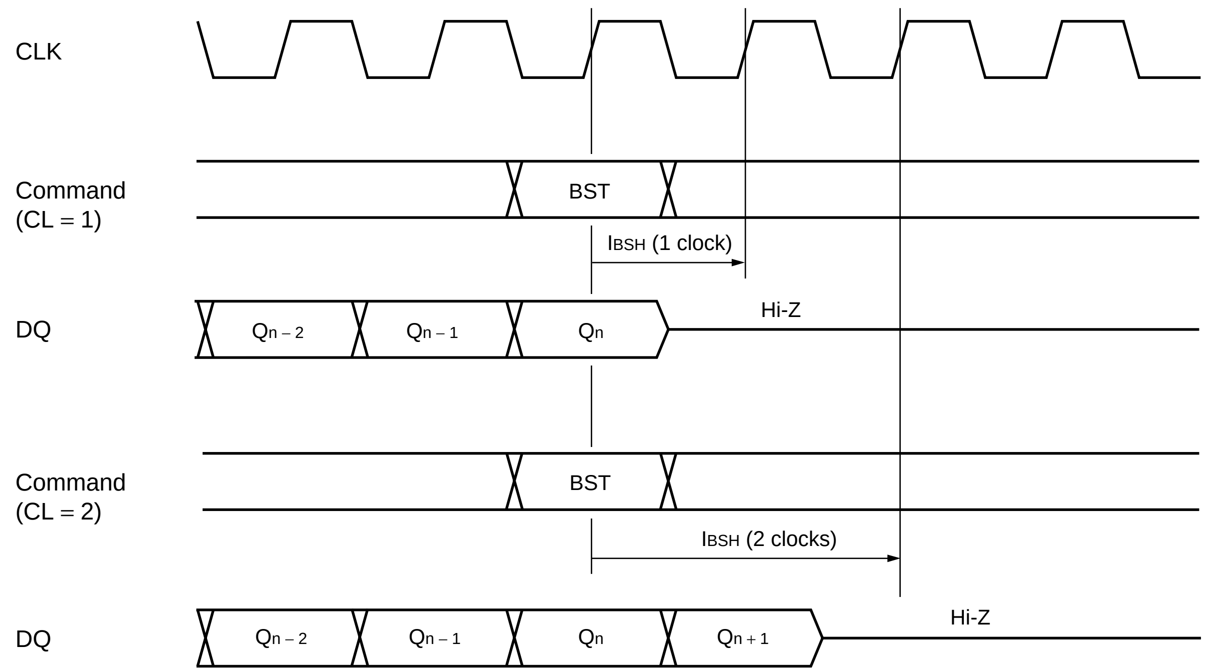
Note : PRECHARGE means ‘PRE’ or ‘PALL’.

TIMING DIAGRAM – 7 : READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)

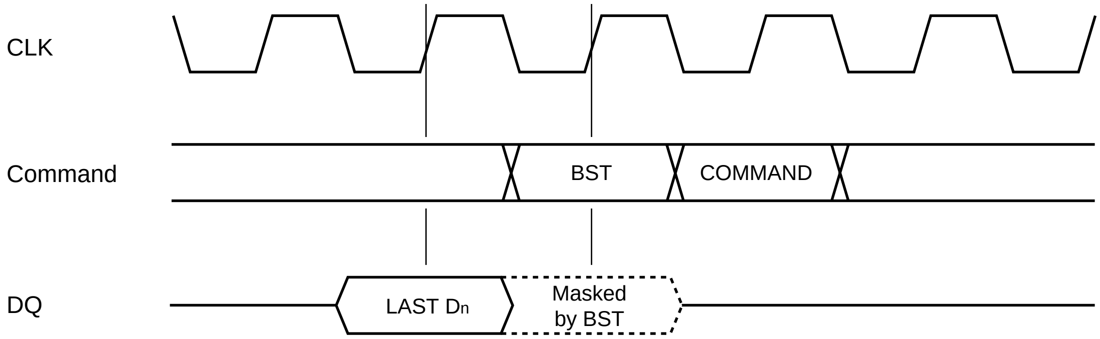


Note : In case of CL = 1, the l_{ROH} is 1 clock.
In case of CL = 2, the l_{ROH} is 2 clocks.
PRECHARGE means ‘PRE’ or ‘PALL’.

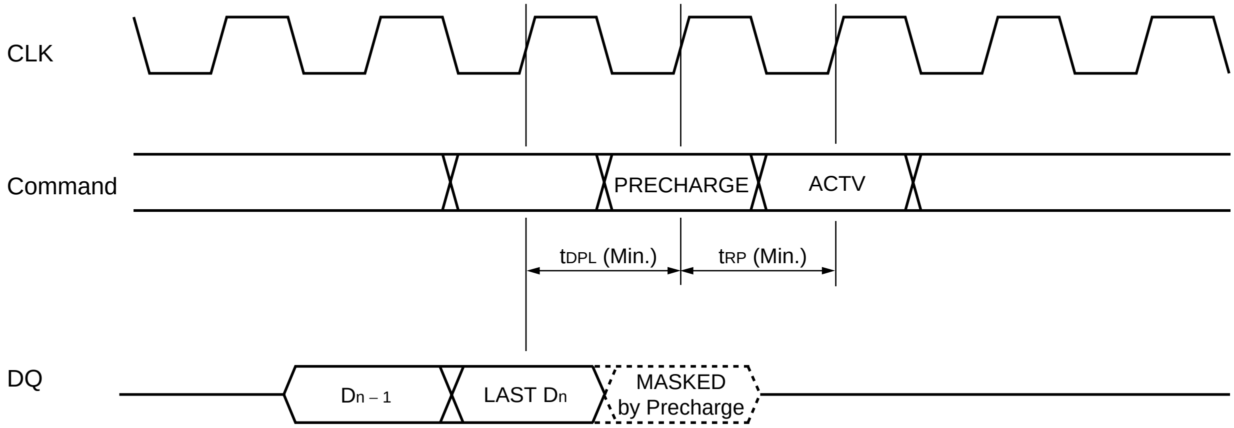
TIMING DIAGRAM – 8 : READ INTERRUPTED BY BURST STOP (EXAMPLE @ BL = Full Column)



TIMING DIAGRAM – 9 : WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ BL = 2)

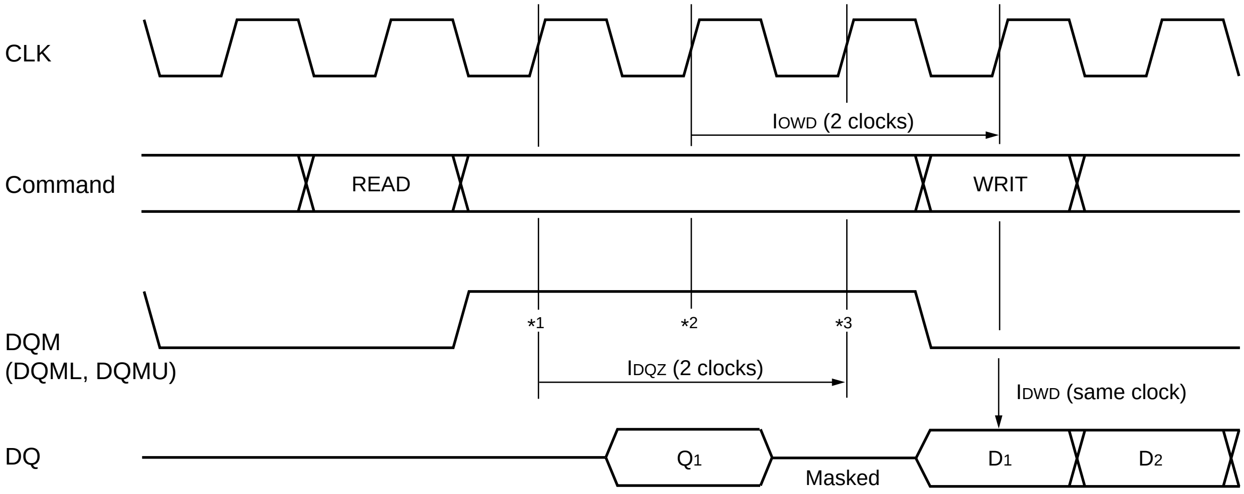


TIMING DIAGRAM – 10 : WRITE INTERRUPTED BY PRECHARGE



Note : The precharge command (PRE) should be issued only after the t_{DPL} of final data input is satisfied.
PRECHARGE means ‘PRE’ or ‘PALL’.

TIMING DIAGRAM – 11 : READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 2, BL = 4)

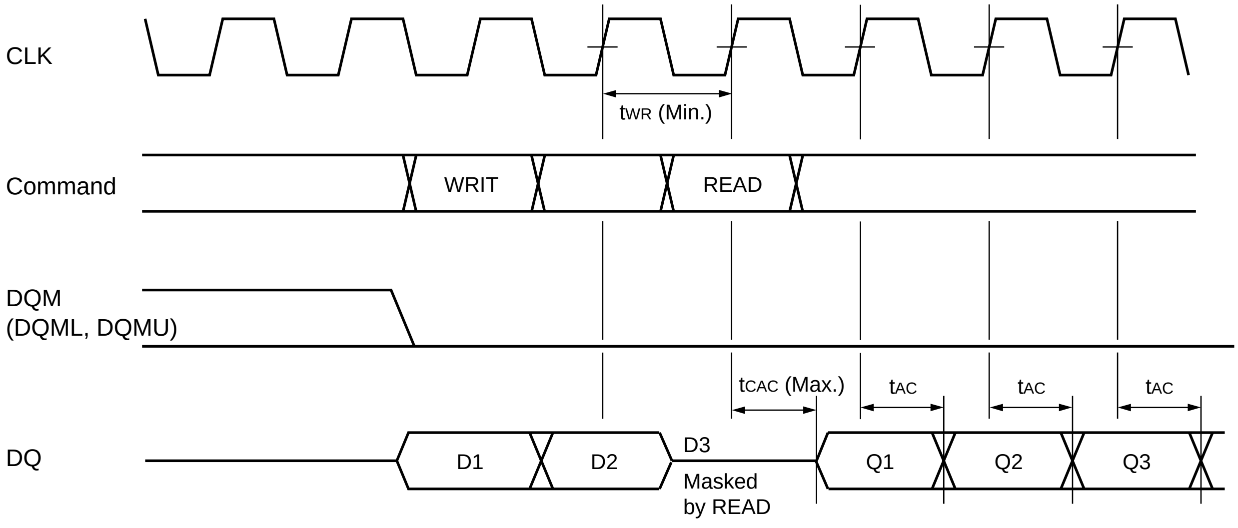


*1: The First DQM makes high-impedance state High-Z between the last output and the first input data.

*2: The Second DQM makes internal output data mask to avoid bus contention.

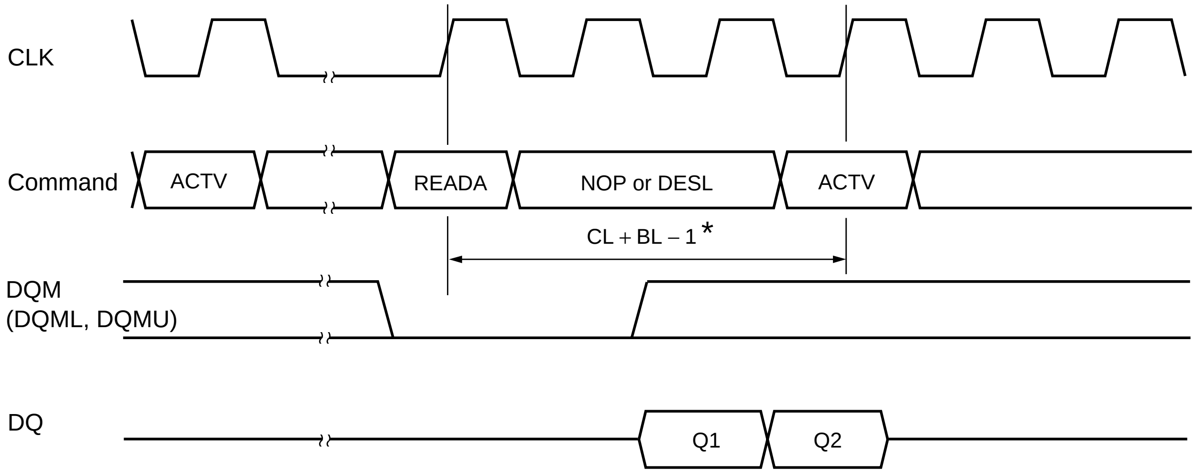
*3: The Third DQM in illustrated above also makes internal output data mask. If burst read ends (the final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

TIMING DIAGRAM – 12 : WRITE TO READ TIMING (EXAMPLE @ CL = 1, BL = 4)



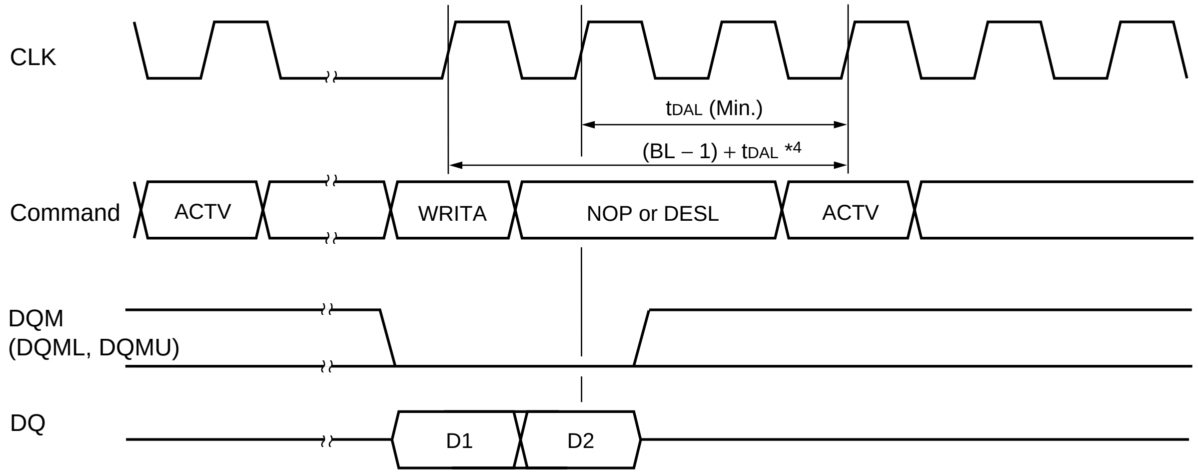
Note : The Read command should be issued after t_{WR} of the final data input is satisfied.
The write data after the READ command is masked by the READ command.

TIMING DIAGRAM – 13 : READ WITH AUTO-PRECHARGE (EXAPLE @ CL = 2, BL = 2 Applied to same bank)



*: The Next ACTV command should be issued after CL + BL – 1 from the READA command.

TIMING DIAGRAM – 14 : WRITE WITH AUTO-PRECHARGE (EXAMPLE @ CL = 2, BL = 2 Applied to same bank)



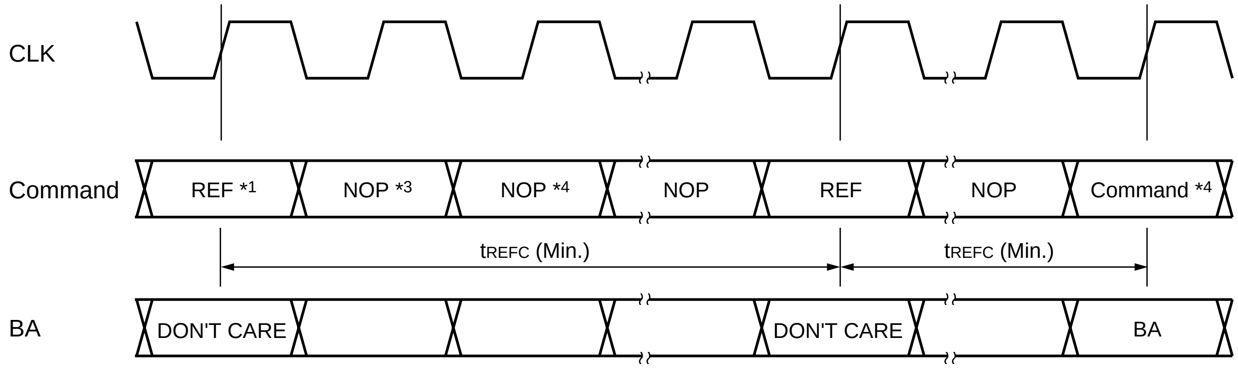
*1: If the final data is masked by DQM, the precharge does not start at the clock of the final data input.

*2: Once the auto precharge command is asserted, no new command within the same bank can be issued.

*3: The Auto-precharge command can not be invoked at full column burst operation.

*4: The Next command should be issued after (BL – 1) + t_{DAL} from the WRITA command.

TIMING DIAGRAM – 15 : AUTO-REFRESH TIMING



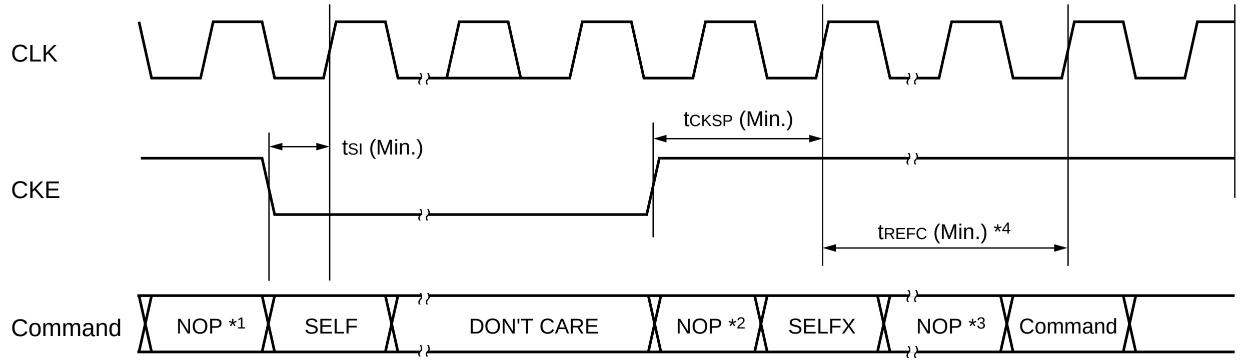
*1: All banks should be precharged prior to the first Auto-refresh command (REF) .

*2: Bank select is ignored at the REF command. The refresh address and bank select are selected by the internal refresh counter.

*3: Either the NOP or DESL command should be asserted within t_{RC} period while Auto-refresh mode.

*4: Any activation command such as the ACTV or MRS commands other than the REF command should be asserted after t_{REFC} from the last REF command.

TIMING DIAGRAM – 16 : SELF-REFRESH ENTRY AND EXIT TIMING



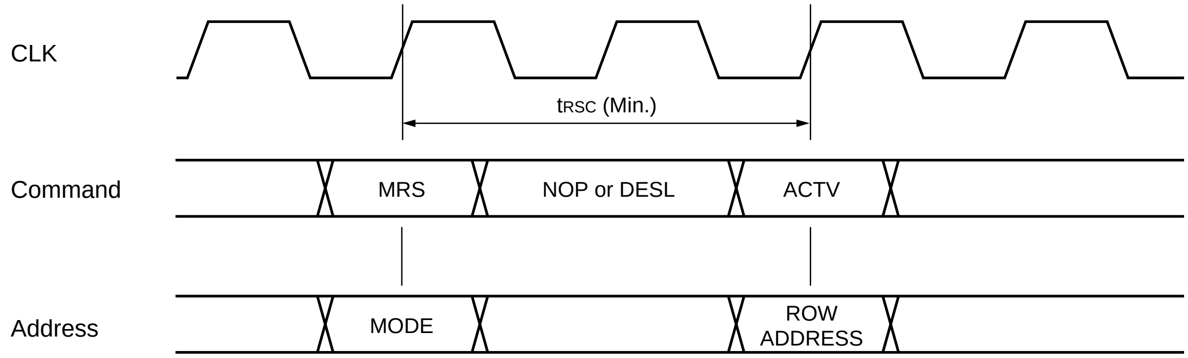
*1: The Precharge command (PRE or PALL) should be asserted if any bank is active prior to the Self-refresh Entry command (SELF) .

*2: The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (Min.) . It is recommended to apply the NOP command in conjunction with CKE.

*3: Either the NOP or DESL command can be used during t_{RC} period.

*4: CKE should be held high for at least one t_{REFC} period after t_{CKSP}.

TIMING DIAGRAM – 17 : MODE REGISTER SET TIMING



Note : The Mode Register Set command (MRS) should be asserted only after all banks have been precharged and DQ is in High-Z.

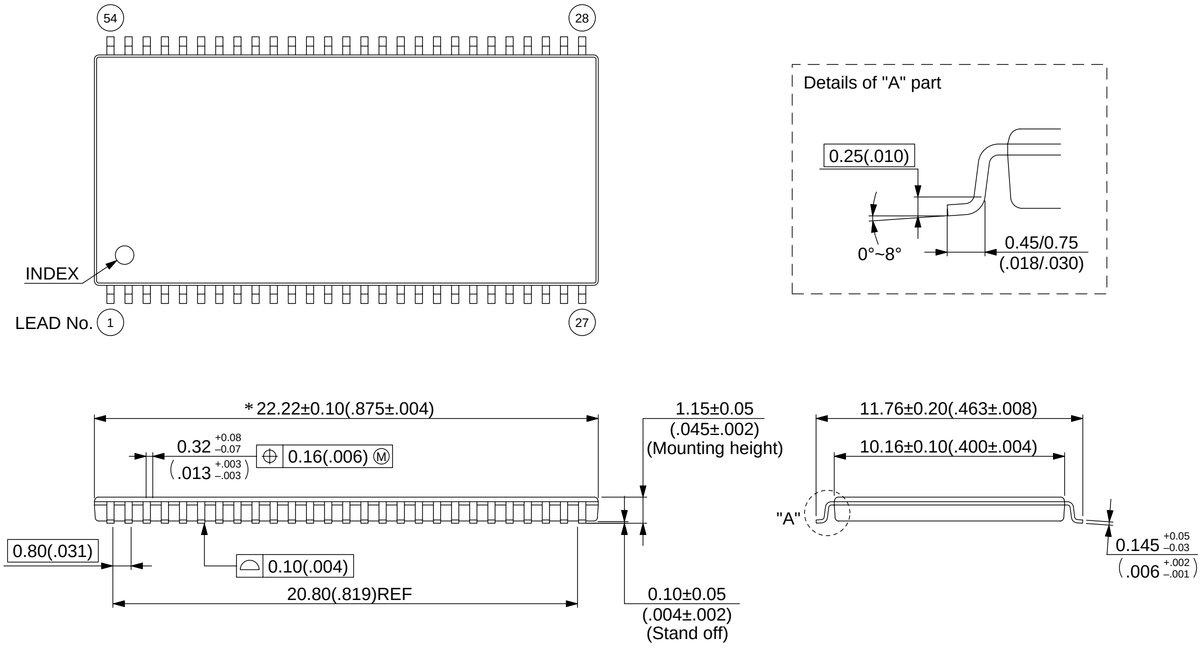
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB81E161622-10FH MB81E161622-12FH	Plastic TSOP (II) , 54 pin (FPT-54P-M02)	

■ PACKAGE DIMENSION

54-pin plastic TSOP (II)
(FPT-54P-M02)

* : Resin protrusion. (Each side : 0.15 (.006) MAX)



Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

F0104

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.