FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11404-1E

MEMORY Low Power SRAM Interface FCRAM™

CMOS

16 Mbit (1 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82D01171A-90/-90L/-90LL

CMOS 1,048,576-WORD × 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

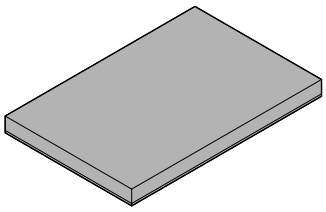
The Fujitsu MB82D01171A is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This MB82D01171A is suited for low power applications such as Cellular Handset and PDA.

■ PRODUCT LINEUP

Parameter	MB82D01171A		
	90	90L	90LL
Read Cycle Time (Min.)	90 ns		
Active Current (Max.) (I_{DDA1})	20 mA		
Standby Current (Max.) (I_{DDS1})	200 µA Max.	100 µA Max.	70 µA Max.
Power Down Current (Max.) (I_{DDP})	10 µA		

■ PACKAGES

48-pin plastic FBGA



(BGA-48P-M16)

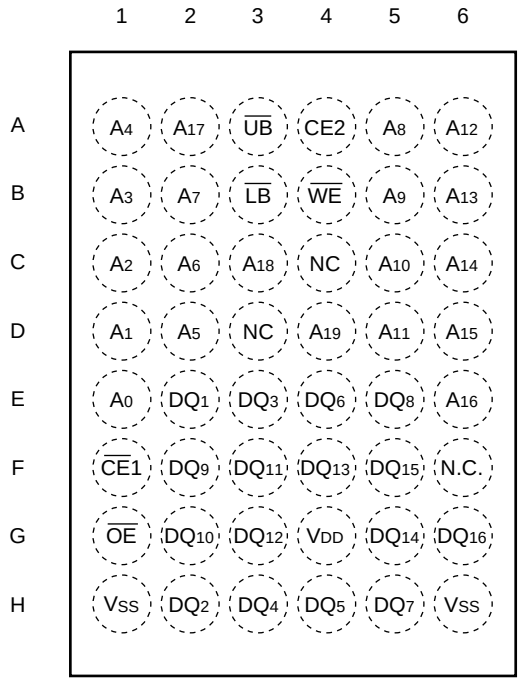
Note: FCRAM is a trademark of Fujitsu Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- 1 M × 16 organization
- Fast Random Cycle Time: t_{RC} = 90 ns
- Low Power Consumption
  V_{DD} standby current: 90: 200 µA
  90L: 100 µA
  90LL: 70 µA
- Wide Operating Condition
  V_{DD} = +2.3 V to +2.7 V or
  +2.7 V to +3.1 V
  T_A = –25 °C to +85 °C
- Byte Write Control
- 4 words Address Access Capability
- Power Down Control by CE2
  V_{DD} power down current: 10 µA

■ PIN ASSIGNMENT

(Top View)

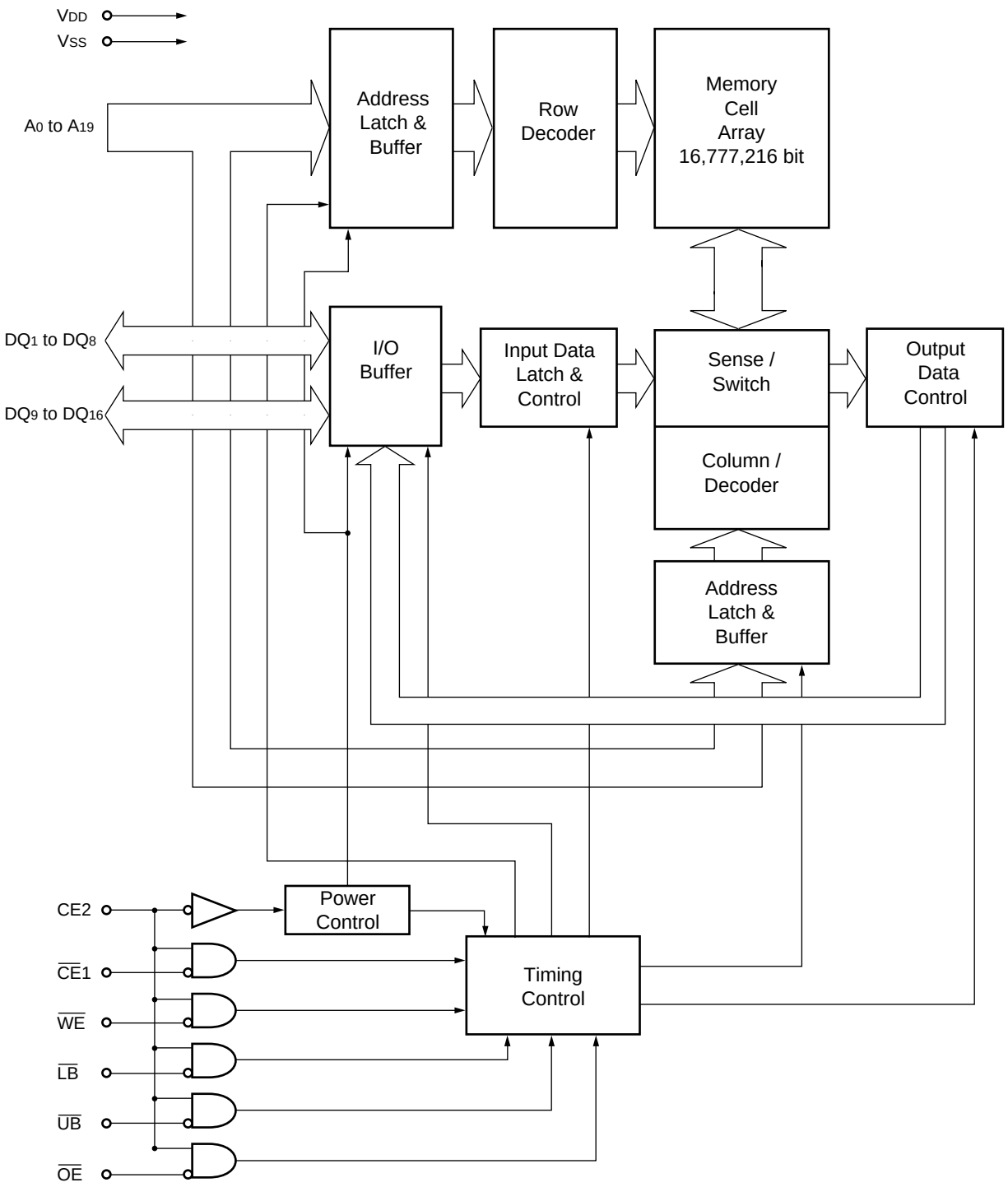


(BGA-48P-M16)

■ PIN DESCRIPTION

Pin Name	Description
A_0 to A_{19}	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Write Control (Low Active)
$\overline{UB}$	Upper Byte Write Control (Low Active)
DQ_{1-8}	Lower Byte Data Input/Output
DQ_{9-16}	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE *1

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ_{1-8}	DQ_{9-16}	I_{DD}	Data Retention
Power Down *2	X	L	X	X	X	X	High-Z	High-Z	I_{DDP}	No
Standby (Deselect)	H	H	X	X	X	X	High-Z	High-Z	I_{DDS}	Yes
Output Disable*3	L	H	H	H	X	X	High-Z	High-Z	I_{DDA}	Yes
Read*4	L	H	H	L	X	X	Output Valid	Output Valid	I_{DDA}	Yes
Write	L	H	L	H	L	L	Input Valid	Input Valid	I_{DDA}	Yes
Write (Lower Byte)	L	H	L	H	L	H	Input Valid	Invalid	I_{DDA}	Yes
Write (Upper Byte)	L	H	L	H	H	L	Invalid	Input Valid	I_{DDA}	Yes

*1 : V = Valid, L = Logic Low, H = Logic High, X = either “L” or “H”, High-Z = High Impedance

*2 : Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.

*3 : Output Disable mode should not be kept longer than 1 μs.

*4 : Byte control at Read mode is not supported.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	–0.5	+3.3	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}	–0.5	+3.3	V
	V_{OUT}	–0.5	+3.3	V
Short Circuit Output Current	I_{OUT}	–50	+50	mA
Storage Temperature	T_{STG}	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage *1	V_{DD} (27)	2.7	3.1	V
	V_{DD} (23)	2.3	2.7	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2	V_{IH} (27)	2.2	V_{DD} + 0.3	V
	V_{IH} (23)	2.0	V_{DD} + 0.3	V
Low Level Input Voltage *1, *2	V_{IL} (27)	–0.3	0.5	V
	V_{IL} (23)	–0.3	0.4	V
Ambient Temperature	T_A	–25	85	°C

*1 : All voltages are referenced to V_{SS}.

*2 : Minimum DC voltage on input or I/O pins are –0.3 V. During voltage transitions, inputs may undershoot V_{SS} to –1.0 V for periods of up to 5 ns. Maximum DC voltage on input and I/O pins are V_{DD} + 0.3 V.
During voltage transitions, inputs may positive overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PIN CAPACITANCE

($f = 1.0$ MHz, $T_A = +25$ °C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Address Input Capacitance	C_{IN1}	$V_{IN} = 0$ V	—	—	5	pF
Control Input Capacitance	C_{IN2}	$V_{IN} = 0$ V	—	—	5	pF
Data Input/Output Capacitance	C_{IO}	$V_{IO} = 0$ V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Conditions		Value			Unit
					Min.	Typ.	Max.	
Input Leakage Current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–1.0	—	+1.0	µA
Output Leakage Current		I_{LO}	$0 \text{ V} \le V_{OUT} \le V_{DD}$, Output Disable		–1.0	—	+1.0	µA
Output High Voltage Level		$V_{OH(27)}$	$V_{DD} = V_{DD(27)}$, $I_{OH} = -0.5$ mA		2.1	—	—	V
		$V_{OH(23)}$	$V_{DD} = V_{DD(23)}$, $I_{OH} = -0.5$ mA		1.8	—	—	V
Output Low Voltage Level		V_{OL}	$I_{OL} = 1$ mA		—	—	0.4	V
V_{DD} Power Down Current		I_{DDP}	$V_{DD} = V_{DD}$ Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE2} \ge V_{DD} - 0.2$ V		—	—	10	µA
V_{DD} Standby Current	-90	I_{DDS}	$V_{DD} = V_{DD}$ Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE1} = CE2 = V_{IH}$, $I_{OUT} = 0$ mA		—	1.5	5	mA
	-90L				—	1	1.5	
	-90LL				—	0.5	1	
	-90	I_{DDS1}	$V_{DD} = V_{DD}$ Max., $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} - 0.2$ V, $\overline{CE1} = CE2 \ge V_{DD} - 0.2$ V, $I_{OUT} = 0$ mA		—	—	200	µA
	-90L				—	—	100	
	-90LL				—	—	70	
V_{DD} Active Current		I_{DDA1}	$V_{DD} = V_{DD}$ Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA	t_{RC} / t_{WC} = Min.	—	15	20	mA
		I_{DDA2}		t_{RC} / t_{WC} = Max.	—	2.5	3.0	mA

Notes: • All voltages are referenced to Vss.
• DC Characteristics are measured after following POWER-UP timing.
• I_{OUT} depends on the output load conditions.

2. AC Characteristics

(1) Read Operation

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{RC}	90	1000	ns	*1
Chip Enable Access Time	t_{CE}	—	90	ns	*2, *4
Output Enable Access Time	t_{OE}	—	45	ns	*2
Address Access Time	t_{AA}	—	90	ns	*2, *5
Output Data Hold Time	t_{OH}	5	—	ns	*2
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*3
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*3
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	30	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	25	ns	*3
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	45	—	ns	*4, *6
	$t_{ASO[ABS]}$	10	—	ns	*7
Address Invalid Time	t_{AX}	—	5	ns	*5
$\overline{CE}1$ Low to Address Hold Time	t_{CLAH}	90	—	ns	*5
$\overline{OE}$ Low to Address Hold Time	t_{OLAH}	45	—	ns	*5, *8
$\overline{CE}1$ High to Address Hold Time	t_{CHAH}	–5	—	ns	
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	0	—	ns	
$\overline{CE}1$ Low to $\overline{OE}$ Low Delay Time	t_{CLOL}	45	1000	ns	*4, *6, *8, *9
$\overline{OE}$ Low to $\overline{CE}1$ High Delay Time	t_{OLCH}	45	—	ns	*8
$\overline{CE}1$ High Pulse Width	t_{CP}	20	—	ns	
$\overline{OE}$ High Pulse Width	t_{OP}	45	1000	ns	*6, *8, *9
	$t_{OP[ABS]}$	20	—	ns	*7

*1: Maximum value is a reference.

*2: The output load is 30 pF.

*3: The output load is 5 pF.

*4: The t_{CE} is applicable if $\overline{OE}$ is brought to Low before $\overline{CE}1$ goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.

*5: Applicable only to A_0 and A_1 when both $\overline{CE}1$ and $\overline{OE}$ are kept at Low for the address access.

*6: The t_{ASO}, t_{CLOL} (Min.) and t_{OP} (Min.) are reference values when the access time is determined by t_{OE}.
If actual value of each parameter is shorter than specified minimum value, t_{OE} become longer by the amount of subtraction actual value from specified minimum value.
For example, if actual t_{ASO}, t_{ASO} (actual) , is shorter than specified minimum value, t_{ASO} (Min.) , during $\overline{OE}$ control access (i.e., $\overline{CE}1$ stays Low) , the t_{OE} become t_{OE} (Max.) + t_{ASO} (Min.) – t_{ASO} (actual) .

*7: The $t_{ASO[ABS]}$ and $t_{OP[ABS]}$ is the absolute minimum value during $\overline{OE}$ control access.

*8: If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC} (Min.) – t_{CLOL} (actual) or t_{RC} (Min.) – t_{OP} (actual) .

*9: Maximum value is applicable if $\overline{CE}1$ is kept at Low.

(2) Write Operation

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{WC}	90	1000	ns	*1
Address Setup Time	t_{AS}	0	—	ns	*2
Address Hold Time	t_{AH}	45	—	ns	*2
$\overline{CE}1$ Write Setup Time	t_{CS}	0	1000	ns	
$\overline{CE}1$ Write Hold Time	t_{CH}	0	1000	ns	
$\overline{WE}$ Setup Time	t_{WS}	0	—	ns	
$\overline{WE}$ Hold Time	t_{WH}	0	—	ns	
$\overline{LB}$ and $\overline{UB}$ Setup Time	t_{BS}	–5	—	ns	
$\overline{LB}$ and $\overline{UB}$ Hold Time	t_{BH}	–5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	1000	ns	*3
$\overline{OE}$ Hold Time	t_{OEH}	45	1000	ns	*3, *4
	$t_{OEH[ABS]}$	20	—	ns	*5
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time	t_{OHCL}	–3	—	ns	*6
Address Hold Time to $\overline{OE}$ High	t_{OHAH}	0	—	ns	*7
$\overline{CE}1$ Write Pulse Width	t_{CW}	60	—	ns	*1, *8
$\overline{WE}$ Write Pulse Width	t_{WP}	60	—	ns	*1, *8
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	ns	*1, *9
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*1, *3, *9
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{CE}1$ High Pulse Width	t_{CP}	20	—	ns	*9

*1: Maximum value is a reference.
Minimum value must be equal or greater than the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}) .

*2: New write address is valid from either $\overline{CE}1$ or $\overline{WE}$ is brought to High.

*3: Maximum value is applicable if $\overline{CE}1$ is kept at Low and both $\overline{WE}$ and $\overline{OE}$ are kept at High.

*4: The t_{OEH} is specified from end of t_{WC} (Min.) .

*5: The $t_{OEH[ABS]}$ is the absolute minimum value if write cycle is terminated by $\overline{WE}$ and $\overline{CE}1$ stays Low.

*6: t_{OHCL} (Min.) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL} (Min.) , $\overline{WE}$ Low must be asserted after t_{RC} (Min.) from $\overline{CE}1$ Low.
In other words, read operation is initiated if t_{OHCL} (Min.) is not satisfied.

*7: Applicable if $\overline{CE}1$ stays Low after read operation.

*8: t_{CW} and t_{WP} is applicable if write operation is initiated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*9: t_{WRC} and t_{WR} is applicable if write operation is terminated by $\overline{CE}1$ and $\overline{WE}$, respectively.
The t_{WR} (Min.) can be ignored if $\overline{CE}1$ is brought to High together or after $\overline{WE}$ is brought to High.
In such case, the t_{CP} (Min.) must be satisfied.

(3) Power Down Parameters

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	100	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit	t_{CHH}	350	—	µs	
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	10	—	ns	

(4) Other Timing Parameters

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	20	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	20	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	350	—	µs	
Input Transition Time	t_T	1	25	ns	*2

*1: It may write some data into any address location if t_{CHWX} is not satisfied.

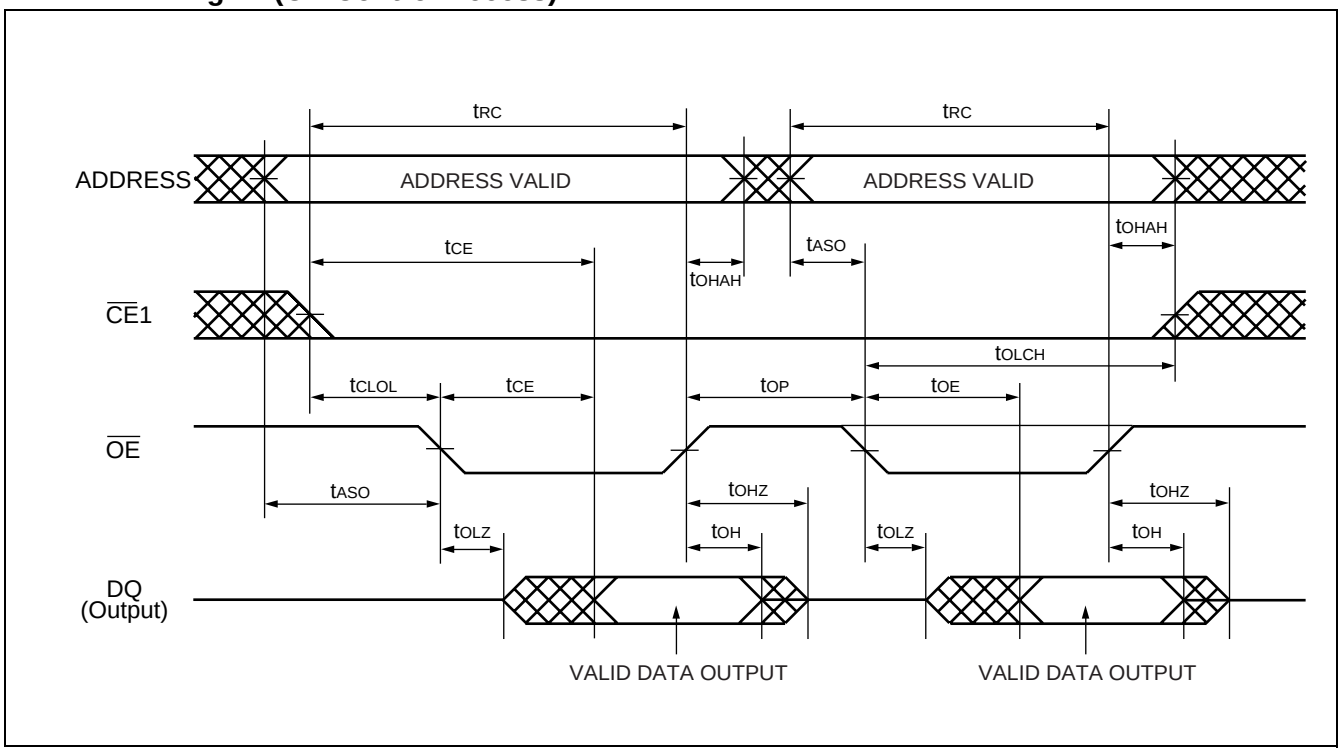
*2: The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.

(5) AC Test Conditions

Parameter	Symbol	Conditions	Measured Value	Unit	Note
Input High Level	V_{IH}	V_{DD} = 2.7 V to 3.1 V	2.3	V	
		V_{DD} = 2.3 V to 2.7 V	2.0	V	
Input Low Level	V_{IL}	V_{DD} = 2.7 V to 3.1 V	0.4	V	
		V_{DD} = 2.3 V to 2.7 V	0.4	V	
Input Timing Measurement Level	V_{REF}	V_{DD} = 2.7 V to 3.1 V	1.3	V	
		V_{DD} = 2.3 V to 2.7 V	1.1	V	
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns	

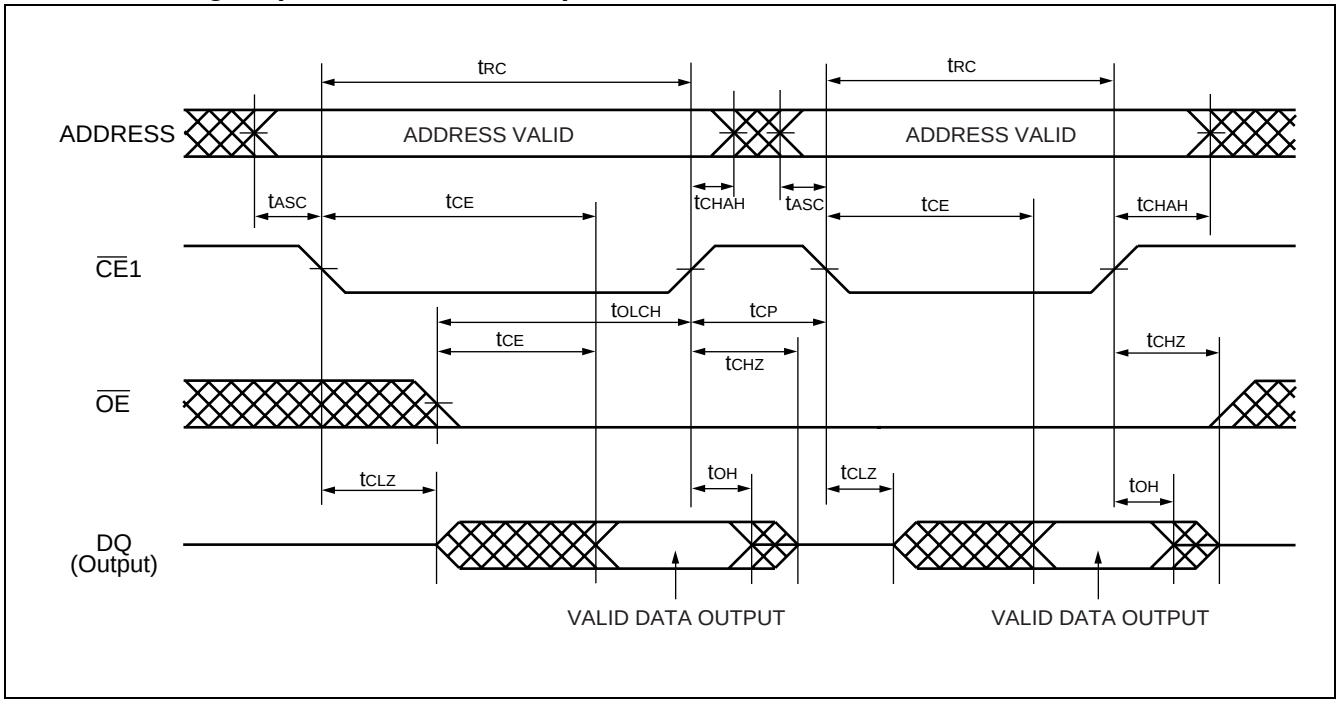
■ TIMING DIAGRAM

1. READ Timing #1 ($\overline{OE}$ Control Access)



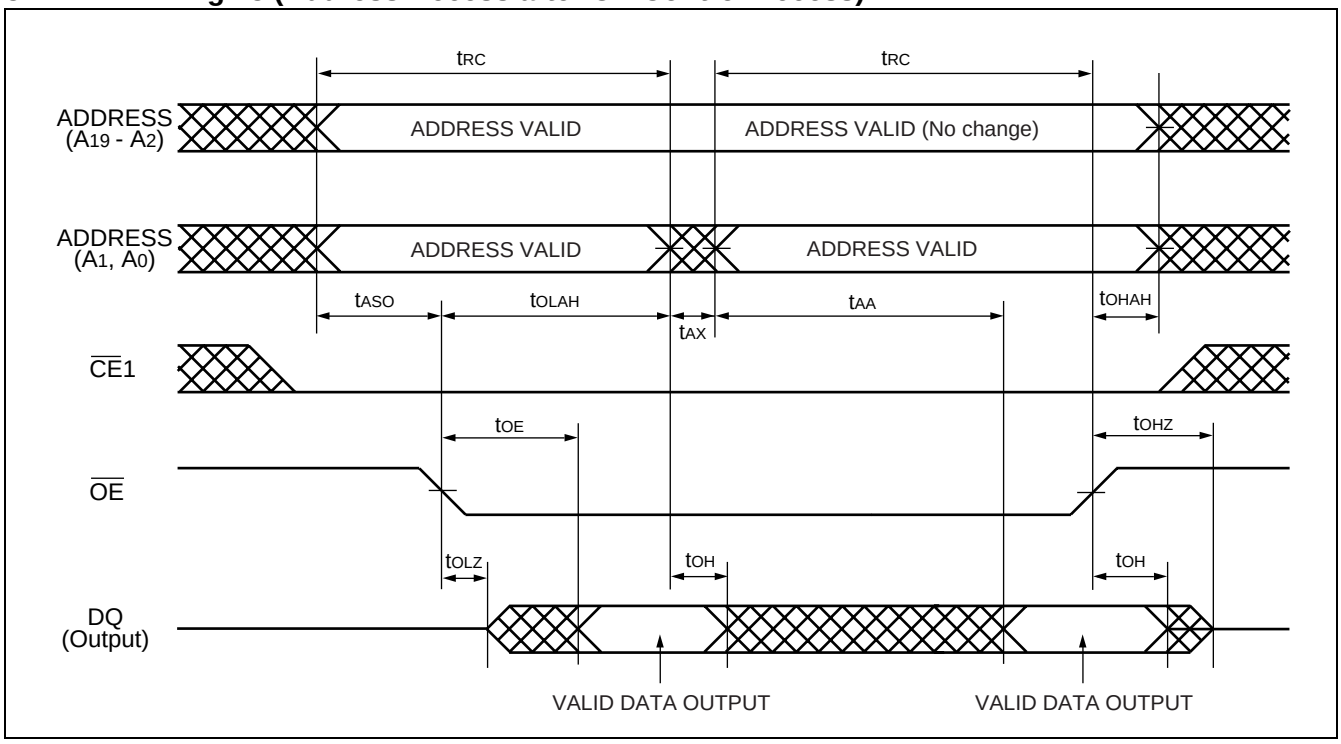
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

2. READ Timing #2 ($\overline{CE}$1 Control Access)



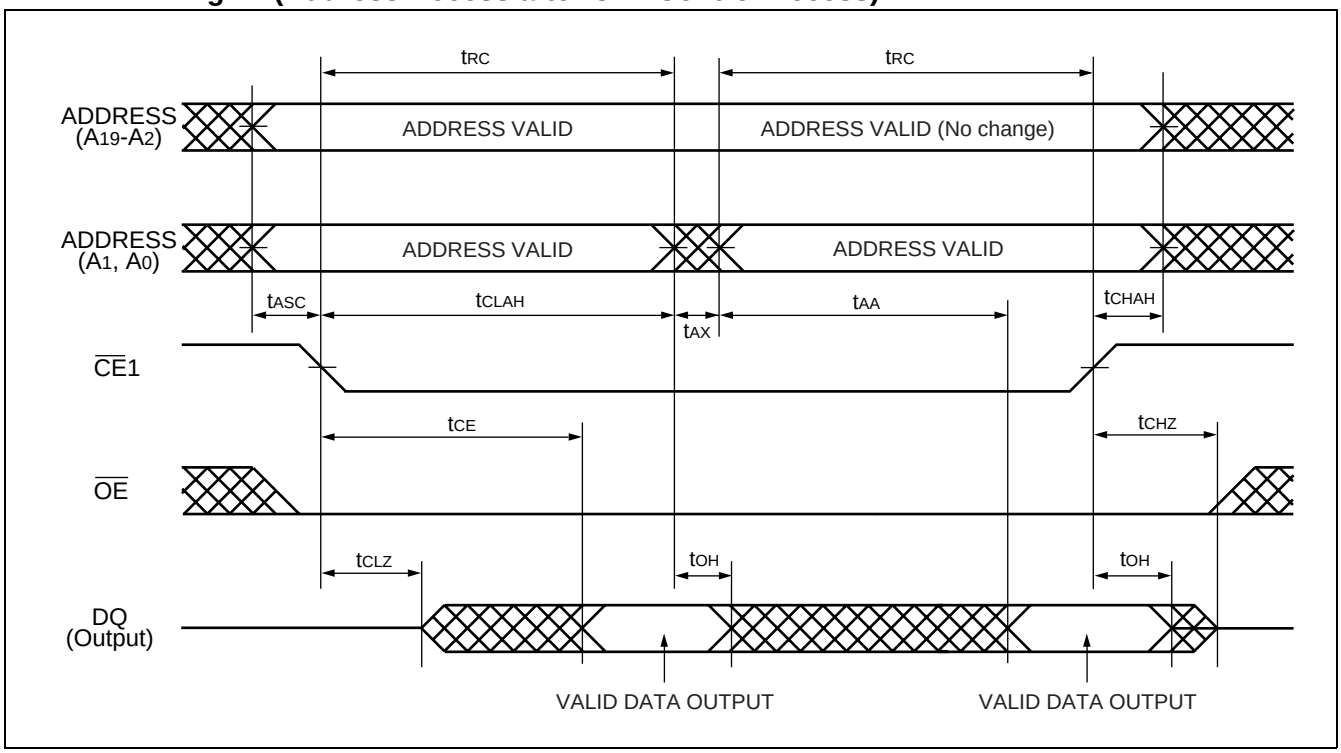
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

3. READ Timing #3 (Address Access after $\overline{OE}$ Control Access)



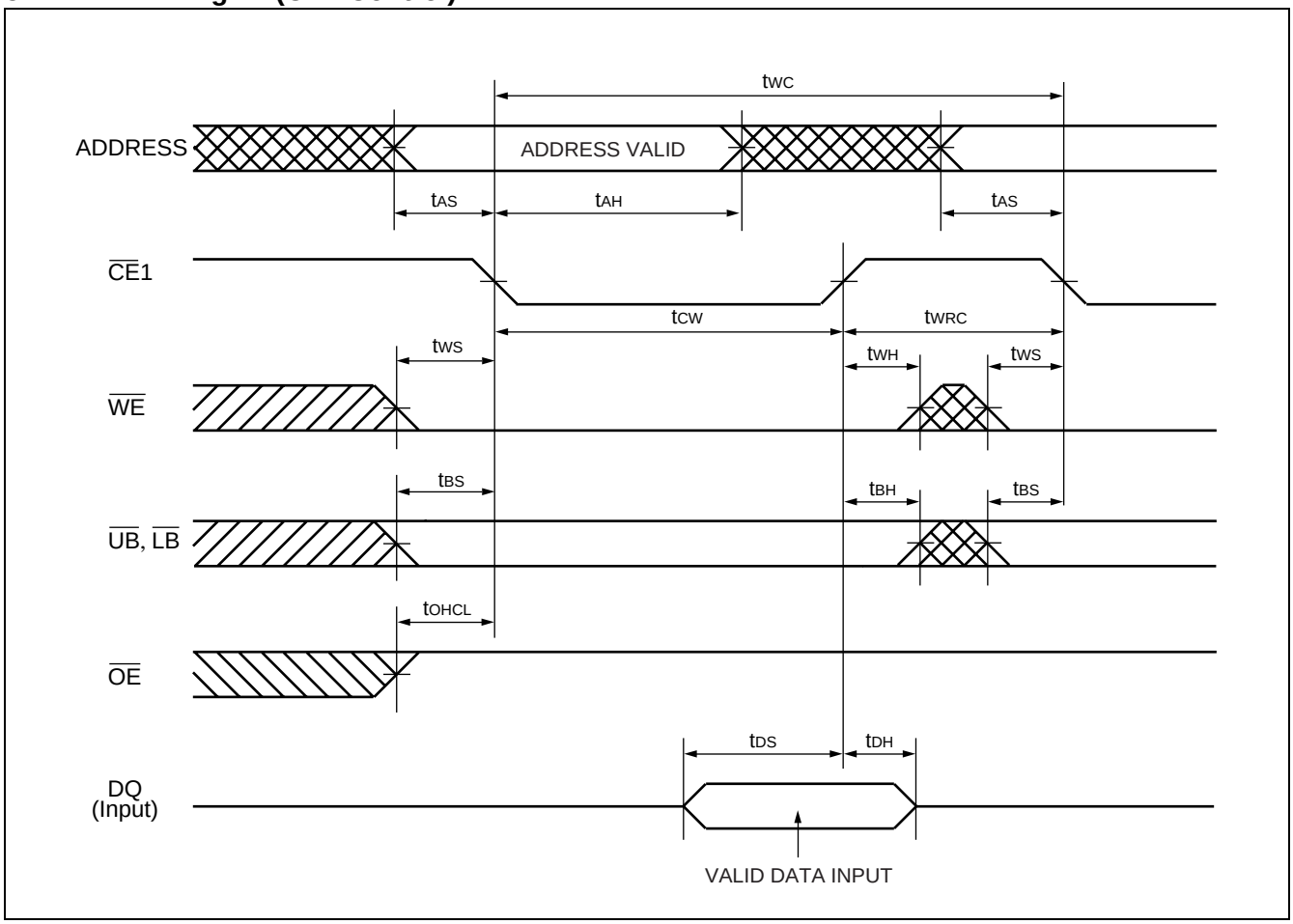
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

4. READ Timing #4 (Address Access after $\overline{CE}$1 Control Access)



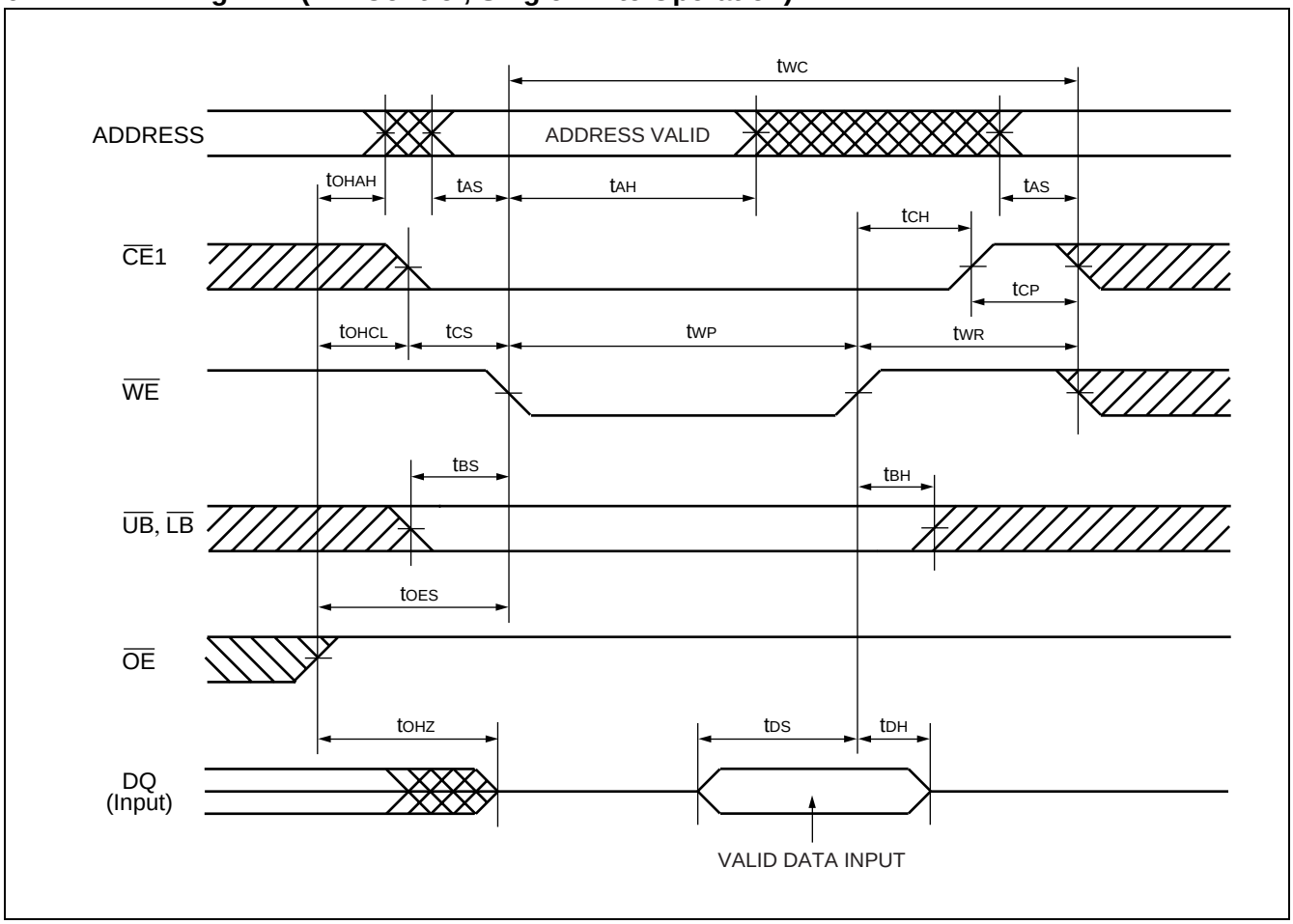
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

5. WRITE Timing #1 ($\overline{CE}$1 Control)



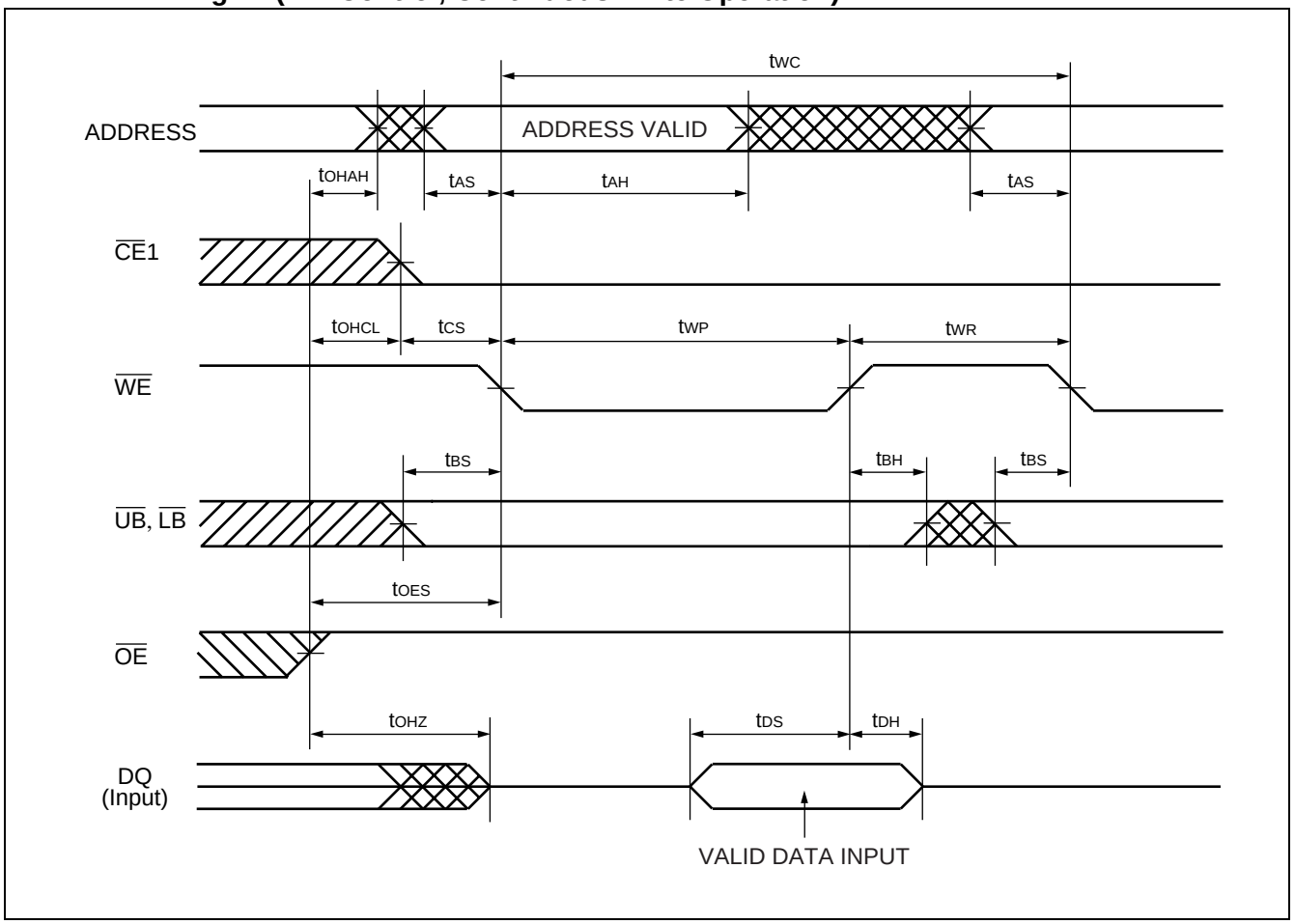
Note : CE2 must be High for write cycle.

6. WRITE Timing #2-1 ($\overline{WE}$ Control, Single Write Operation)



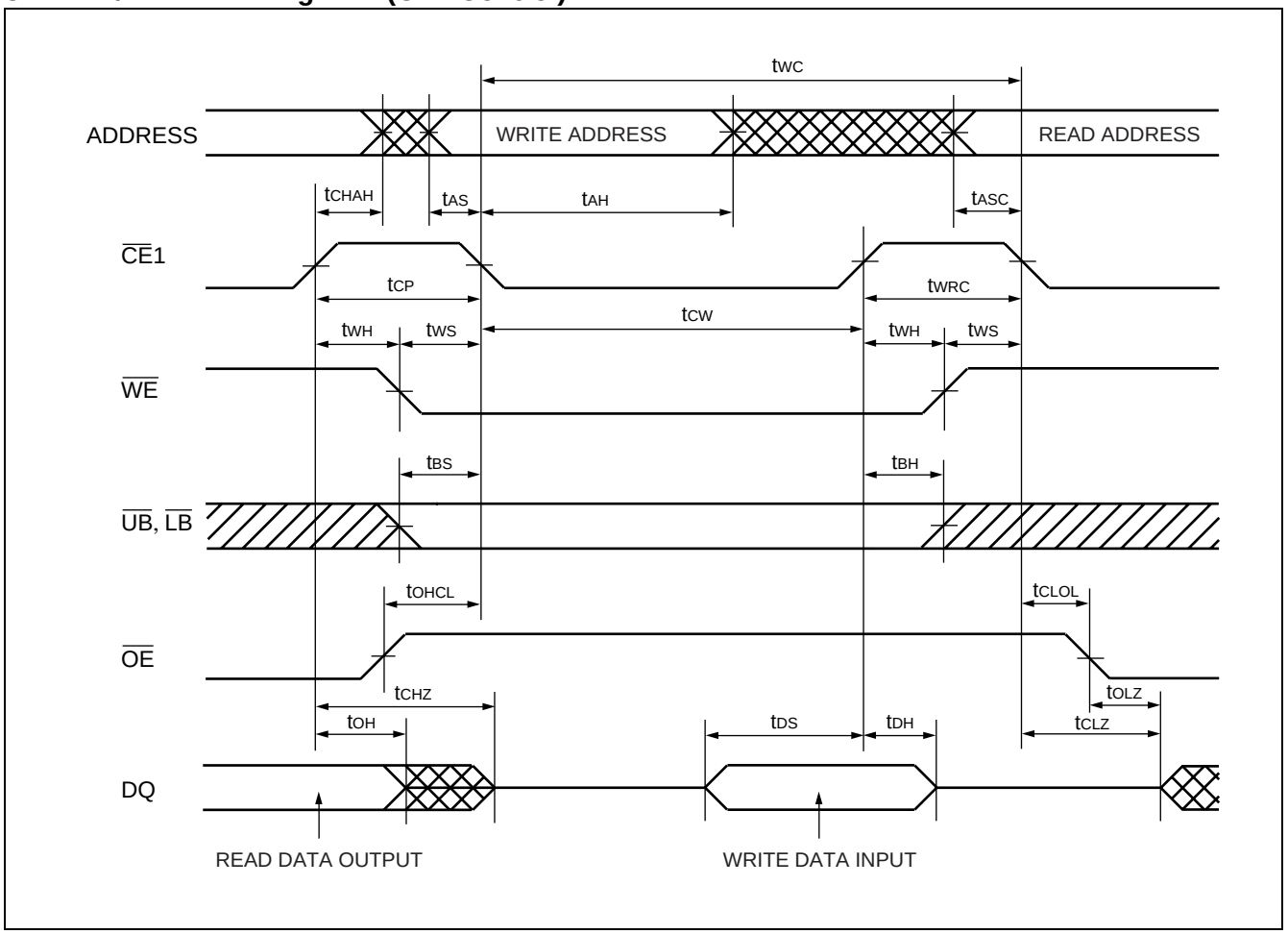
Note : CE2 must be High for write cycle.

7. WRITE Timing #2 ($\overline{WE}$ Control, Continuous Write Operation)



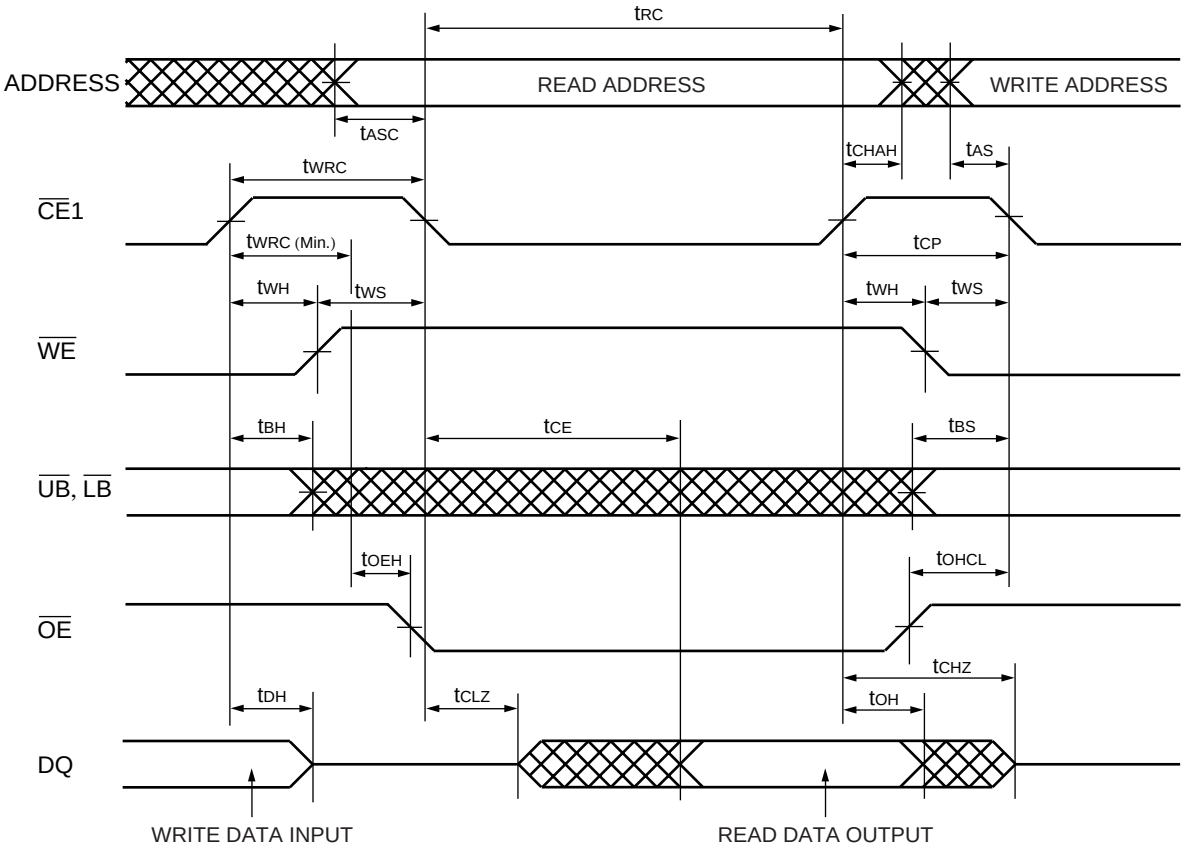
Note : CE2 must be High for write cycle.

8. READ/WRITE Timing #1-1 ($\overline{CE}$1 Control)



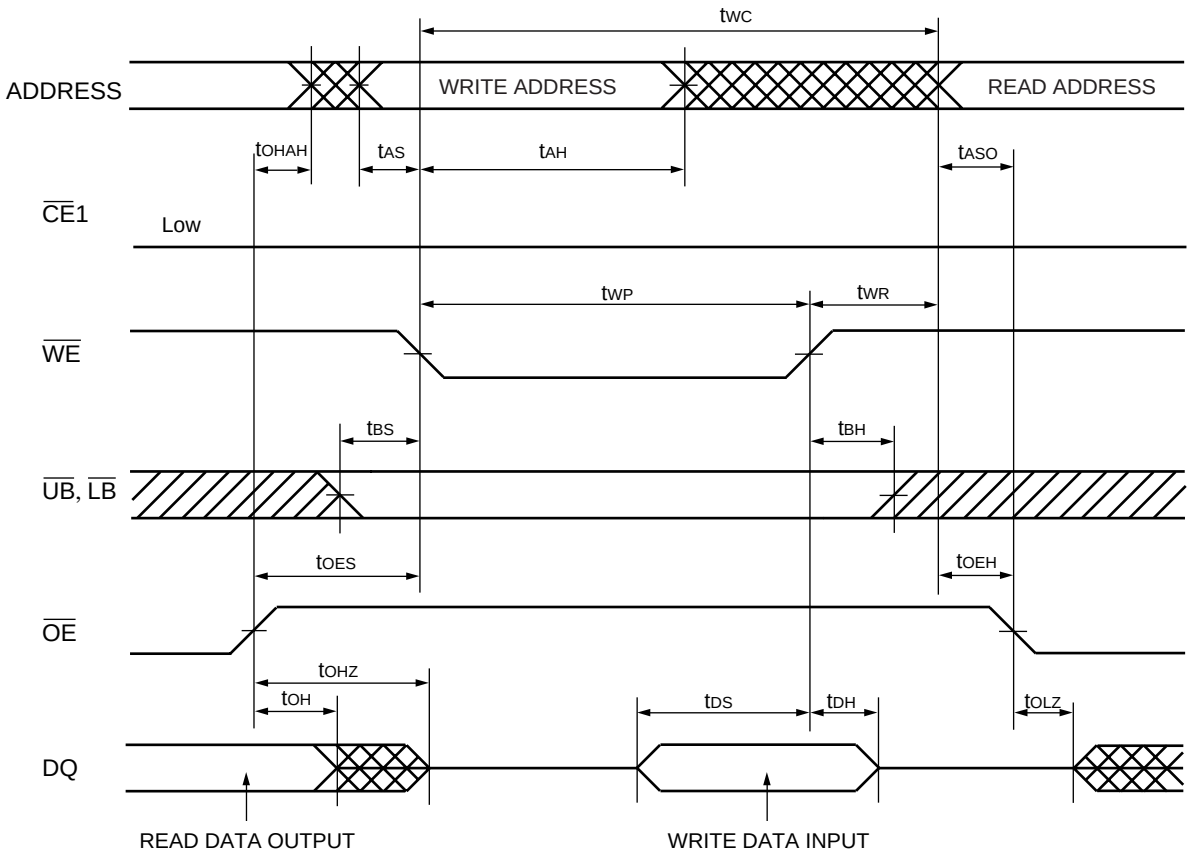
Note : Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

9. READ/WRITE Timing #1-2 ($\overline{CE}$1 Control)



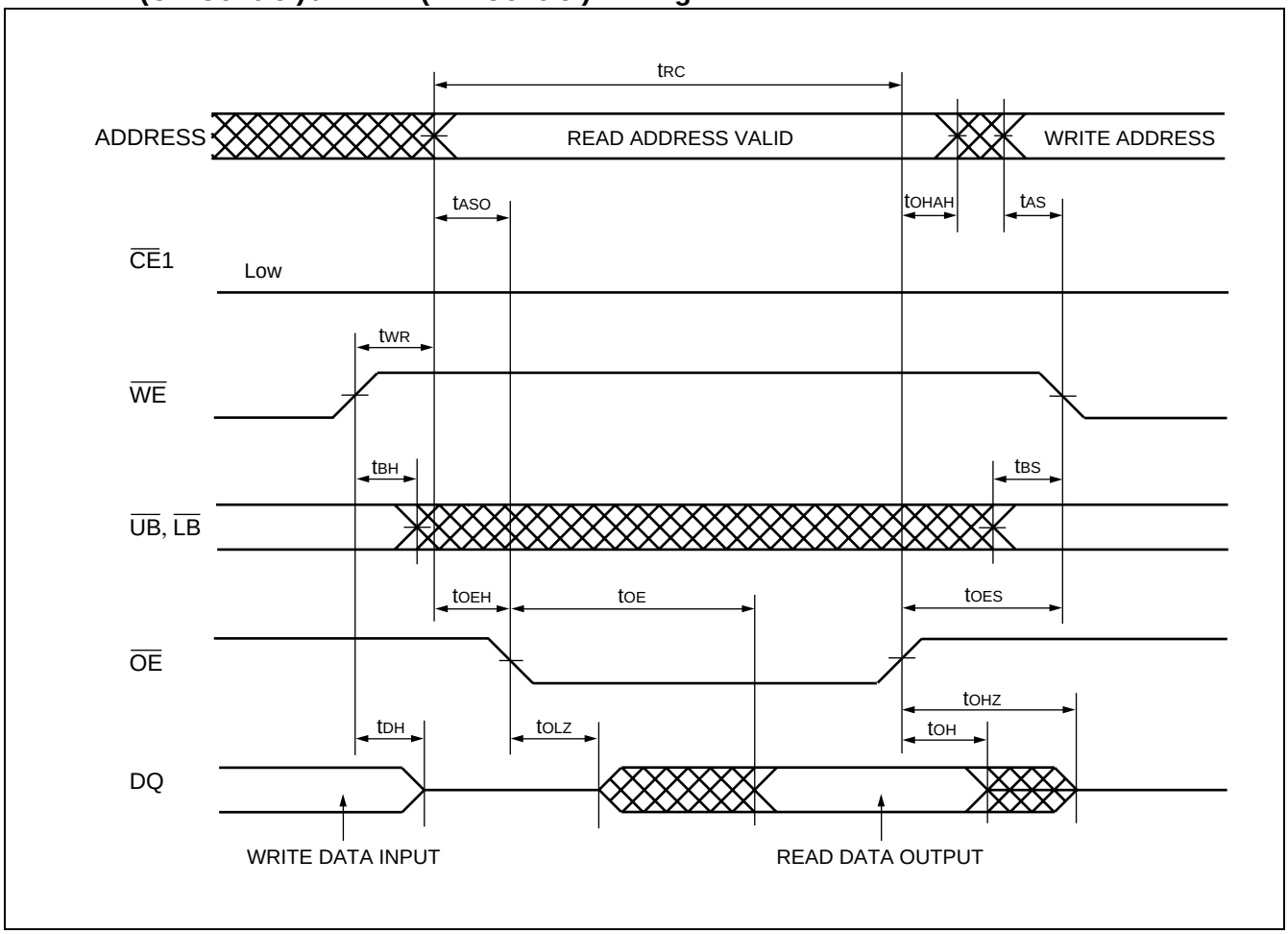
Note : The t_{OEH} is specified from the time satisfied both t_{WRC} and t_{WR} (Min.) .

10. READ ($\overline{OE}$ Control) /WRITE ($\overline{WE}$ Control) Timing #2-1



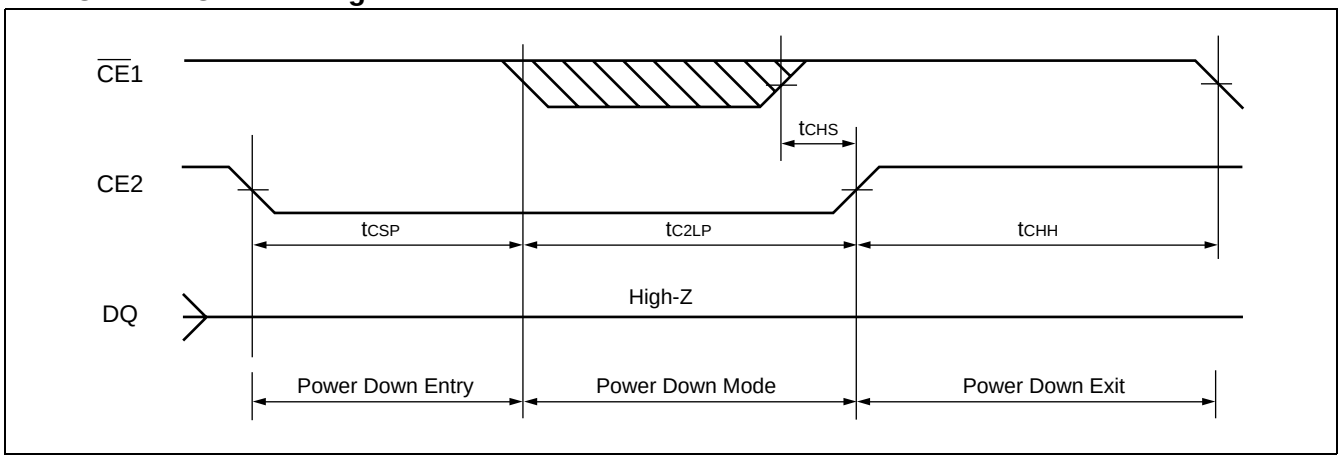
Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to Low, output is exclusively controlled by $\overline{OE}$.

11. READ ($\overline{OE}$ Control) /WRITE ($\overline{WE}$ Control) Timing #2-2

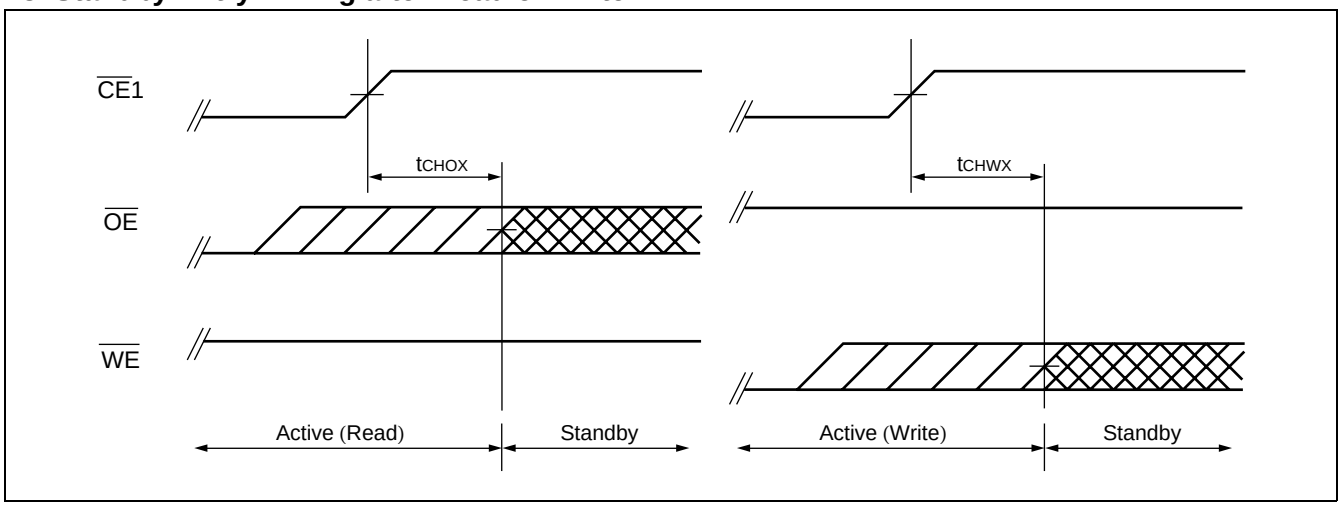


Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to Low, output is exclusively controlled by $\overline{OE}$.

12. POWER DOWN Timing

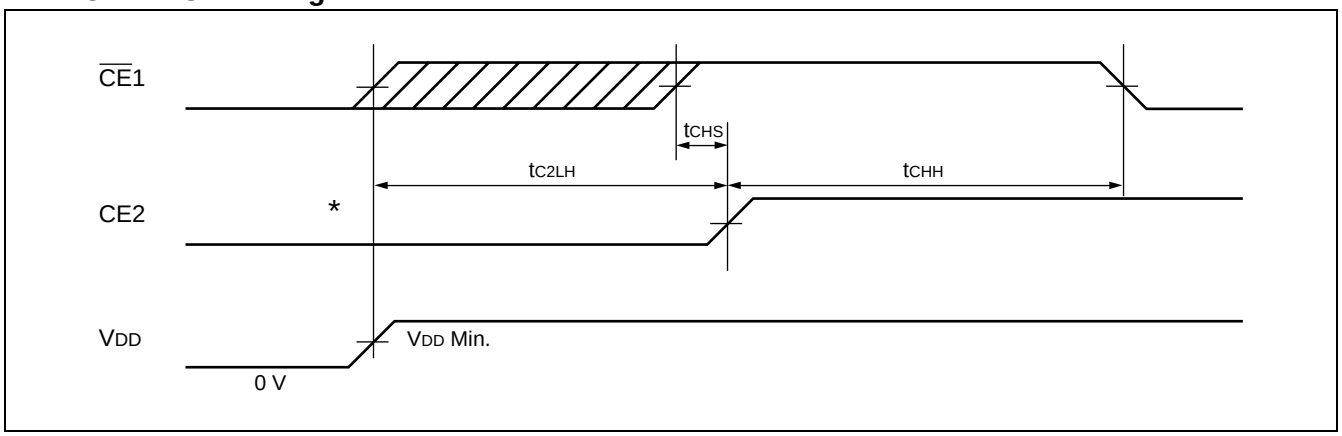


13. Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (Min.) period from either last address transition of A_0 and A_1, or $\overline{CE}1$ Low to High transition.

14. POWER-UP Timing



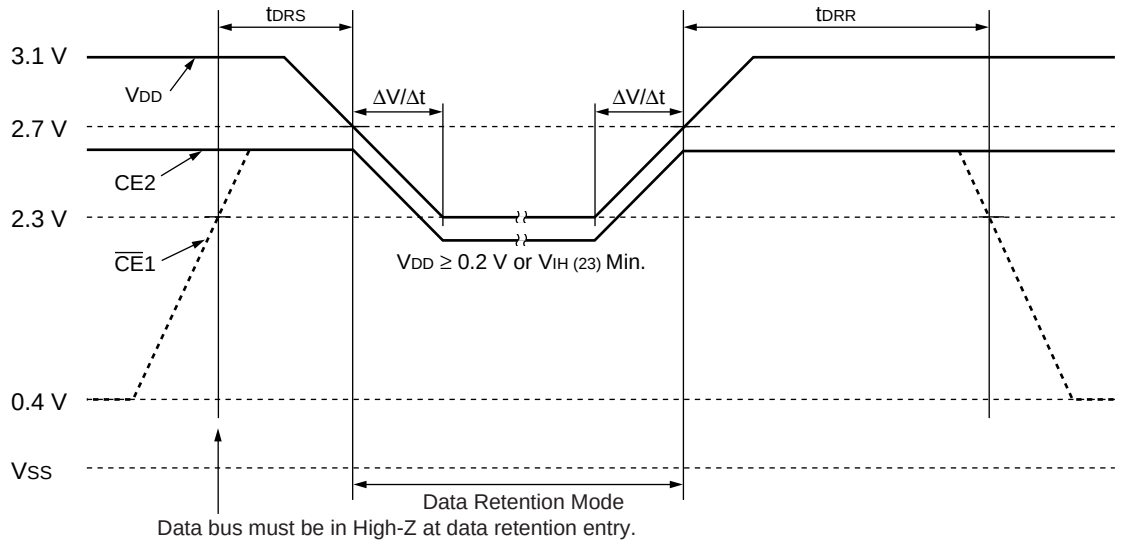
*: It is recommended CE2 to kept at Low during V_{DD} power-up.
The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

■ DATA RETENTION

1. Low V_{DD} Characteristics

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD} Data Retention Supply Voltage		V_{DR}	$\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V or, $\overline{CE}1 = CE2 = V_{IH}$,	2.3	—	3.1	V
V_{DD} Data Retention Supply Current	-90	I_{DR}	$V_{DD} = V_{DD\,(23)}$, $V_{IN} = V_{IH\,(23)}$ or V_{IL}, $\overline{CE}1 = CE2 = V_{IH\,(23)}$, $I_{OUT} = 0$ mA	—	1.5	5	mA
	-90L			—	1	1.5	
	-90LL			—	0.5	1	
	-90	I_{DR1}	$V_{DD} = V_{DD\,(23)}$, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, $\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V, $I_{OUT} = 0$ mA	—	—	200	µA
	-90L			—	—	100	
	-90LL			—	—	70	
Data Retention Setup Time		t_{DRS}	$V_{DD} = V_{DD\,(27)}$ at data retention entry	0	—	—	ns
Data Retention Recovery Time		t_{DRR}	$V_{DD} = V_{DD\,(27)}$ after data retention	90	—	—	ns
V_{DD} Voltage Transition Time		$\Delta V/\Delta t$		0.5	—	—	V/µs

2. Data Retention Timing

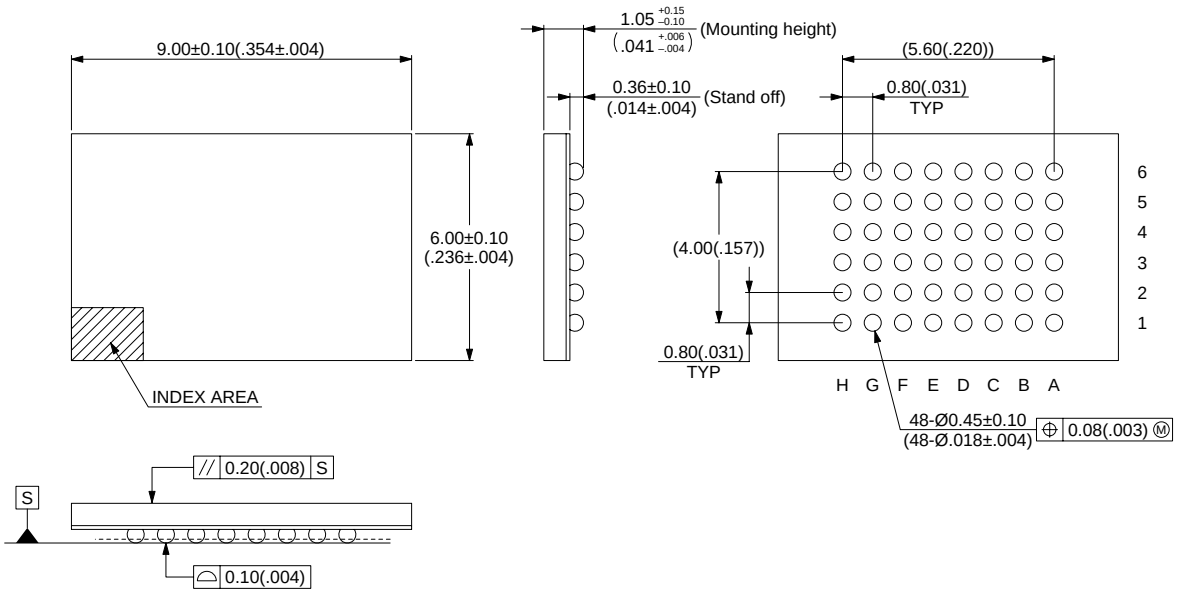


■ ORDERING INFORMATION

Part Number	Package	Remarks
MB82D01171A-90PBT	Plastic FBGA 48-ball (BGA-48P-M16)	
MB82D01171A-90LPBT	Plastic FBGA 48-ball (BGA-48P-M16)	
MB82D01171A-90LLPBT	Plastic FBGA 48-ball (BGA-48P-M16)	

■ PACKAGE DIMENTION (PRELIMINARY)

48-pin plastic FBGA
(BGA-48P-M16)



Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

F0104

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.