FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11409-1E

MEMORY
CMOS

2 × 512K × 32-BIT× 2-PART DUAL PART SINGLE DATA RATE I/F FCRAM™

Consumer/Embedded Application Specific Memory for SiP

MB811L646449-12/18

■ DESCRIPTION

The Fujitsu MB811L646449 is a Dual Part Single Data Rate Interface Fast Cycle Random Access Memory (FCRAM*) containing 33,554,432 memory cells accessible in a 32-bit format for each part. The MB811L646449 features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB811L646449 is utilized using a Fujitsu advanced FCRAM core technology and designed for low power consumption and low voltage operation than regular synchronous DRAM (SDRAM).

The MB811L646449 is dedicated for SiP (System in a package), and ideally suited for various embedded/ consumer applications including digital AVs and image processing where a large band width and low power consumption memory is needed.

*: FCRAM is a trademark of Fujitsu Limited, Japan.

■ PRODUCT LINE

Parameter		MB811L646449-12	MB811L646449-18
Clock Frequency		81 MHz Max	54 MHz Max
CL - t_{RCD} - t_{RP}	CL = 2	2 - 2 - 2 Min	2 - 2 - 2 Min
Burst Mode Cycle Time	CL = 2	12 ns Min	18 ns Min
Access Time from Clock	CL = 2	9 ns Max	9 ns Max
Operating Current		240 mA Max	160 mA Max
Power Down Mode Current (I_{CC2PS})		2 mA Max	2 mA Max
Self Refresh Current (I_{CC6})		5 mA Max	5 mA Max

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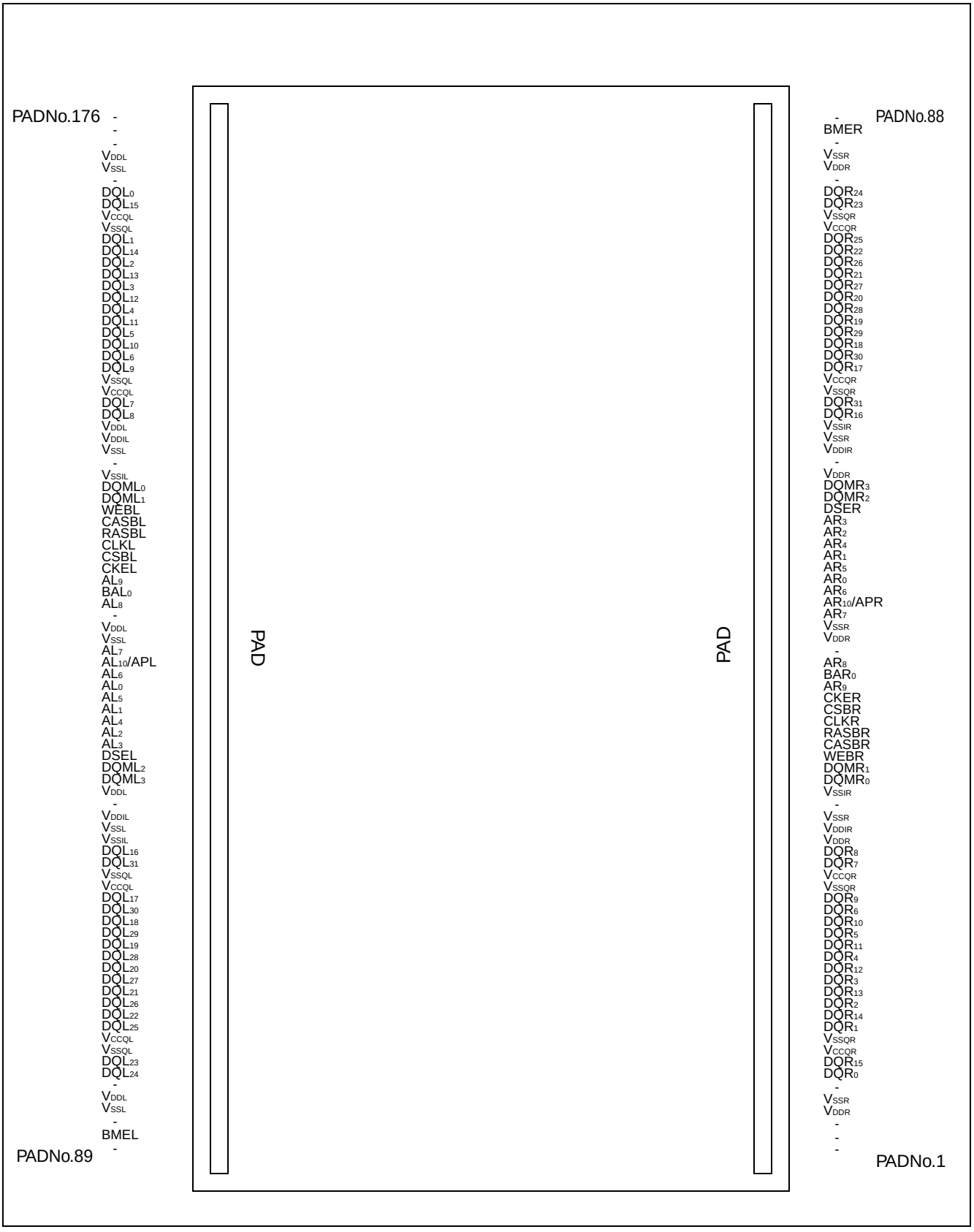
■ FEATURES

- Dual 32M bit (2 banks × 512K words × 32 bits) parts on a single chip
- Independent lines of power supply, address, control and I/O lines for each part
- Configurable as 2 banks × 512K words × 64 bits × 1 part or 4 banks × 512K words × 32 bits × 1 part as well as 2 banks × 512K words × 32 bits × 2 parts, with external line connections
- V_{CCQ}: +3.3 V Supply ±0.3 V tolerance or +2.5 V Supply ±0.2 V tolerance
- V_{DD}: +2.5 V Supply ±0.2 V tolerance
- LVCMOS compatible I/O interface
- 2 K refresh cycles every 32 ms
- Two bank operation for each part
- Large band width with bank interleave operation.
- Burst read/write operation and burst read/single write operation capability
- Programmable burst type and burst length
  Burst type : Sequential Mode, Interleave Mode
  Burst length : BL = 1, 2, 4, 8, full column (256)
- CAS latency=2
- Auto-and Self-refresh
- CKE power down mode
- Byte control with DQM_0 to DQM_3

■ PAD LAYOUT


PADNo.176
-
-
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VDDL
VSSL
-
DQL0
DQL15
VCCQL
VSSQL
DQL1
DQL14
DQL2
DQL13
DQL3
DQL12
DQL4
DQL11
DQL5
DQL10
DQL6
DQL9
VSSQL
VCCQL
DQL7
DQL8
VDDL
VDDIL
VSSL
-
VSSIL
DQML0
DQML1
WEBL
CASBL
RASBL
CLKL
CSBL
CKEL
AL9
BAL0
AL8
-
VDDL
VSSL
AL7
AL10/APL
AL6
AL0
AL5
AL1
AL4
AL2
AL3
DSEL
DQML2
DQML3
VDDL
-
VDDIL
VSSL
VSSIL
DQL16
DQL31
VSSQL
VCCQL
DQL17
DQL30
DQL18
DQL29
DQL19
DQL28
DQL20
DQL27
DQL21
DQL26
DQL22
DQL25
VCCQL
VSSQL
DQL23
DQL24
-
VDDL
VSSL
-
BMEL
-
PADNo.89
PAD
PAD
-
PADNo.88
BMER
-
VSSR
VDDR
-
DQR24
DQR23
VSSQR
VCCQR
DQR25
DQR22
DQR26
DQR21
DQR27
DQR20
DQR28
DQR19
DQR29
DQR18
DQR30
DQR17
VCCQR
VSSQR
DQR31
DQR16
VSSIR
VSSR
VDDIR
-
VDDR
DQMR3
DQMR2
DSER
AR3
AR2
AR4
AR1
AR5
AR0
AR6
AR10/APR
AR7
VSSR
VDDR
-
AR8
BAR0
AR9
CKER
CSBR
CLKR
RASBR
CASBR
WEBR
DQMR1
DQMR0
VSSIR
-
VSSR
VDDIR
VDDR
DQR8
DQR7
VCCQR
VSSQR
DQR9
DQR6
DQR10
DQR5
DQR11
DQR4
DQR12
DQR3
DQR13
DQR2
DQR14
DQR1
VSSQR
VCCQR
DQR15
DQR0
-
VSSR
VDDR
-
-
-
PADNo.1

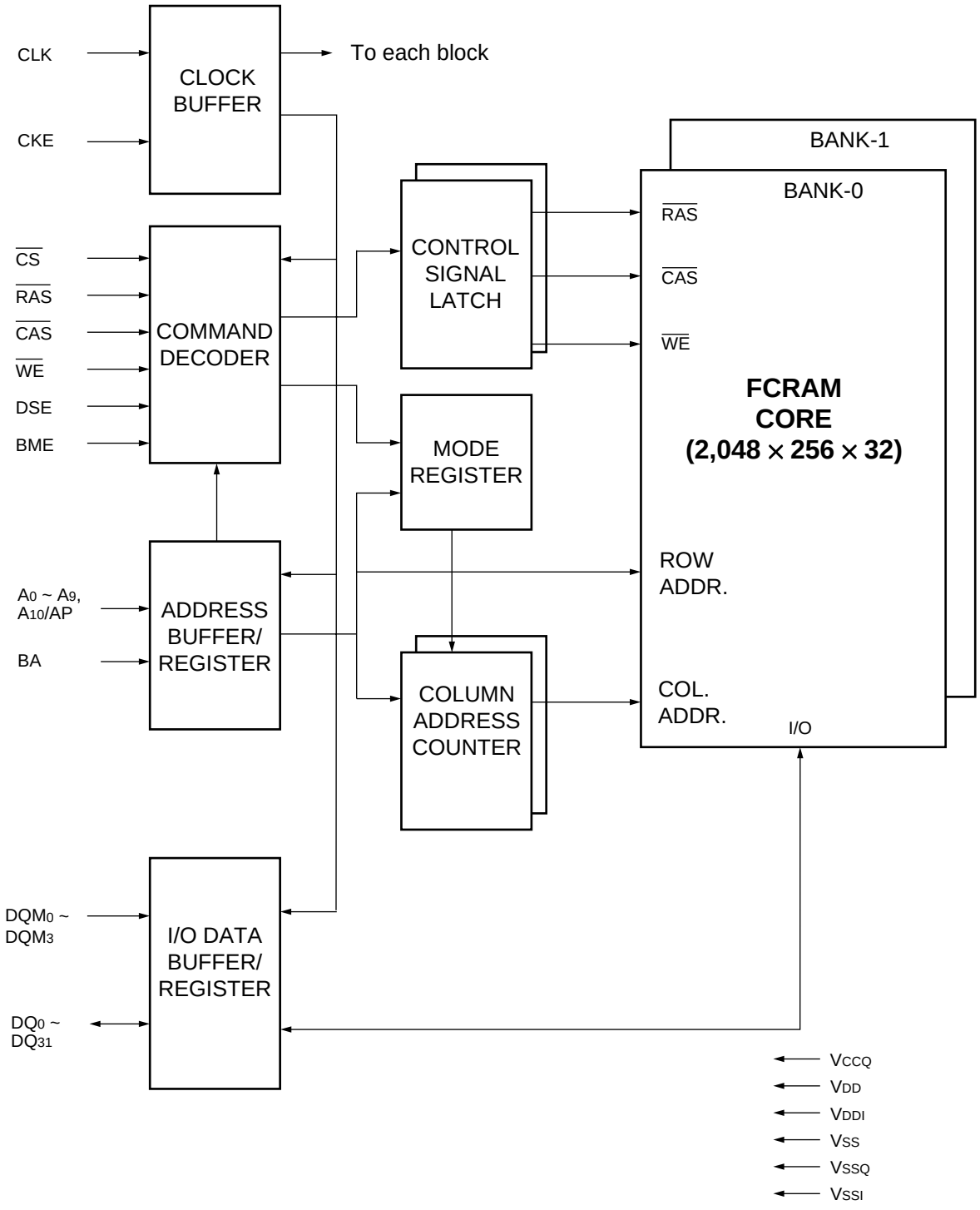
■ PAD DESCRIPTIONS

Symbol	Function
V_{CCQ}, V_{DD}, V_{DDI}	Supply Voltage
DQ_0 to DQ_{31}	Data I/O
V_{SS}, V_{SSQ}, V_{SSI}	Ground
—	Don't Bond
$\overline{WE}$(WEB)	Write Enable
$\overline{CAS}$(CASB)	Column Address Strobe
$\overline{RAS}$(RASB)	Row Address Strobe
$\overline{CS}$(CSB)	Chip Select
BA	Bank Select (Bank Address)
AP	Auto Precharge Enable
A_0 to A_{10}	Address Input — Row: A_0 to A_{10}; Column: A_0 to A_7
CKE	Clock Enable
CLK	Clock Input
DQM_0 to DQM_3	Data Input/Output Mask
DSE	Disable (apply V_{SS} except DISABLE mode)
BME	Burn In Mode Entry (apply V_{SS} except Burn In mode)

* : Left part or right part is defined by adding suffix 'L' or 'R' in the end of each PAD name.

■ BLOCK DIAGRAM

MB811L646449 BLOCK DIAGRAM (for 1 Part)



■ FUNCTIONAL TRUTH TABLE

1. Command Truth Table

Function	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	A_9, A_8	A_7 to A_0	Remarks
		n-1	n									
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	*1
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	*1
Burst Stop	BST	H	X	L	H	H	L	X	X	X	X	*2
Read	READ	H	X	L	H	L	H	V	L	X	V	*3
Read with Auto-precharge	READA	H	X	L	H	L	H	V	H	X	V	*3
Write	WRIT	H	X	L	H	L	L	V	L	X	V	*3
Write with Auto-precharge	WRITA	H	X	L	H	L	L	V	H	X	V	*3
Bank Active	ACTV	H	X	L	L	H	H	V	V	V	V	*4
Precharge Single Bank	PRE	H	X	L	L	H	L	V	L	X	X	
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X	X	
Mode Register Set	MRS	H	X	L	L	L	L	X	X	V	V	*5, *6

V = Valid, L = Logic Low, H = Logic High, X = either L or H,
n = state at current clock cycle, n –1 = state at 1 clock cycle before n.

*1 : NOP and DESL commands have the same effect on the part. The both command have the device hold the internal operation.

*2 : BST command is effective for all burst length (BL = 1, 2, 4, 8, full column (256)) .

*3 : READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to “■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram) .”

*4 : ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command).

*5 : Required after power up. Refer to “18. Power-Up Initialization” in “■ FUNCTIONAL DESCRIPTION.”

*6 : MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to “■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram) .”

Notes : • All commands assume no CSUS command on previous rising edge of clock.
• All commands are assumed to be valid state transitions.
• All inputs are latched on the rising edge of clock.

2. DQM Truth Table

Function	Command	CKE		DQMi *1,*2
		n-1	n	
Data Input/Output Enable	ENBi *1	H	X	L
Data Input/Output Disable	MASKi *1	H	X	H

V = Valid, L = Logic Low, H = Logic High, X = either L or H,
n = state at current clock cycle, n –1 = state at 1 clock cycle before n.

*1 : i = 0, 1, 2, 3

*2 : DQM_0 for DQ_0 to DQ_7, DQM_1 for DQ_8 to DQ_{15}, DQM_2 for DQ_{16} to DQ_{23}, DQM_3 for DQ_{24} to DQ_{31}

Notes : • All commands assume no CSUS command on previous rising edge of clock.
• All commands are assumed to be valid state transitions.
• All inputs are latched on the rising edge of the clock.

3. CKE Truth Table

Current State	Function	Com-mand	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	A_9 to A_0	Re-marks
			n-1	n								
Bank Active	Clock Suspend Mode Entry	CSUS	H	L	X	X	X	X	X	X	X	*1
Any	Clock Suspend Continue	—	L	L	X	X	X	X	X	X	X	*1
Clock Suspend	Clock Suspend Mode Exit	—	L	H	X	X	X	X	X	X	X	
Idle	Auto-refresh Command	REF	H	H	L	L	L	H	X	X	X	*2
Idle	Self-refresh Entry	SELF	H	L	L	L	L	H	X	X	X	*2, *3
Self Refresh	Self-refresh Exit	SELFX	L	H	L	H	H	H	X	X	X	*4
			L	H	H	X	X	X	X	X	X	
Idle	Power Down Entry	PD	H	L	L	H	H	H	X	X	X	*3
			H	L	H	X	X	X	X	X	X	
Power Down	Power Down Exit	—	L	H	L	H	H	H	X	X	X	
			L	H	H	X	X	X	X	X	X	

V = Valid, L = Logic Low, H = Logic High, X = either L or H,
n = state at current clock cycle, n –1 = state at 1 clock cycle before n.

*1 : The CSUS command requires that at least one bank is active. Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram) ."
NOP or DSEL commands should only be issued after CSUS and PRE(or PALL) commands asserted at the same time.

*2 : REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)."

*3 : SELF and PD commands should only be issued after the last read data have been appeared on DQ.

*4 : CKE should be held high within one t_{RC} period after t_{CKSP}.

Notes : • All comands assume no CSUS command on previous rising edge of clock.
• All commands are assumed to be valid state transitions.
• All inputs are latched on the rising edge of the clock.

4. Operation Command Table (Applicable to single bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Remarks
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*1
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}	
	L	L	H	L	BA, AP	PRE/PALL	NOP	
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*2, *5
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC})	*2, *6
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA, CA, AP	READ/READA	Start Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Start Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Start Precharge; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Re-marks
Read	H	X	X	X	X	DESL	Continue Burst to End → Bank Active	
	L	H	H	H	X	NOP	Continue Burst to End → Bank Active	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP	*3
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Start Precharge →Idle; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write	H	X	X	X	X	DESL	Continue Burst to End → Write Recovery	
	L	H	H	H	X	NOP	Continue Burst to End → Write Recovery	
	L	H	H	L	X	BST	Burst Stop → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*3
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Start Precharge; Determine Precharge Type	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Re-marks
Read with Auto-precharge	H	X	X	X	X	DESL	Continue Burst to End → Precharge → Idle	
	L	H	H	H	X	NOP	Continue Burst to End → Precharge → Idle	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*1
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write with Auto-precharge	H	X	X	X	X	DESL	Continue Burst to End → Precharge → Idle	
	L	H	H	H	X	NOP	Continue Burst to End → Precharge → Idle	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*1
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Re-marks
Pre-charging	H	X	X	X	X	DESL	Idle after t_{RP}	
	L	H	H	H	X	NOP	Idle after t_{RP}	
	L	H	H	L	X	BST	Idle after t_{RP}	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*1
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	PALL may affect other bank	*4
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	Bank Active after t_{RCD}	
	L	H	H	H	X	NOP	Bank Active after t_{RCD}	
	L	H	H	L	X	BST	Bank Active after t_{RCD}	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*1
	L	L	H	H	BA, RA	ACTV	Illegal	*1
	L	L	H	L	BA, AP	PRE/PALL	Illegal	*1
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

(Continued)

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Command	Function	Re-marks
Refreshing	H	X	X	X	X	DESL	Idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Idle after t_{RC}	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	
Mode Register Setting	H	X	X	X	X	DESL	Idle after t_{RSC}	
	L	H	H	H	X	NOP	Idle after t_{RSC}	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

ABBREVIATIONS:

V = Valid, L = Logic Low, H = Logic High, X = either L or H
RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

*1 : Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.

*2 : Illegal if any bank is not idle.

*3 : Must satisfy bus contention, bus turn around, and/or write recovery requirements.
Refer to “11. READ Interrupted by WRITE (Example @ CL = 2, BL ≥ 4)” and “12. WRITE to READ Timing (Example @ CL = 2, BL = 4)” in “■ TIMING DIAGRAMS.”

*4 : NOP to bank precharging or in idle state. May precharge bank specified by BA (and AP).

*5 : SELF command should only be issued after the last read data have been appeared on DQ.

*6 : MRS command should only be issued on condition that all DQ are in High-Z.

Notes :
- All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle. Illegal means don’t used command. If used, power up sequence be asserted after power shout down.
- All commands assume no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.
- Illegal means that the device operation and/or data-integrity are not guaranteed. It used, power up sequence will be asserted after power shut down.
- All entries in “4. Operation Command Table” assume that the CKE was High during the proceeding clock cycle and the current clock cycle.

5. Command Truth Table for CKE

Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Re-marks
	n-1	n							
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{RC})	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{RC})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	Maintain Self-refresh	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	H	X	Idle after t_{RC}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	H	X	X	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	*1
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle	
	L	H	L	H	H	H	X		
	L	L	X	X	X	X	X	Maintain Power Down Mode	
	L	H	L	L	X	X	X	Illegal	
	L	H	L	H	L	X	X	Illegal	

(Continued)

Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	Function	Re-marks
	n-1	n							
All Banks Idle	H	H	H	X	X	X	MODE	Refer to “Operation Command Table”.	
	H	H	L	H	X	X	MODE	Refer to “Operation Command Table”.	
	H	H	L	L	H	X	MODE	Refer to “Operation Command Table”.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	MODE	Refer to “Operation Command Table”.	
	H	L	H	X	X	X	X	Power Down	
	H	L	L	H	H	H	X	Power Down	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh	*2
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active Bank Activating Read/Write	H	H	X	X	X	X	X	Refer to “Operation Command Table”.	
	H	L	X	X	X	X	X	Start Clock Suspend next cycle	
	L	X	X	X	X	X	X	Invalid	
Clock Suspend	H	X	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	Maintain Clock Suspend	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to “Operation Command Table”.	
	H	L	X	X	X	X	X	Illegal	

V = Valid, L = Logic Low, H = Logic High, X = either L or H,
n = state at current clock cycle, n –1 = state at 1 clock cycle before n.

*1 : CKE should be held High for t_{RC} period after t_{CKSP}.

*2 : SELF command should only be issued after the last data has been appeared on DQ.

Notes : • All entries in “5. Command Truth Table for CKE” are specified at CKE(n) state and CKE input from CKE(n–1) to CKE(n) state must satisfy corresponding set up and hold time for CKE.
- All commands assume no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.

■ FUNCTIONAL DESCRIPTION

1. SDR I/F FCRAM Basic Function

Three major differences between this SDR I/F FCRAMs and conventional DRAMs are: synchronized operation, burst mode, and mode register.

The **synchronized operation** is the fundamental difference. SDR I/F FCRAM uses a clock input for the synchronization, while the DRAM is basically asynchronous memory although it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase differences while each operation of SDR I/F FCRAM is determined by commands and all operations are referenced to a positive clock edge. “BASIC TIMING FOR CONVENTIONAL DRAM VS SDR I/F FCRAM” shows the basic timing diagram differences between SDR I/F FCRAMs and DRAMs.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode registe**r is to justify the SDR I/F FCRAM operation and function into desired system conditions. “■ MODE REGISTER TABLE” shows how SDR I/F FCRAM can be configured for system requirement by mode register programming.

The program to the mode register should be excuted after all banks are precharged.

2. FCRAM™

MB811L646449 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

3. Clock Input (CLK) and Clock Enable (CKE)

All input and output signals of SDR I/F FCRAM use register type buffers. CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by a rising edge of CLK. CKE is a high active clock enable signal. CKE controls the internal clock generator. CKE is latched by a rising edge of CLK. CKE should become High level on the previous clock cycle when a basic command is issued. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

4. Chip Select ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address input. When $\overline{CS}$ is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn’t needed, $\overline{CS}$ can be tied to ground level.

5. Command Input ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply SDR I/F FCRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDR I/F FCRAM operation. Refer to “■ FUNCTIONAL TRUTH TABLE.”

6. Address Input (A_0 to A_{10})

Address input selects an arbitrary location of a total of 524,288 words of each memory cell matrix in one part. A total of nineteen address input signals are required to decode such a matrix. SDR I/F FCRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), eleven Row addresses are initially latched and the remainder of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

7. Bank Select (BA)

This SDR I/F FCRAM has two banks in one part and each bank is organized as 512 K words by 32-bit. Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).

8. Data Input and Output (DQ_0 to DQ_{31})

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input:

t_{RAC} ; from the bank active command when t_{RCD} (Min) is satisfied. (This parameter is reference only.)
t_{CAC} ; from the read command when t_{RCD} is greater than t_{RCD} (Min). (This parameter is reference only.)
t_{AC} ; from the previous clock edge when output data is valid.

The polarity of the output data is identical to that of the input data. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}).

Refer to "■ AC CHARACTERISTICS."

9. Data I/O Mask (DQM_0 to DQM_3)

DQM_0 to DQM_3 is an active high enable input and has an output disable and input mask function. During burst cycle and when DQM_0 to DQM_3 = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type. DQM_0, DQM_1, DQM_2 and DQM_3 control DQ_0 to DQ_7, DQ_8 to DQ_{15}, DQ_{16} to DQ_{23} and DQ_{24} to DQ_{31}, respectively.

10. Burst Mode Operation and Burst Type

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary or full column. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after l_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps around to least significant address (= 0). The interleave mode is a scrambled decoding scheme for A_0 and A_2. If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

Burst Length	Starting Column Address			Sequential Mode	Interleave Mode
	A_2	A_1	A_0		
2	X	X	0	0 – 1	0 – 1
	X	X	1	1 – 0	1 – 0
4	X	0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X	0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X	1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X	1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

11. Full Column Burst and Burst Stop Command (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps around to first column address (= 0) and continues to count until interrupted by the news read (READ) /write (WRIT), precharge (PRE), or burst stop (BST) commands. The selection of Auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.
For the detail rule, please refer to “8. READ Interrupted by Burst Stop (Example @ CL = 2, BL = Full Column) ” in “■ TIMING DIAGRAMS.”
When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

12. Burst Read & Single Write

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

13. Precharge and Precharge Option (PRE, PALL)

SDR I/F FCRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE). With the Precharge command, SDR I/F FCRAM will automatically be in standby state after precharge time (t_{RP}).

The precharged bank is selected by combination of AP and BA when Precharge command is asserted. If AP = High, all banks are precharged regardless of BA (PALL). If AP = Low, a bank to be selected by BA is precharged (PRE).
The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion.
This auto precharge is entered by AP = High when a read or write command is asserted. Refer to "■ FUNCTIONAL TRUTH TABLE."

14. Auto-Refresh (REF)

Auto-refresh uses the internal refresh address counter. The SDR I/F FCRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDR I/F FCRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 15.6 μs or a total 2048 refresh commands within 32 ms period.

15. Self-Refresh Entry (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SDR I/F FCRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note : When the burst refresh method is used, a total of 2048 auto-refresh commands must be asserted within 2 ms prior to the self-refresh mode entry.

16. Self-Refresh Exit (SELFX)

To exit self-refresh mode, apply minimum t_{CKSP} after CKE brought high, and then the No Operation command (NOP) or the Deselect command (DESL) should be asserted within one t_{RC} period. CKE should be held High within one t_{RC} period after t_{CKSP}. Refer to "16. Self-Refresh Entry and Exit Timing" in section "■ TIMING DIAGRAMS" for the detail.

It is recommended to assert an Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

Note : When the burst refresh method is used, a total of 2048 auto-refresh commands must be asserted within 2 ms after the self-refresh exit.

17. Mode Register Set (MRS)

The mode register of SDR I/F FCRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS latency, and Operation Code. Refer to "■ MODE REGISTER TABLE."

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all DQ is in High-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDR I/F FCRAM. Refer to "18. Power-Up Initialization".

18. Power-up Initialization

SDR I/F FCRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply power (V_{DD} and V_{DDI} should be applied before or in parallel with V_{CCQ})and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 100 μs.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 2 Auto-refresh command (REF).
5. Program the mode register by Mode Register Set command (MRS).

In addition, it is recommended DQM and CKE to track V_{DD} to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 2 Auto-refresh command (REF). It is possible to excute 5 after 4.

19. Disable

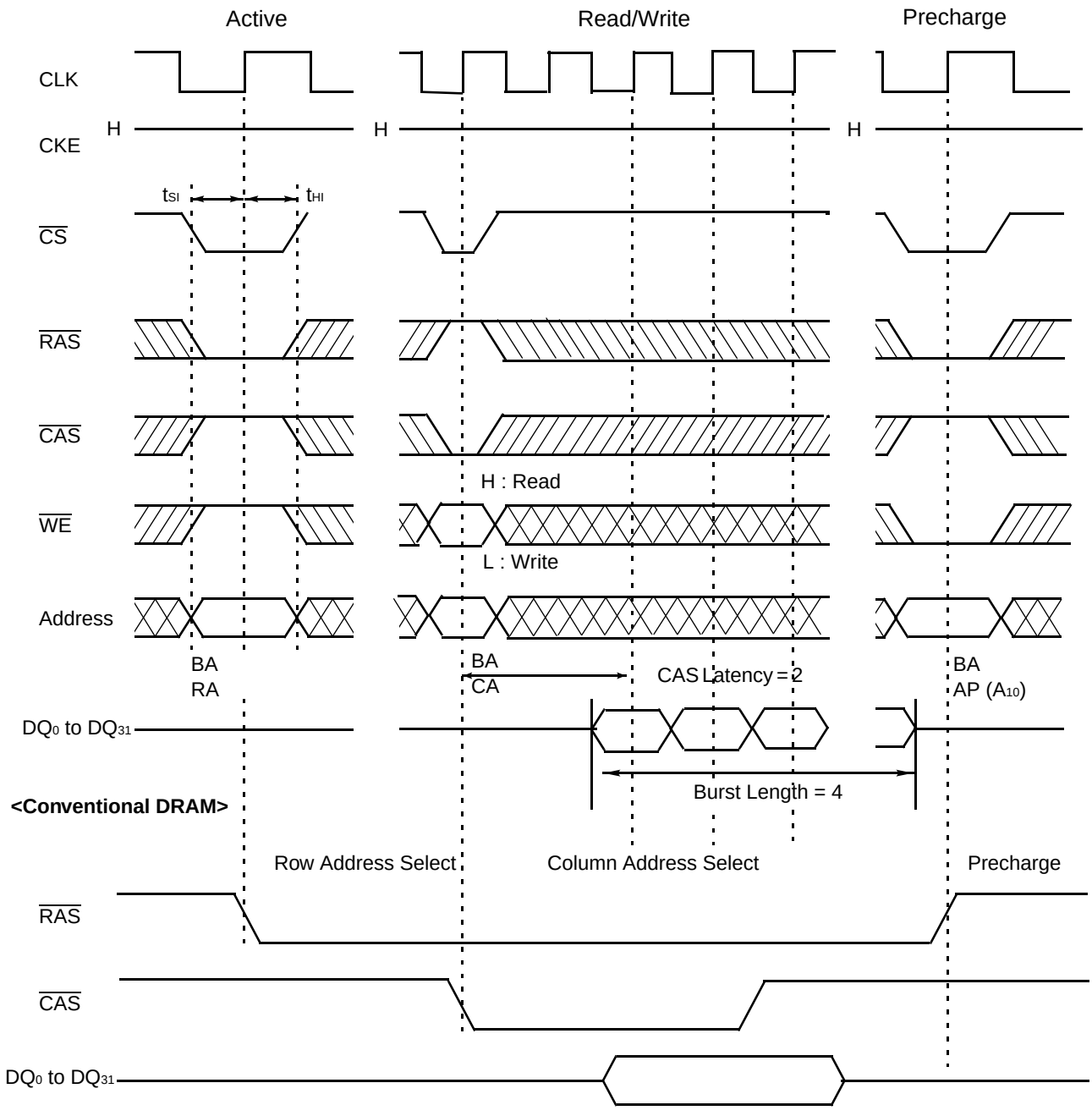
When DSE PAD is applied high level, SDR I/F FCRAM entries DISABLE mode. This command entry doesn't require clock. In DISABLE mode,SDR I/F FCRAM current cousumption is less than I_{CC2PS} and output is High-Z. Any command isn't accepted in this mode. To exit DISABLE mode, apply Low level to DSE PAD.

20. BURN IN

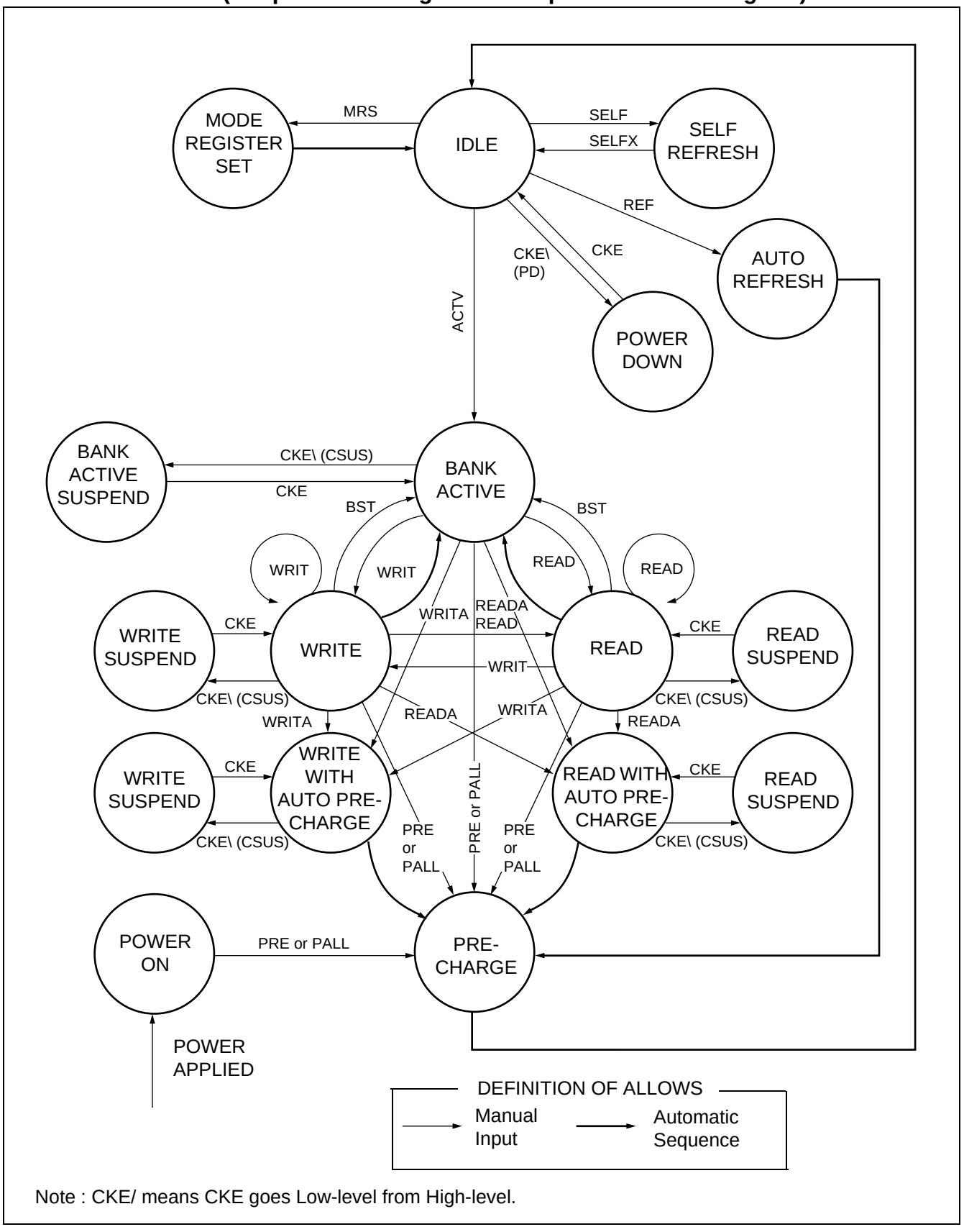
When BME PAD is applied High level,SDR I/F FCRAM entries BURN IN mode. This command doesn't require clock. In BURN IN mode, self refresh function is asserted internaly. Any command isn't accepted in this mode. To exit BURN IN mode,apply Low level to BME PAD.

BASIC TIMING FOR CONVENTIONAL DRAM VS SDR I/F FCRAM

<SDR I/F FCRAM>



■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)



Note : CKE/ means CKE goes Low-level from High-level.

■ BANK OPERATION COMMAND TABLE

- **Minimum Clock Latency or Delay Time for 1 Bank Operation**

Second command (same bank) / First command	MRS	ACTV	READ	READA*4	WRIT	WRITA*4	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV			t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}			1
READ			1	1	*5 1	*5 1	*4 1	*4 1			1
READA	*1,*2 BL + t_{RP}	BL + t_{RP}					*4 BL + t_{RP}	*4 BL + t_{RP}	*2 BL + t_{RP}	*2,*7 BL + t_{RP}	
WRIT			t_{WR}	t_{WR}	1	1	*4 t_{DPL}	*4 t_{DPL}			1
WRITA	*2 BL-1 + t_{DAL}	BL-1 + t_{DAL}					*4 BL-1 + t_{DAL}	*4 BL-1 + t_{DAL}	*2 BL-1 + t_{DAL}	*2 BL-1 + t_{DAL}	
PRE	*2,*3 t_{RP}	t_{RP}					1	*4 1	*2 t_{RP}	*2,*6 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}					1	1	t_{RP}	*6 t_{RP}	1
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

*1 : If t_{RP}(Min) ≤ CL×t_{CK}, minimum latency is a sum of (BL+CL)×t_{CK}.
*2 : Assume all banks are in Idle state.
*3 : Assume output is in High-Z state.
*4 : Assume t_{RAS}(Min) is satisfied.
*5 : Assume no I/O conflict.
*6 : Assume after the last data have been appeared on DQ.
*7 : If t_{RP}(Min) ≤ (CL-1)×t_{CK}, minimum latency is a sum of (BL+CL-1)×t_{CK}.

Illegal Command

- **Minimum Clock Latency or Delay Time for Multibank Operation**

First command \ Second command (other bank)	MRS	ACTV	READ*5	READA*5,*6	WRIT*5	WRITA*5,*6	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV		*2 t_{RRD}	*7 1	*7 1	*7 1	*7 1	*6,*7 1	*7 t_{RAS}			1
READ		*2,*4 1	1	1	*10 1	*10 1	*6 1	*6 1			1
READA	*1,*2 BL+ t_{RP}	*2,*4 1	*6 1	*6 1	*6,*10 1	*6,*10 1	*6 1	*6 BL+ t_{RP}	*2 BL+ t_{RP}	*2,*9 BL+ t_{RP}	
WRIT		*2,*4 1	1	1	1	1	*6 1	*6 t_{DPL}			1
WRITA	*2 BL-1 + t_{DAL}	*2,*4 1	*6 1	*6 1	*6 1	*6 1	*6 1	*6 BL-1 + t_{DAL}	*2 BL-1 + t_{DAL}	*2 BL-1 + t_{DAL}	
PRE	*2,*3 t_{RP}	*2,*4 1	*7 1	*7 1	*7 1	*7 1	*6,*7 1	*7 1	*2 t_{RP}	*2,*8 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}					1	1	t_{RP}	*8 t_{RP}	1
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

*1 : If t_{RP}(Min) ≤ CL×t_{CK}, minimum latency is a sum of (BL+CL)×t_{CK}.
*2 : Assume bank of the object is in Idle state.
*3 : Assume output is in High-Z state.
*4 : t_{RRD}(Min) of other bank (the second command will be asserted) is satisfied.
*5 : Assume other bank is in active, read or write state.
*6 : Assume t_{RAS}(Min) is satisfied.
*7 : Assume other banks are not in READA/WRITA state.
*8 : Assume after the last data have been appeared on DQ.
*9 : If t_{RP}(Min) ≤ (CL-1)×t_{CK}, minimum latency is a sum of (BL+CL-1)×t_{CK}.
*10 : Assume no I/O conflict.

Illegal Command

■ MODE REGISTER TABLE

MODE REGISTER SET

BA	A_{10}	A_9	A_{8} *3	A_{7} *3	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0 or 1		Op-code	0	0	CL			BT	BL			MODE REGISTER

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT = 0	BT = 1 *2
0	0	0	1	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_9	Op-code
0	Burst Read & Burst Write
1	Burst Read & Single Write*1

A_3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round, Binary-up)

*1 : When A_9 = 1, burst length at Write is always one regardless of BL value.

*2 : BL = 1 and Full Column are not applicable to the interleave mode.

*3 : A_7 = 1 and A_8 = 1 are reserved for vender test.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{CCQ} Supply Relative to V_{SS}	V_{CCQ}	–0.5	+4.6	V
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}, V_{DDI}	–0.5	+3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	+4.6	V
Short Circuit Output Current	I_{OUT}	–50	+50	mA
Power Dissipation	P_D	1.0		W
Storage Temperature	T_{STG}	–55	+125	°C

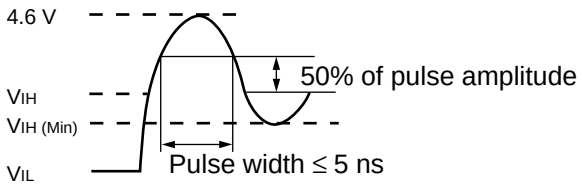
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

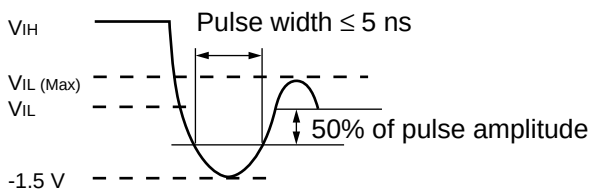
(Referenced to V_{SS})

Parameter	Symbol		Value			Unit	Remarks
			Min	Typ	Max		
Supply Voltage	V_{CCQ}	3.3 V I/O	3.0	3.3	3.6	V	
		2.5 V I/O	2.3	2.5	2.7	V	
	V_{DD}, V_{DDI}		2.3	2.5	2.7	V	
	V_{SS}, V_{SSQ}, V_{SSI}		0	0	0	V	
Input High Voltage	V_{IH}	3.3 V I/O	2.4	—	V_{CCQ} + 0.5	V	*1
		2.5 V I/O	2.0	—	V_{CCQ} + 0.5	V	
Input Low Voltage	V_{IL}		–0.5	—	0.4	V	*2
Ambient Temperature	T_A		0	—	70	°C	

*1. Overshoot limit: V_{IH} (Max)
= 4.6 V for pulse width ≤ 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.



*2. Undershoot limit: V_{IL} (Min)
= V_{SS} –1.5 V for pulse width ≤ 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

(T_A = +25°C, f = 1 MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance, Except for CLK	C_{IN1}	1.5	—	5.0	pF
Input Capacitance for CLK	C_{IN2}	1.5	—	4.0	pF
I/O Capacitance (DQ_0 to DQ_{31})	$C_{I/O}$	2.0	—	6.0	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol		Condition	Value		Unit
					Min	Max	
Output High Voltage		$V_{OH(DC)}$	3.3 V I/O	I_{OH} = –2 mA	2.4	—	V
			2.5 V I/O	I_{OH} = –0.5 mA	2.0	—	V
Output Low Voltage		$V_{OL(DC)}$	3.3 V I/O	I_{OL} = 2 mA	—	0.4	V
			2.5 V I/O	I_{OL} = 0.5 mA	—	0.4	V
Input Leakage Current (Any Input except for DSEL,DSER,BMEL,BMER)		I_{LI}		0 V ≤ V_{IN} ≤ V_{CCQ}; All other pins not under test = 0 V	–5	+5	µA
Input Leakage Current (DSEL,DSER,BMEL,BMER)		I_{LIPD}		V_{IN} = 0 V All oher pins not under test = 0V	–5	+5	µA
Input Pull Down Resistance (DSEL,DSER,BMEL,BMER)		R_{PD}		—	5	20	kΩ
Output Leakage Current		I_{LO}		0 V ≤ V_{IN} ≤ V_{CCQ}; Data out disabled	–5	+5	µA
Operating Current (Average Power Supply Current)	MB811L646449-12	I_{CC1}		Burst Length = 1, t_{CK} = Min, t_{RC} = Min, One bank active, Output pin open, Adrresses changed up to 1 - time during t_{RC} (Min), 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	240	mA
	MB811L646449-18					160	
Power Supply Current (Precharge Standby Current)		I_{CC2P}		CKE = V_{IL}, All banks idle, t_{CK} = Min, Power down mode, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	4	mA
		I_{CC2PS}		CKE = V_{IL} , All banks idle, CLK = V_{IH} or V_{IL}, Power down mode, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	2	mA
	MB811L646449-12	I_{CC2N}		CKE = V_{IH} , All banks idle, t_{CK} = Min, NOP commands only, Input signals (except to CMD) are changed 1 time during 2 clocks, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	24	mA
	MB811L646449-18					16	
		I_{CC2NS}		CKE = V_{IH} , All banks idle CLK = V_{IH} or V_{IL}, Input signal are stable, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	4	mA

(Continued)

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min	Max	
Power Supply Current (Active Standby Current)		I_{CC3P}	CKE = V_{IL}, Any bank active, t_{CK} = Min, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	4	mA
		I_{CC3PS}	CKE = V_{IL}, Any bank active, CLK = V_{IH} or V_{IL}, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	2	mA
	MB811L646449-12	I_{CC3N}	CKE = V_{IH}, Any bank active, t_{CK} = Min, NOP commands only, Input signals (except to CMD) are changed 1 time during 2 clocks, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	75	mA
	MB811L646449-18				50	
		I_{CC3NS}	CKE = V_{IH}, Any bank active, CLK = V_{IH} or V_{IL}, Input signals are stable, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	4	mA
Average Power Supply Current (Burst mode Current)	MB811L646449-12	I_{CC4}	t_{CK} = Min, Burst Length = 4, Output pin open, All-banks active, Gapless data, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	285	mA
	MB811L646449-18				190	
Average Power Supply Current (Refresh Current #1)	MB811L646449-12	I_{CC5}	Auto-refresh; t_{CK} = Min, t_{RC} = Min, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	300	mA
	MB811L646449-18				200	
Average Power Supply Current (Refresh Current #2)		I_{CC6}	Self-refresh; t_{CK} = Min, CKE ≤ 0.2 V, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{CCQ}	—	5	mA

Notes : • All voltages are referenced to V_{SS}.

- DC characteristics are measured after following the “18. Power-Up Initialization” procedure in “■ FUNCTIONAL DESCRIPTION.”
- I_{CC} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open and no termination register.

■ AC CHARACTERISTICS

(1) AC Characteristics

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB811L646449-12		MB811L646449-18		Unit	Re-maeks
		Min	Max	Min	Max		
Clock Period CL = 2	t_{CK2}	12	—	18	—	ns	
Clock High Time	t_{CH}	t_{CK} x 0.3	—	t_{CK} x 0.4	—	ns	*2
Clock Low Time	t_{CL}	t_{CK} x 0.3	—	t_{CK} x 0.4	—	ns	*2
Input Setup Time	t_{SI}	3	—	4	—	ns	*2
Input Hold Time	t_{HI}	1.5	—	1.5	—	ns	*2
Access Time from Clock(t_{CK} =Min) CL = 2	t_{AC2}	—	9	—	9	ns	*2,*3,*4
Output in Low-Z	t_{LZ}	0	—	0	—	ns	*2
Output in High-Z CL = 2	t_{HZ2}	2	9	2	9	ns	*2,*5
Output Hold Time CL = 2	t_{OH}	2	—	2	—	ns	*2,*4
Time between Auto-Refresh command interval	t_{REFI}	—	15.6	—	15.6	µs	*1
Time between Refresh	t_{REF}	—	32	—	32	ms	
Transition Time	t_T	0.5	10	0.5	10	ns	
CKE Setup Time for Power Down Exit Time	t_{CKSP}	3	—	4	—	ns	*2

Notes : • AC characteristics are measured after following the “18. Power-Up Initialization” procedure in “■ FUNCTIONAL DESCRIPTION.”
• AC characteristics assume t_T = 1 ns, 10 pF of capacitive load and 50 Ω of terminated load.
• 1.4 V is the reference level for 3.3 V I/O for measuring timing of input signals. 1.2 V is the reference level for 2.5 V I/O for measuring timing of input singnals. Transition times are measured between V_{IH} (Min) and V_{IL} (Max).

*1 : This value is for reference only.

*2 : If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) – 0.5] ns should be added to t_{AC} (Max), t_{HZ} (Max), and t_{CKSP} (Min) spec values, [(t_T/2) – 0.5] ns should be subtracted from t_{LZ} (Min), t_{HZ} (Min), and t_{OH} (Min) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min), t_{CL} (Min), t_{SI} (Min), and t_{HI} (Min) spec values.

*3 : t_{AC} also specifies the access time at burst mode.

*4 : t_{AC} and t_{OH} are measured under OUTPUT LOAD CIRCUIT shown in “OUTPUT LOAD CIRCUIT”.

*5 : Specified where output buffer is no longer driven.

(2) Base Values for Clock Count/Latency

Parameter	Symbol	MB811L646449-12		MB811L646449-18		Unit	Re-marks
		Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	t_{RC}	72	—	108	—	ns	*
$\overline{RAS}$ Precharge Time	t_{RP}	24	—	36	—	ns	
$\overline{RAS}$ Active Time	t_{RAS}	48	110000	72	110000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	24	—	36	—	ns	
Write Recovery Time	t_{WR}	18	—	18	—	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time	t_{RRD}	24	—	36	—	ns	
Data-in to Precharge Lead Time	t_{DPL}	12	—	18	—	ns	
Data-in to Active/Refresh Command Period CL=2	t_{DAL2}	1 cyc + t_{RP}	—	1 cyc + t_{RP}	—	ns	
Mode Resister Set Cycle Time	t_{RSC}	24	—	36	—	ns	

* : Actual clock count of t_{RC} (ℓ_{RC}) will be sum of clock count of t_{RAS} (ℓ_{RAS}) and t_{RP} (ℓ_{RP}).

(3) Clock Count Formula*

$$\text{Clock cycle} \geq \frac{\text{Base Value}}{\text{Clock Period}} \text{ (Round up a whole number)}$$

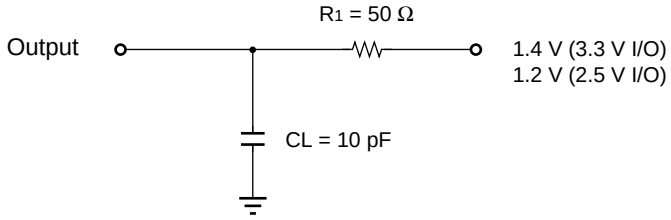
* : All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off to a whole number).

(4) Latency - Fixed Values

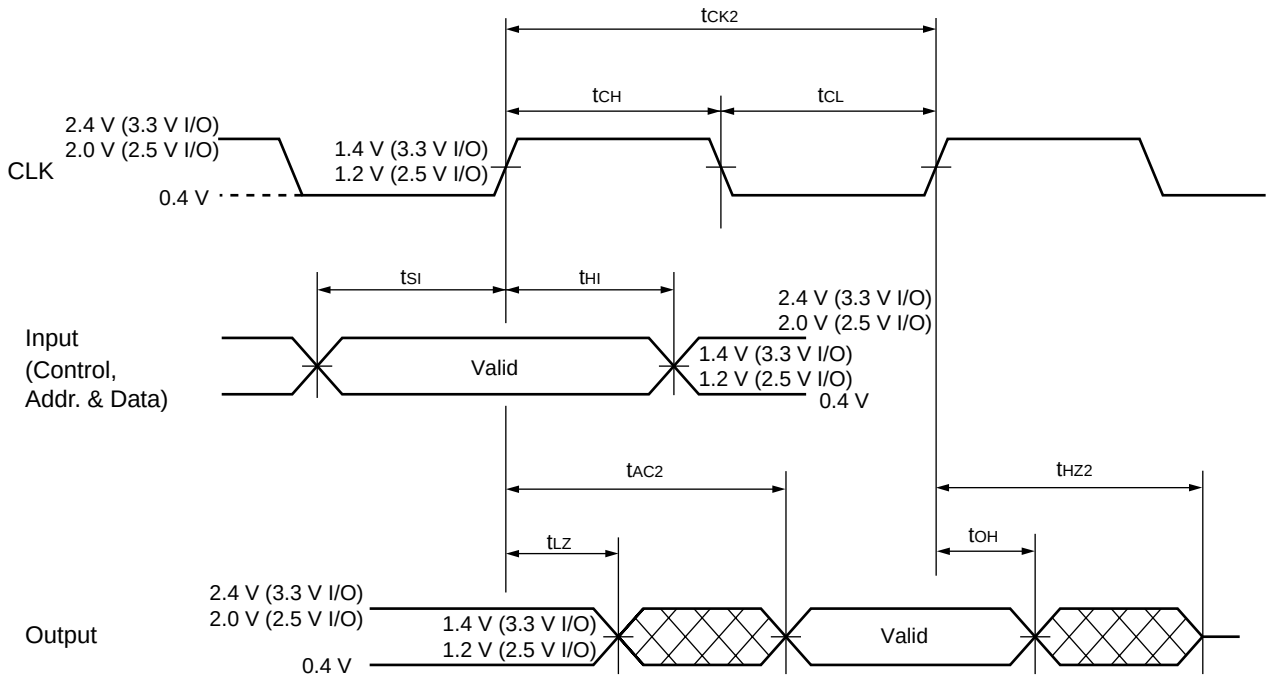
(The latency values on these parameters are fixed regardless of clock period.)

Parameter		Sym-bol	MB811L646449-12	MB811L646449-18	Unit
CKE to Clock Disable		ℓ_{CKE}	1	1	cycle
DQM to Output in High-Z		ℓ_{DQZ}	2	2	cycle
DQM to Input Data Delay		ℓ_{DQD}	0	0	cycle
Last Output to Write Command Delay		ℓ_{OWD}	2	2	cycle
Write Command to Input Data Delay		ℓ_{DWD}	0	0	cycle
Precharge to Output in High-Z Delay	CL = 2	ℓ_{ROH2}	2	2	cycle
Burst Stop Command to Output in High-Z Delay	CL = 2	ℓ_{BSH2}	2	2	cycle
$\overline{CAS}$ to $\overline{CAS}$ Delay (Min)		ℓ_{CCD}	1	1	cycle
$\overline{CAS}$ Bank Delay (Min)		ℓ_{CBD}	1	1	cycle

OUTPUT LOAD CIRCUIT

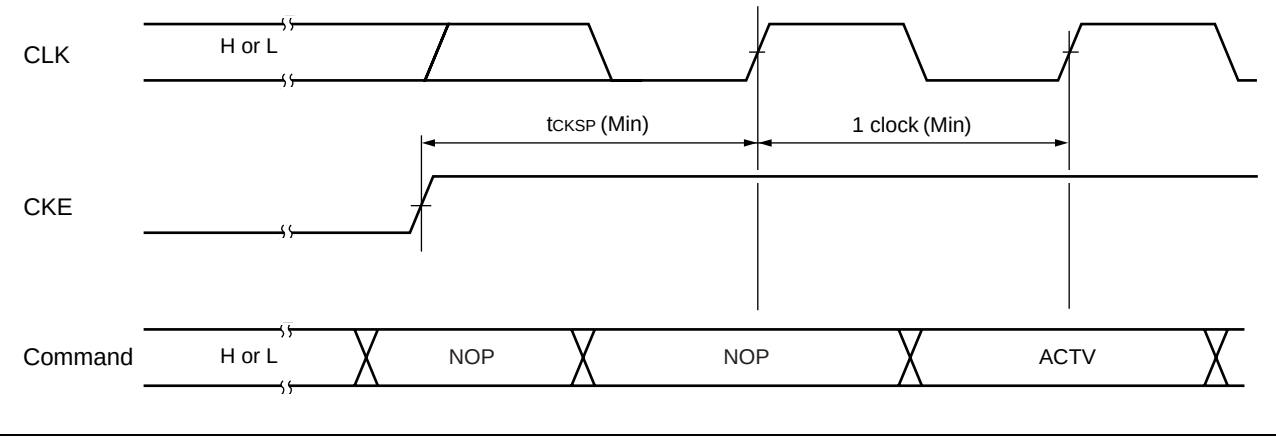


(5) Timing Diagram, Setup, Hold and Delay Time

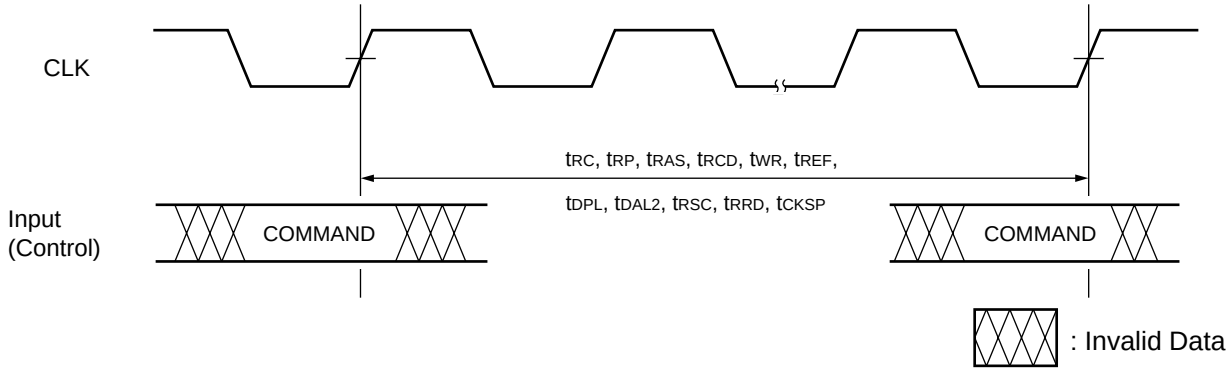


Notes : • Reference level of input signal is 1.4 V for LVCMOS (3.3 V I/O),1.2 V for LVCMOS (2.5 V I/O).
• Access time is measured at 1.4 V for LVCMOS (3.3 V I/O),1.2 V for LVCMOS (2.5 V I/O).
• AC characteristics are also measured in this condition.

(6) Timing Diagram, Delay Time for Power Down Exit

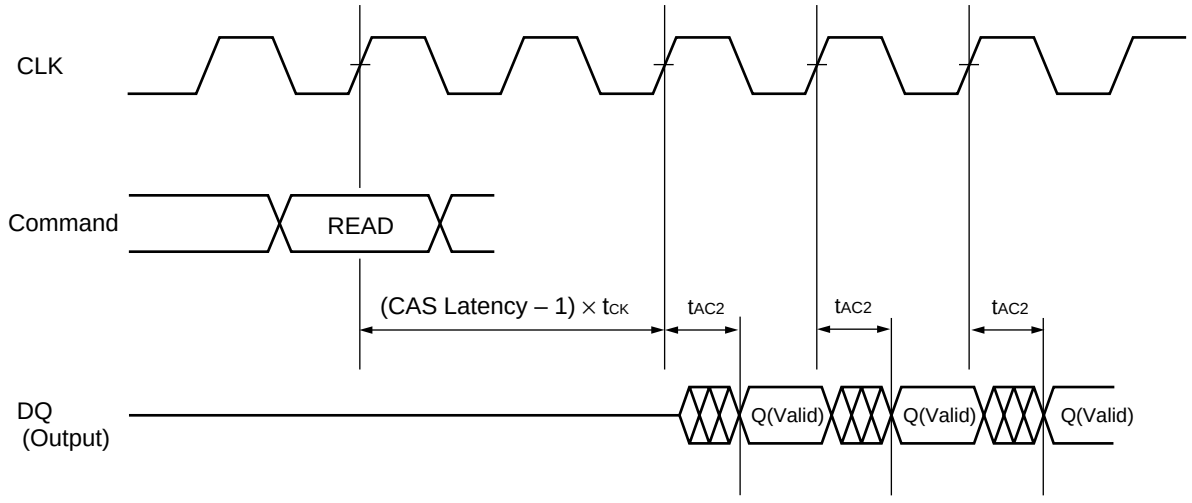


(7) Timing Diagram, Pulse Width



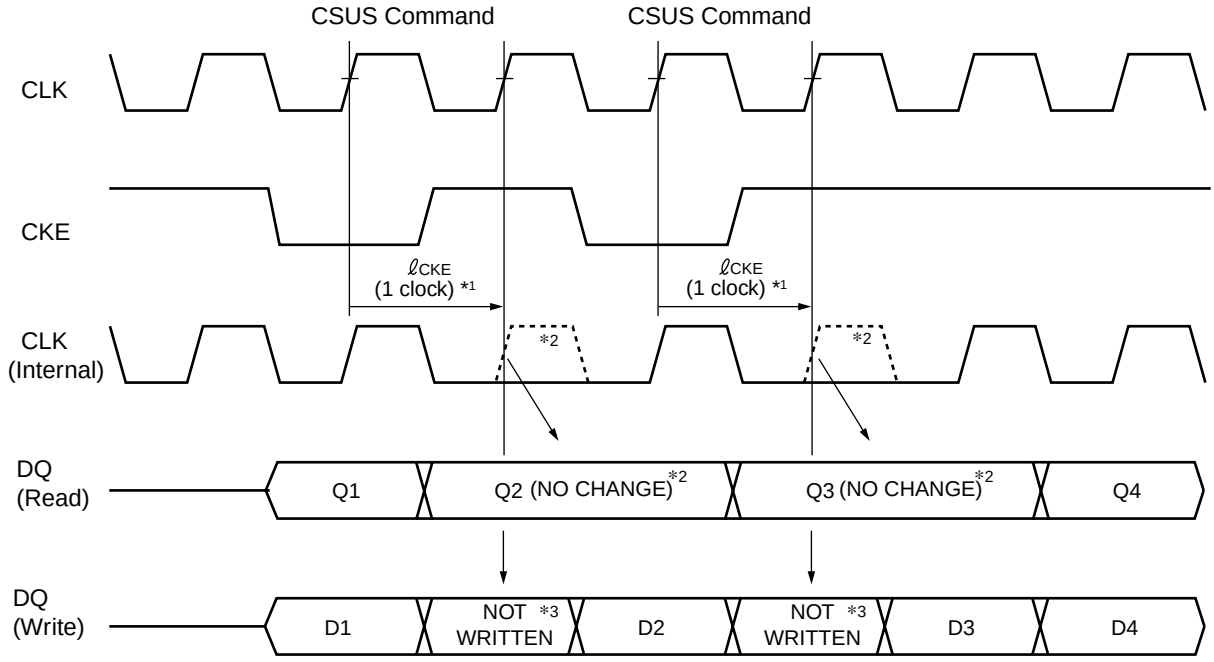
Notes : • These parameters are a limit value of the rising edge of the clock from one command input to the next input. t_{CKSP} is the latency value from the rising edge of CKE.
• Measurement reference voltage is 1.4 V (3.3 V I/O) or 1.2 V (2.5 V I/O).

(8) Timing Diagram, Access Time



■ TIMING DIAGRAMS

1. Clock Enable - Read and Write Suspend (@ BL = 4)

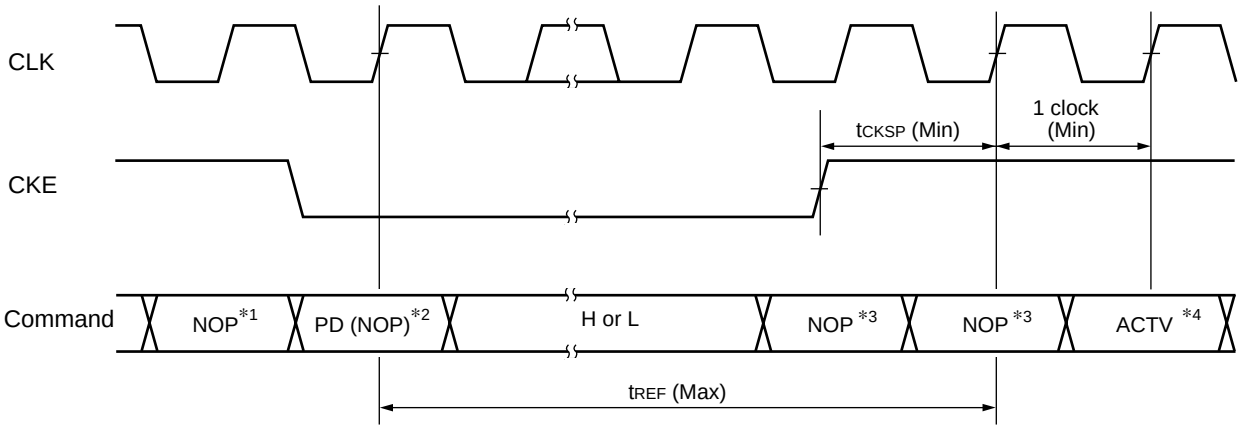


*1: The latency of CKE (ℓ_{CKE}) is one clock.

*2: During read mode, burst counter will not be increased and/or decreased at the next clock of CSUS command. Output data remain the same data.

*3: During the write mode, data at the next clock of CSUS command is ignored.

2. Clock Enable - Power Down Entry and Exit



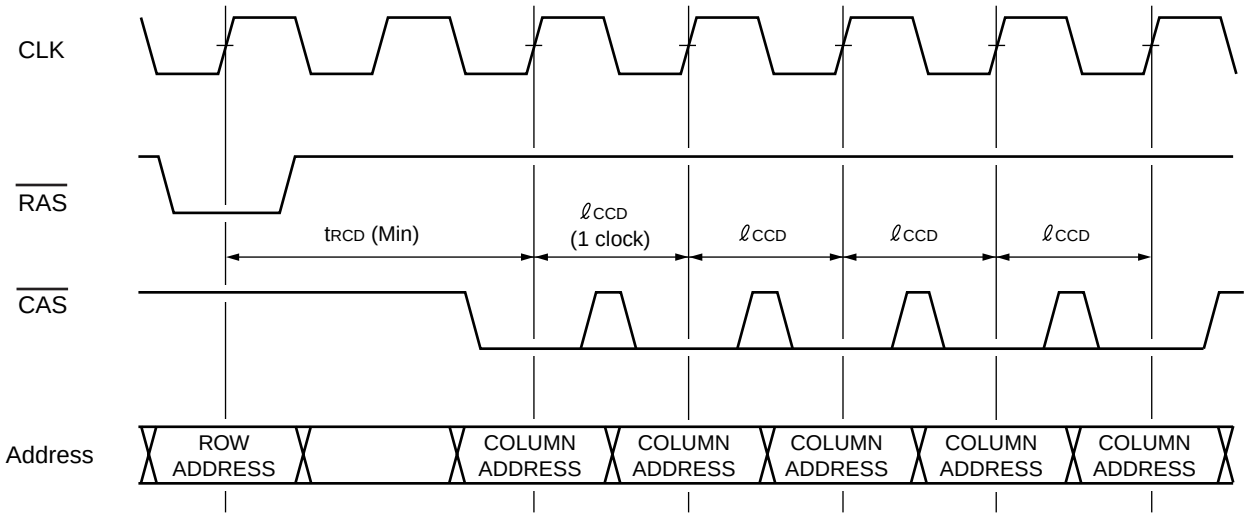
*1: Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.

*2: Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.

*3: It is recommended to apply NOP command in conjunction with CKE.

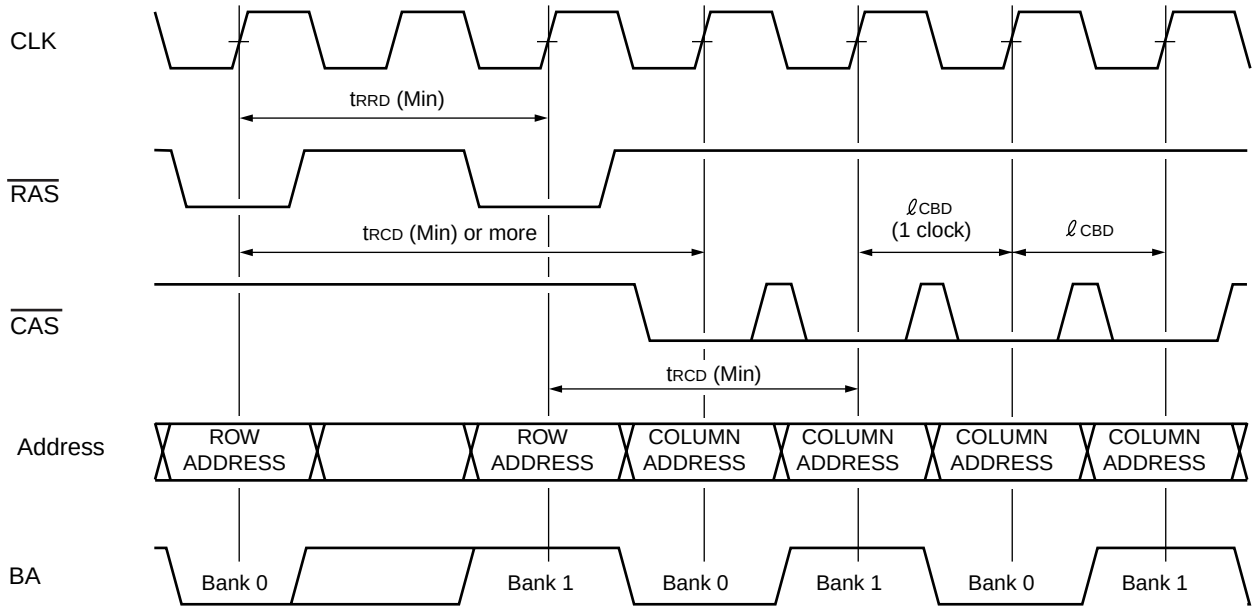
*4: The ACTV command can be latched after t_{CKSP} (Min) + 1 clock (Min).

3. Column Address to Column Address Input Delay



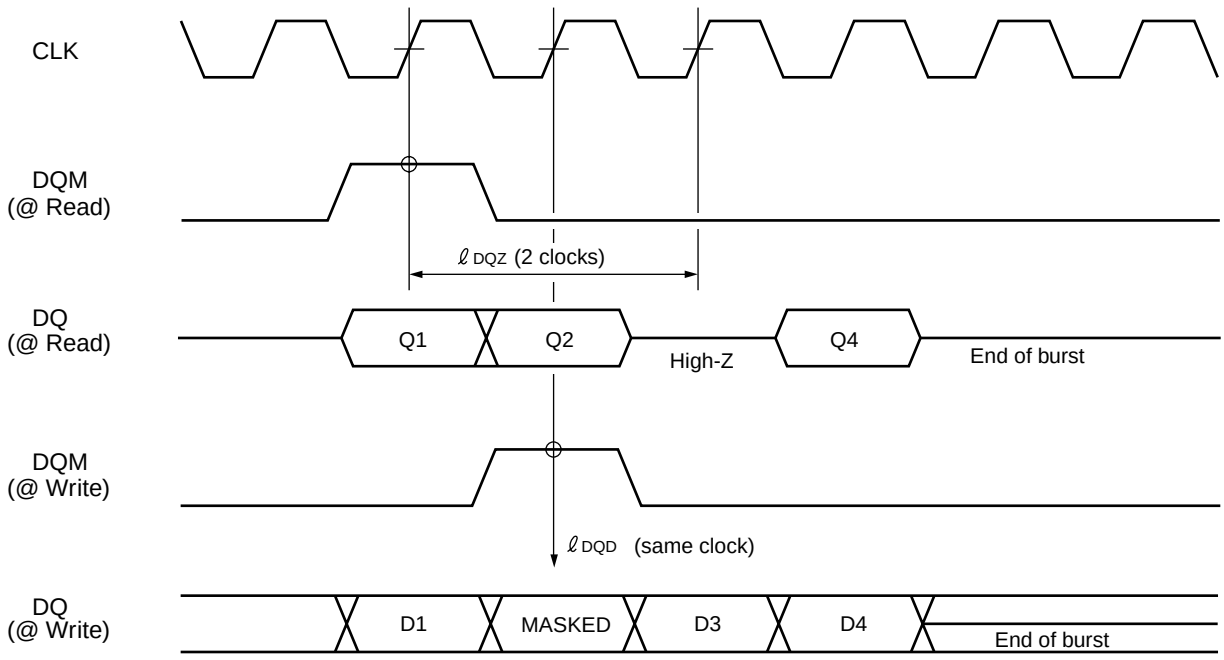
Note : $\overline{CAS}$ to $\overline{CAS}$ delay can be one or more clock period.

4. Different Bank Address Input Delay

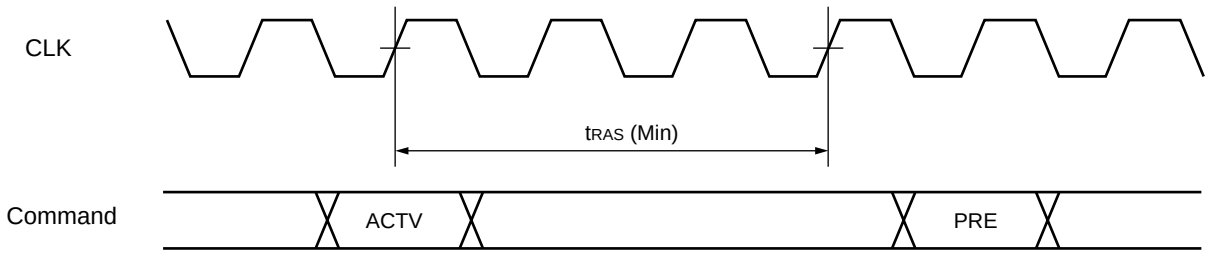


Note : $\overline{CAS}$ Bank delay can be one or more clock period.

5. DQM - Input Mask and Output Disable (@ BL = 4)

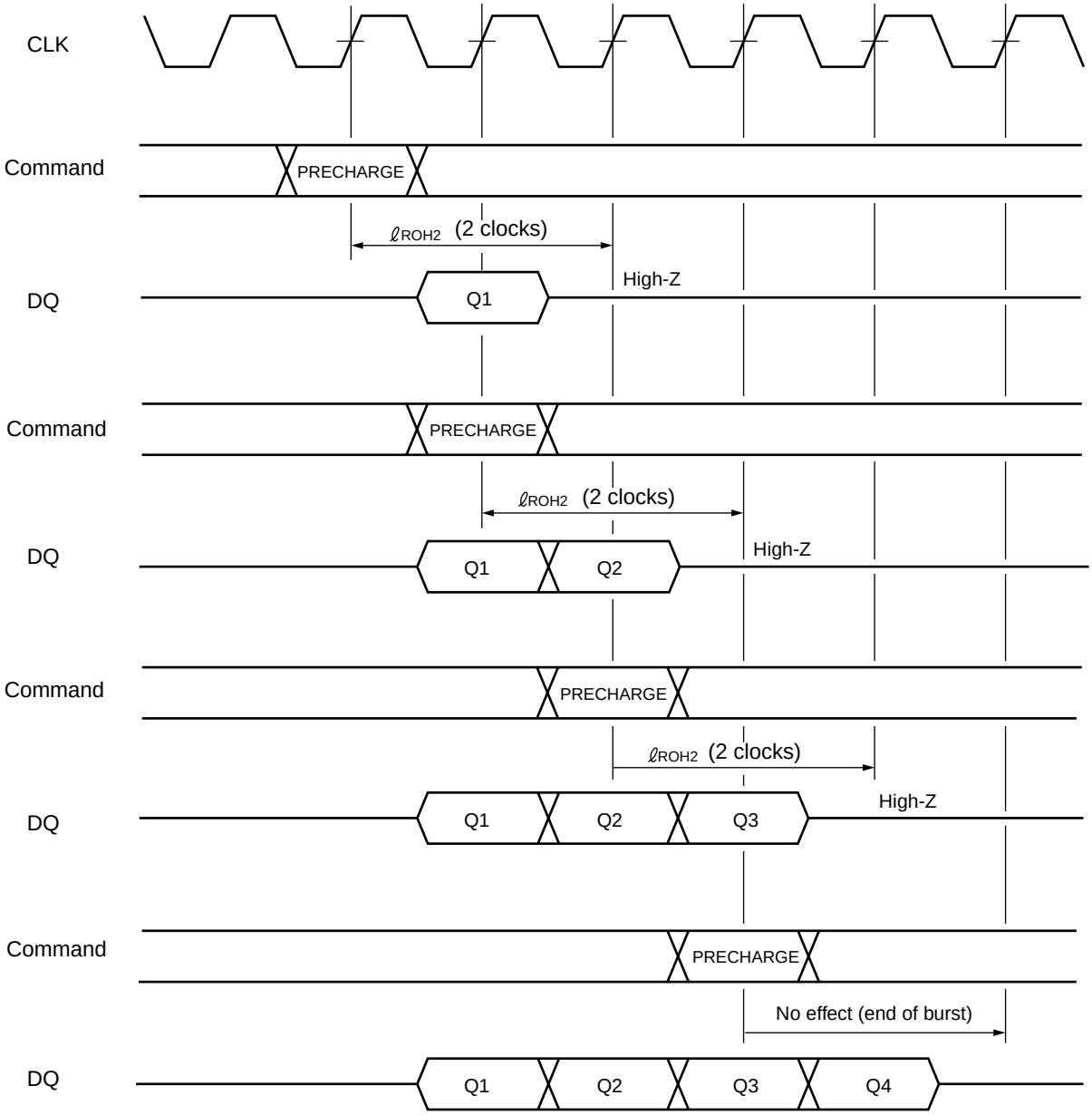


6. Precharge Timing (Applied to the Same Bank)



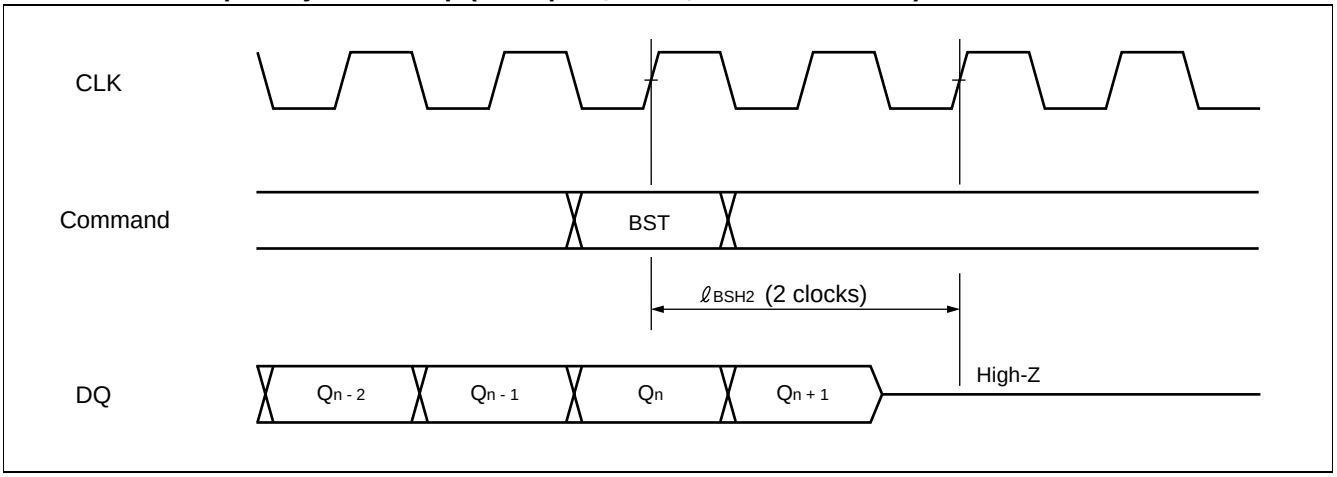
Note : PRECHARGE means ’PRE’ or ’PALL’.

7. READ Interrupted by Precharge (Example @ CL = 2, BL = 4)

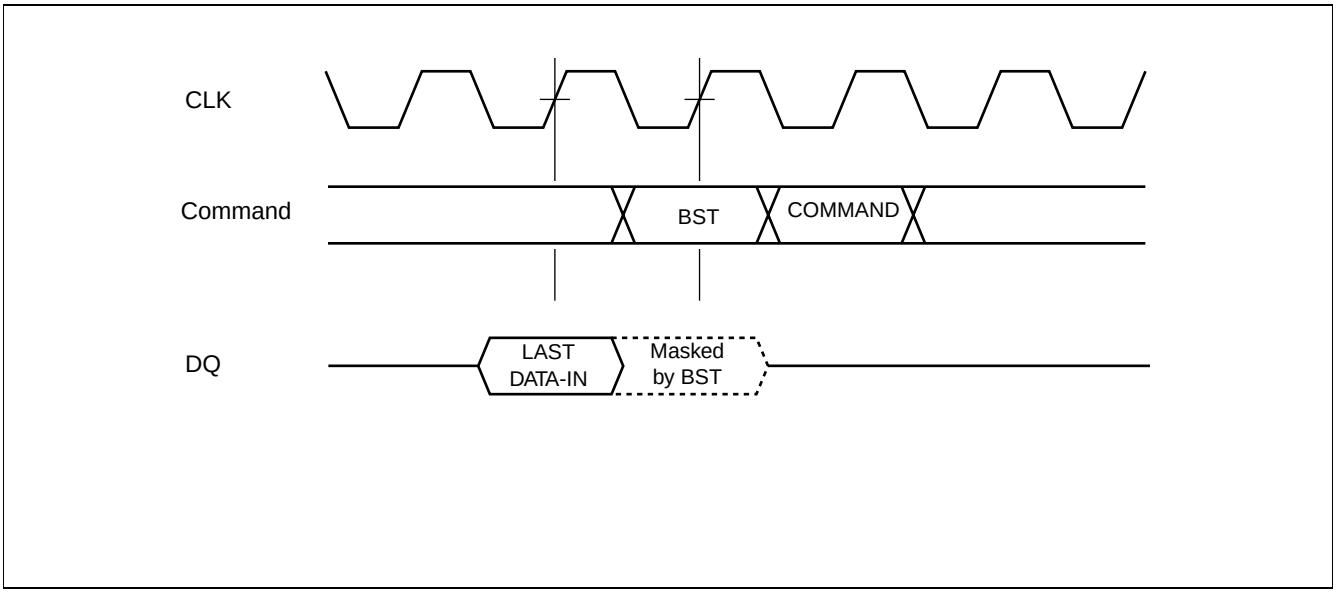


Note : In case of CL = 2, the ℓROH2 is 2 clocks.
PRECHARGE means 'PRE' or 'PALL'.

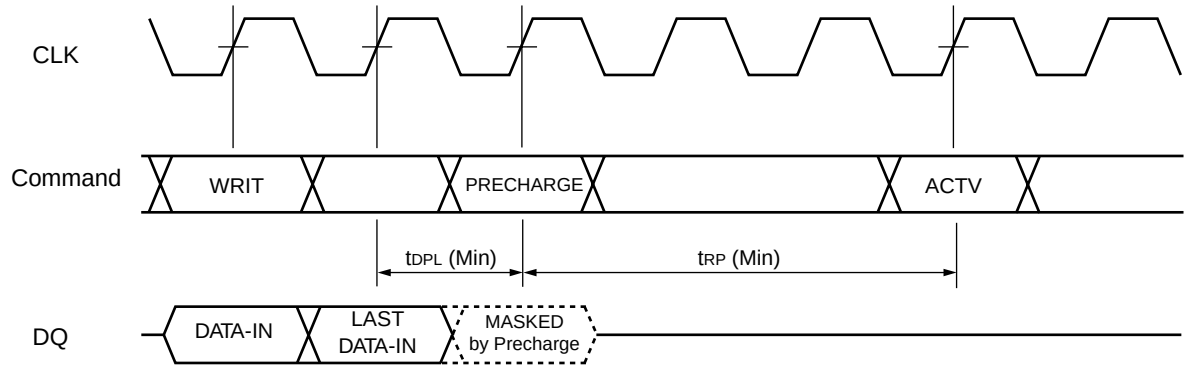
8. READ Interrupted by Burst Stop (Example @CL=2,BL = Full Column)



9. WRITE Interrupted by Burst Stop (Example @ BL = 2)

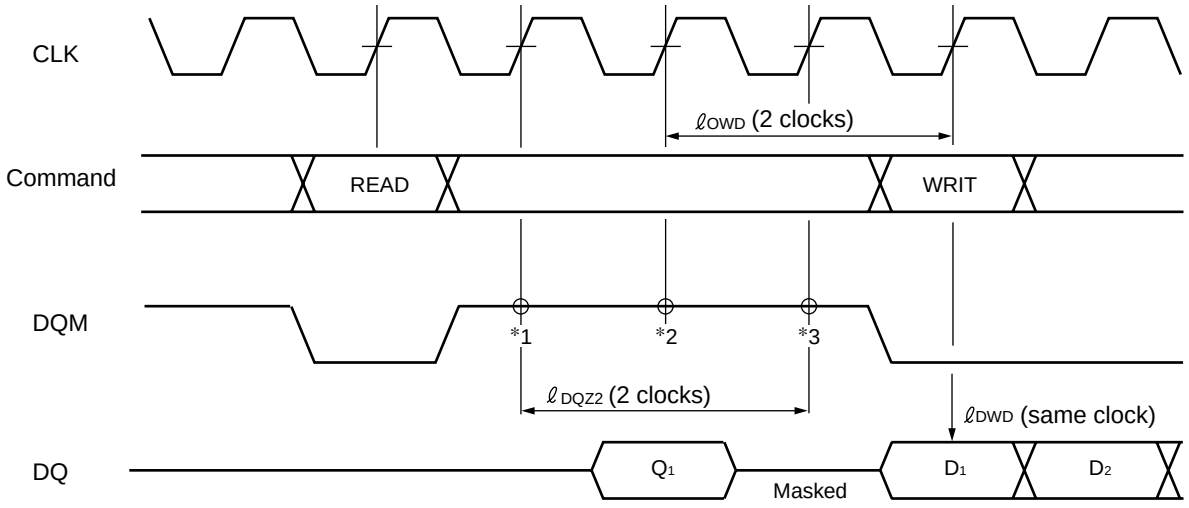


10. WRITE Interrupted by Precharge (Example @ CL = 2)



Note : The precharge command (PRE) should only be issued after the t_{DPL} of final data input is satisfied.
PRECHARGE means 'PRE' or 'PALL'.

11. READ Interrupted by WRITE (Example @ CL = 2, BL ≥ 4)

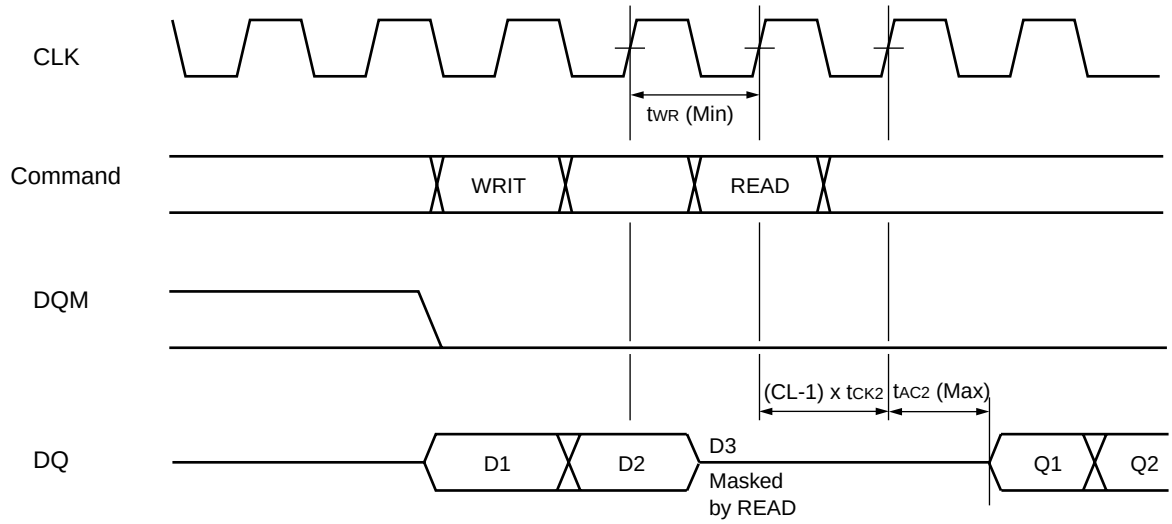


*1: The first DQM makes high-impedance state High-Z between last output and first input data.

*2: The second DQM makes internal output data mask to avoid bus contention.

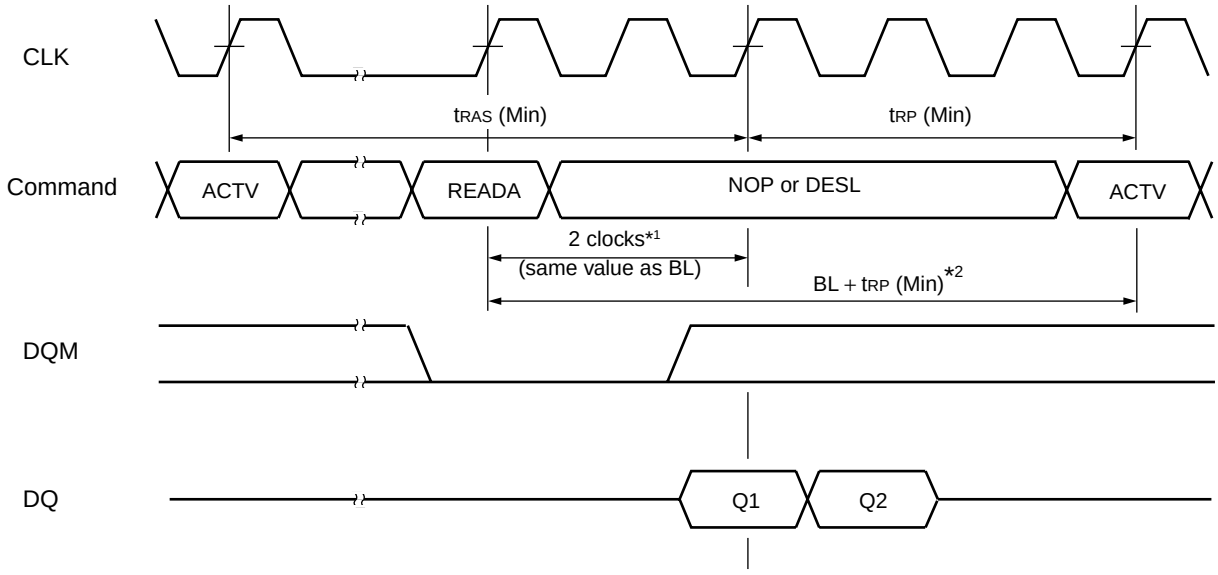
*3: The third DQM also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

12. WRITE to READ Timing (Example @ CL = 2, BL = 4)



Note : • Read command should be issued after t_{WR} of final data input is satisfied.
• The write data after the READ command is masked by the READ command.

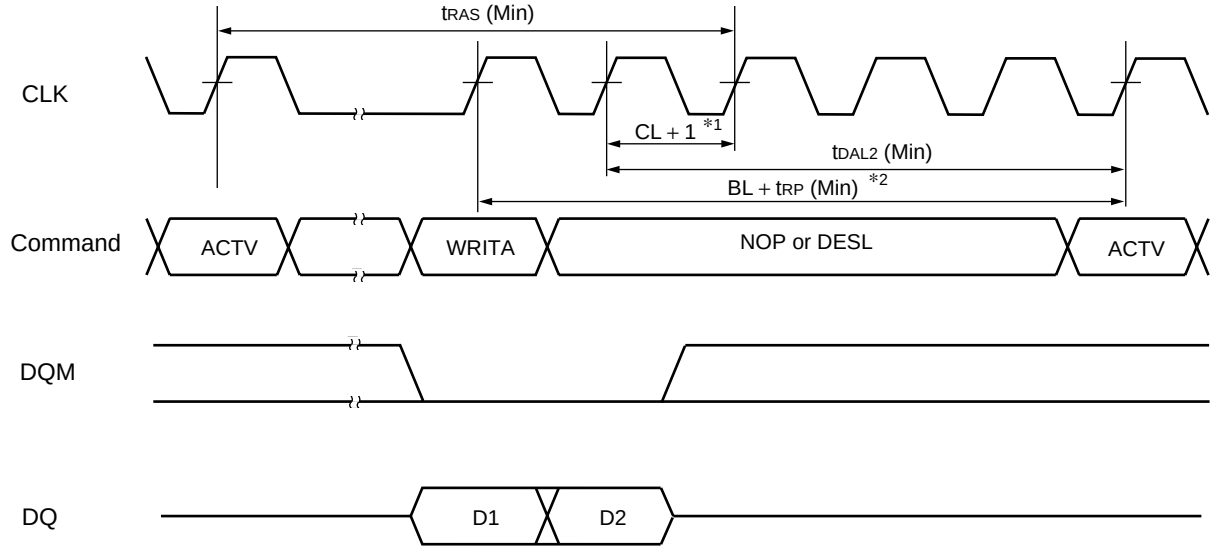
13. READ with Auto-Precharge (EXAPLE @ CL = 2, BL = 2 Applied to same bank)



*1: Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.

*2: The next ACTV command should be issued after BL+t_{RP} (Min) from READA command.

14. WRITE with Auto-Precharge (Example @ CL = 2, BL = 2 Applied to same bank)

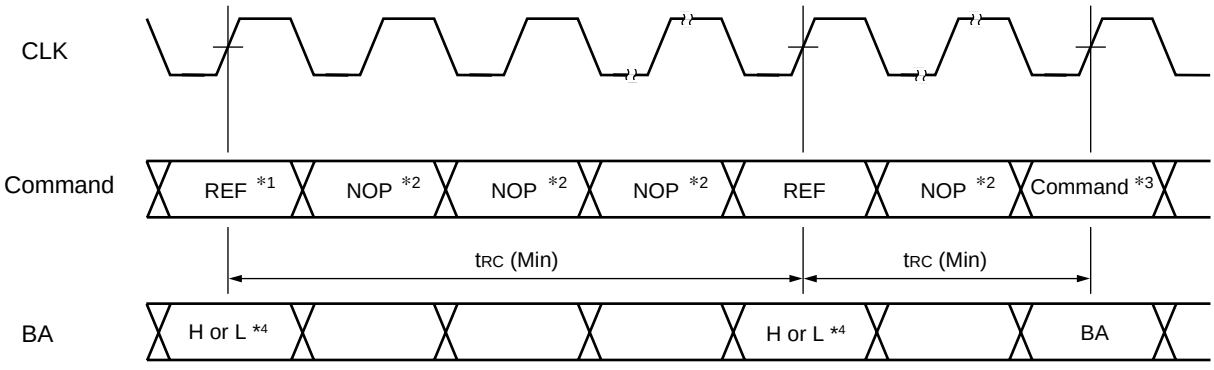


*1: Precharge at write with Auto-precharge is started after CL - 1 from the end of burst.

*2: The next command should be issued after BL+ t_{RP} (Min) at CL = 2 from WRITA command.

Notes:
- Even if the final data is masked by DQM, the precharge does not start the clock of final data input.
- Once the auto precharge command is asserted, no new command within the same bank can be issued.
- Auto-precharge command doesn't affect at full column burst operation except Burst READ & Single Write.

15. Auto-Refresh Timing



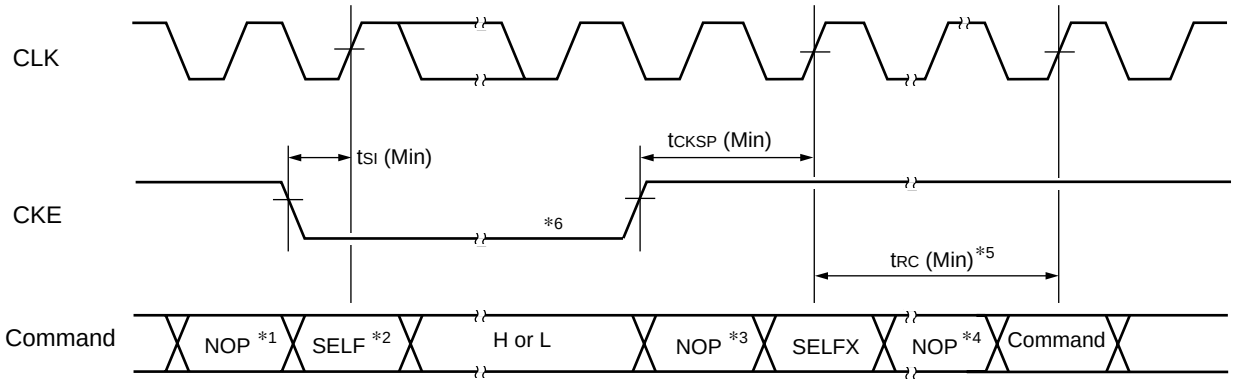
*1: All banks should be precharged prior to the first Auto-refresh command (REF).

*2: Either NOP or DESL command should be asserted during t_{RC} period while Auto-refresh mode.

*3: Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{RC} from the last REF command.

*4: Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.

16. Self-Refresh Entry and Exit Timing



*1: The precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).

*2: SELF command should be issued only after the last read data has been appeared on DQ.

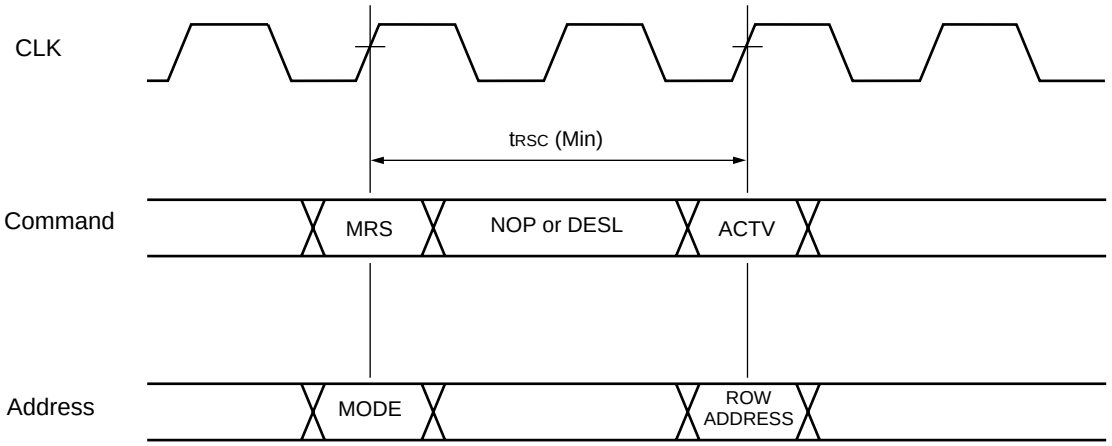
*3: The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (Min). It is recommended to apply NOP command in conjunction with CKE.

*4: Either NOP or DESL command can be used during t_{RC} period.

*5: CKE should be held high within one t_{RC} period after t_{CKSP}.

*6: CKE level should be held less than 0.2 V during self-refresh mode.

17. Mode Register Set Timing



Note : The Mode Register Set command (MRS) should only be asserted after all banks have been precharged and DQ is in High-Z.

■ ORDERING INFORMATION

Part number	Configuration	Shipping form	Remarks
MB811L646449-12WFKT	524,288 word × 32 bit × 2 bank × 2 part	wafer	
MB811L646449-18WFKT	524,288 word × 32 bit × 2 bank × 2 part	wafer	

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