FLASH MEMORY

CMOS

8 M (1 M × 8/512 K × 16) BIT

MBM29SL800TD/BD-10/12

■ DESCRIPTION

The MBM29SL800TD/BD are a 8 M-bit, 1.8 V-only Flash memory organized as 1 Mbytes of 8 bits each or 512 Kwords of 16 bits each. The MBM29SL800TD/BD are offered in a 48-pin TSOP (I) , and 48-ball FBGA packages. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

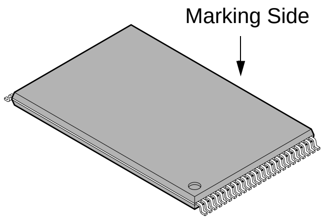
(Continued)

■ PRODUCT LINE UP

Part No.		MBM29SL800TD/MBM29SL800BD	
Ordering Part No.	V_{CC} = +2.0 V ± 0.2	–10	–12
Max. Address Access Time (ns)		100	120
Max. $\overline{CE}$ Access Time (ns)		100	120
Max. $\overline{OE}$ Access Time (ns)		35	50

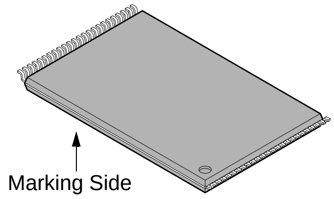
■ PACKAGE

48-pin Plastic TSOP (I)



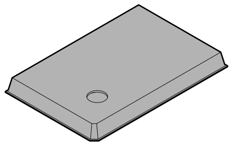
(FPT-48P-M19)

48-pin Plastic TSOP (I)



(FPT-48P-M20)

48-pin Plastic FBGA



(BGA-48P-M02)

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The standard MBM29SL800TD/BD offer access times 100 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$) , write enable ($\overline{WE}$) , and output enable ($\overline{OE}$) controls.

The MBM29SL800TD/BD are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29SL800TD/BD are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.5 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29SL800TD/BD are erased when shipped from the factory.

The devices feature single 1.8 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

Fujitsu’s Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29SL800TD/BD memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

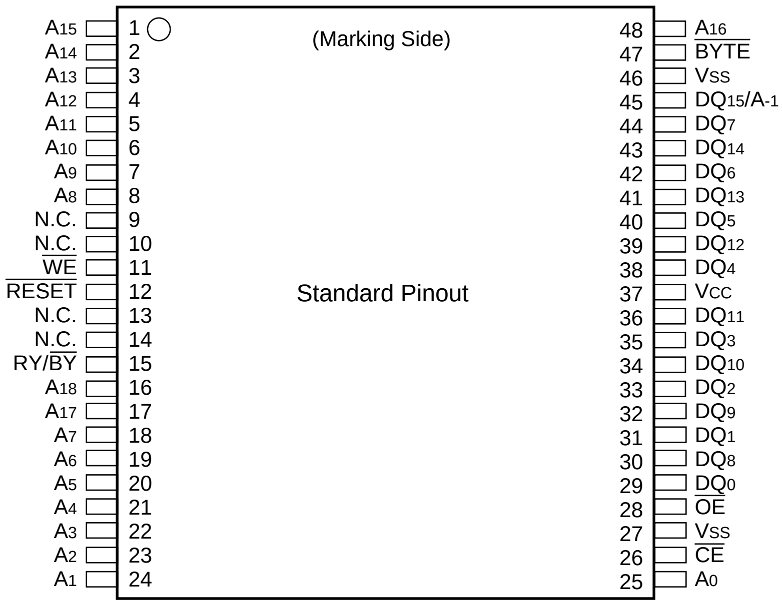
■ FEATURES

- **Single 1.8 V read, program, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  48-pin TSOP (I) (Package suffix : TN – Normal Bend Type, TR – Reversed Bend Type)
  48-ball FBGA (Package suffix : PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  100 ns maximum access time
- **Sector erase architecture**
  One 8 Kword, two 4 Kwords, one 16 Kword, and fifteen 32 Kwords sectors in word mode
  One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and fifteen 64 Kbytes sectors in byte mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection set function by Extended sector Protect command**
- **Temporary sector unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin

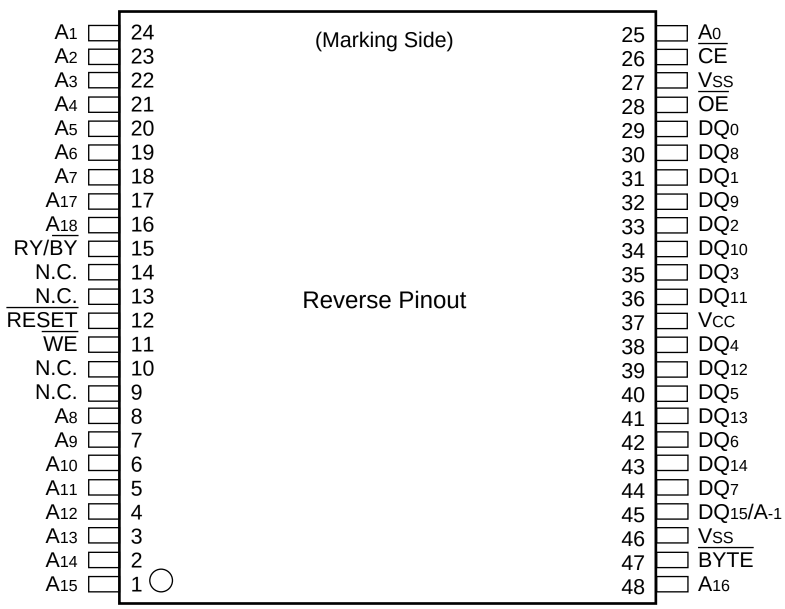
Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP (I)



(FPT-48P-M19)



(FPT-48P-M20)

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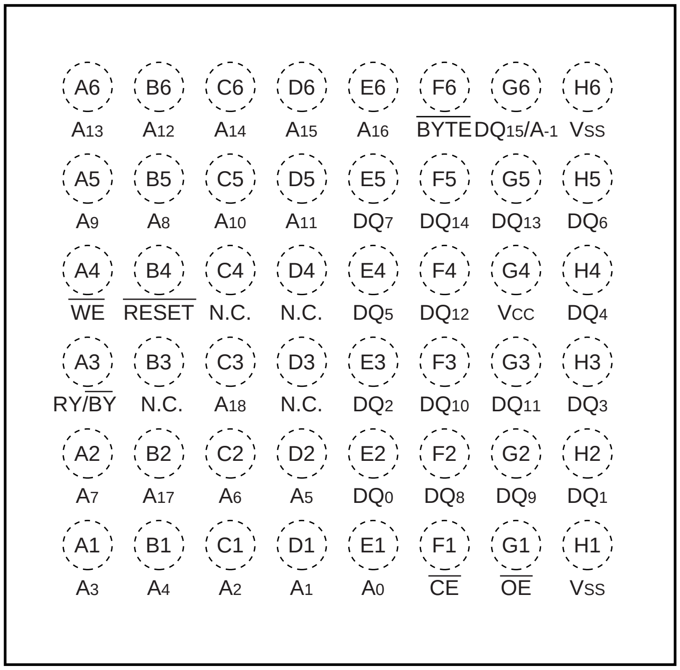
FBGA
(TOP VIEW)
Marking side



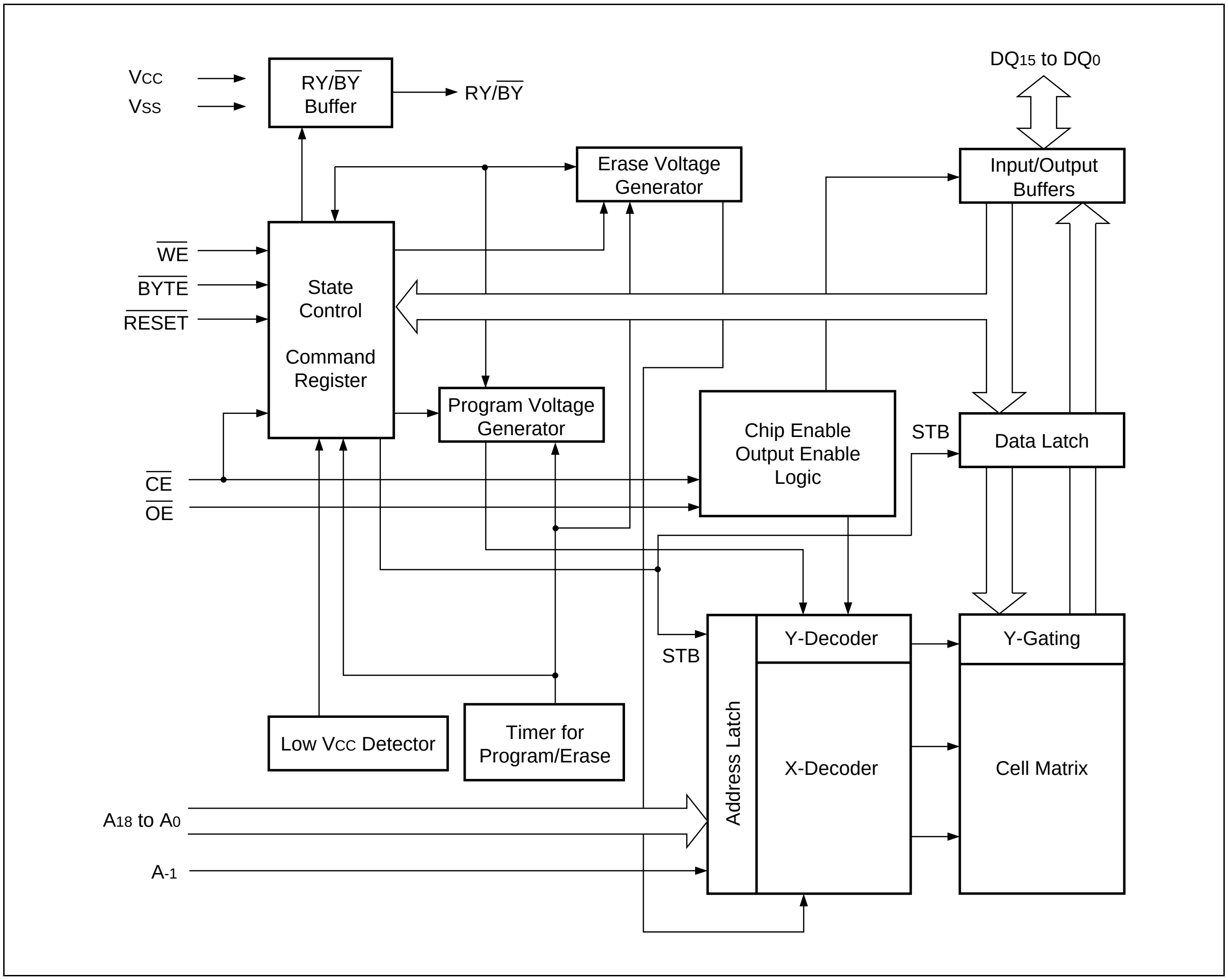
(BGA-48P-M02)

■ PIN DESCRIPTION

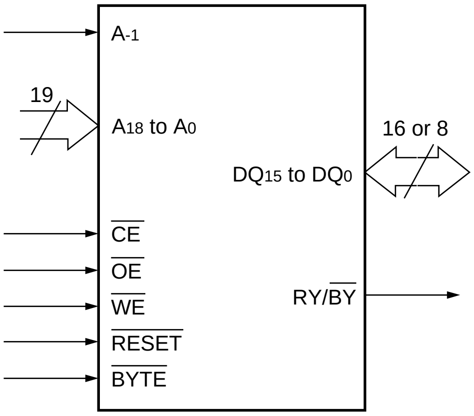
Table 1　MBM29SL800TD/800BD Pin Configuration

Pin name	Function
A_{18} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Hardware Reset Pin/Temporary Sector Unprotection
RY/$\overline{\text{BY}}$	Ready/Busy Output
$\overline{\text{BYTE}}$	Selects 8-bit or 16-bit mode
V_{SS}	Device Ground
V_{CC}	Device Power Supply
N.C.	No Internal Connection

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

Table 2 MBM29SL800TD/800BD User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code *1	L	L	H	H	L	L	V_{ID}	Code	H
Read *3	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection *2, *4	L	V_{ID}	$\sqcup$	L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	High-Z	L

Table 3 MBM29SL800TD/800BD User Bus Operations ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/ A_{-1}	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	L	V_{ID}	Code	H
Auto-Select Device Code *1	L	L	H	L	H	L	L	V_{ID}	Code	H
Read *3	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection *2, *4	L	V_{ID}	$\sqcup$	L	L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection *5	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	X	High-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, $\sqcup$ = Pulse input. See DC Characteristics for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See Table 4.

*2: Refer to the section on Sector Protection.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 2.0 V ± 10%

*5: It is also used for the extended sector protection.

Table 4 MBM29SL800TD/800BD Standard Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/ Reset	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/ Reset	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Sector Erase Suspend			Erase can be suspended during sector erase with Addr. ("H" or "L") . Data (B0h)											
Sector Erase Resume			Erase can be resumed after suspend with Addr. ("H" or "L") . Data (30h)											

Notes : 1. Address bits A_{11} to A_{18} = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA)

2. Bus operations are defined in Tables 2 and 3.
3. RA = Address of the memory location to be read
   PA = Address of the memory location to be programmed
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
5. The system should generate the following address patterns :
   Word Mode : 555h or 2AAh to addresses A_0 to A_{10}
   Byte Mode : AAAh or 555h to addresses A_{-1} and A_0 to A_{10}
6. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

Table 5 MBM29SL800TD/BD Extended Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—
	Byte		AAAh		555h		AAAh			
Fast Program (Note)	Word	2	XXXh	A0h	PA	PD	—	—	—	—
	Byte		XXXh							
Reset from Fast Mode (Note)	Word	2	XXXh	90h	XXXh	F0h	—	—	—	—
	Byte		XXXh		XXXh					
Extended Sector Protect	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD
	Byte									

SPA : Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0) .
SD : Sector protection verify data. Output 01h at protected sector address and output 00h at unprotected sector address.

Note : This command is valid while Fast Mode.

Table 6.1 MBM29SL800TD/800BD Sector Protection Verify Autoselect Codes

Type			A_{12} to A_{18}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29SL800TD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	EAh
		Word					X	22EAh
	MBM29SL800BD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	6Bh
		Word					X	226Bh
Sector Protection			Sector Address	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for Byte mode.

*2 : Outputs 01h at protected sector address and outputs 00h at unprotected sector address.

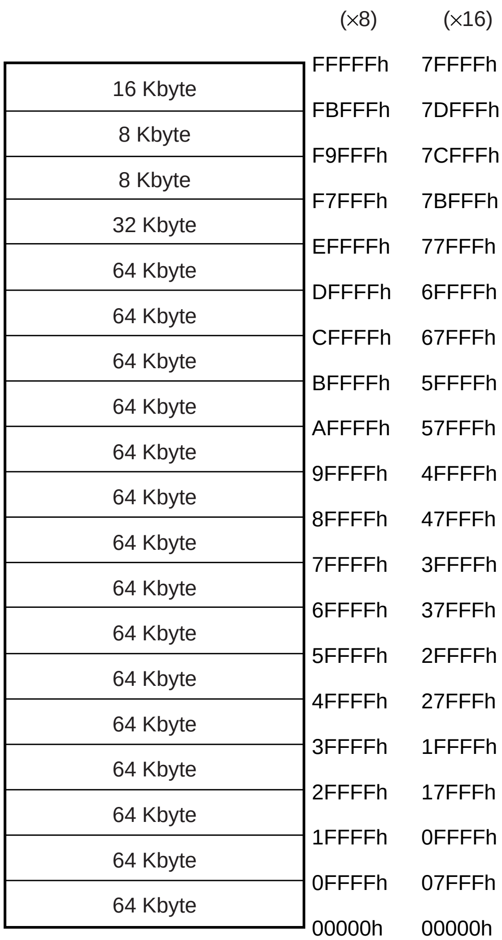
Table 6.2 Expanded Autoselect Code

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29SL 800TD	(B)	EAh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	1	0	1	0	1	0
		(W)	22EAh	0	0	1	0	0	0	1	0	1	1	1	0	1	0	1	0
	MBM29SL 800BD	(B)	6Bh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	1	0	1	0	1	1
		(W)	226Bh	0	0	1	0	0	0	1	0	0	1	1	0	1	0	1	1
Sector Protection			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

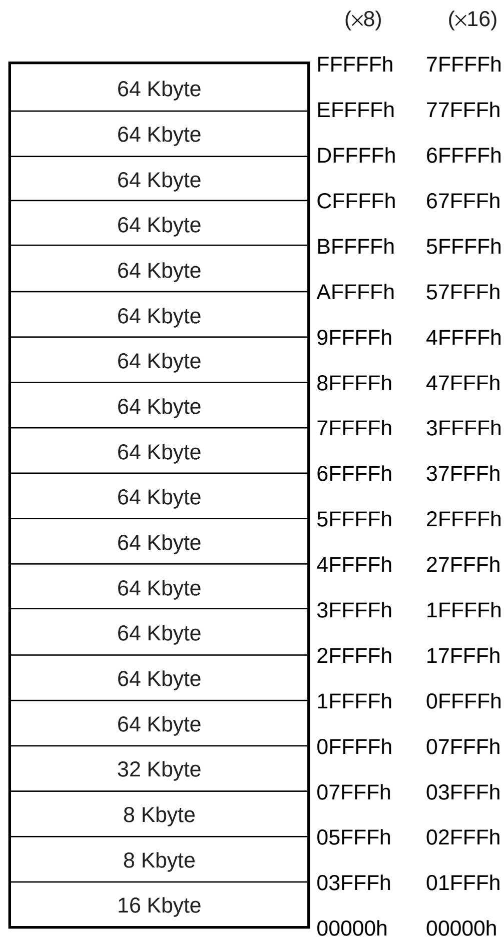
(B) : Byte mode
(W) : Word mode

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and fifteen 64 Kbytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.



MBM29SL800TD Sector Architecture



MBM29SL800BD Sector Architecture

Table 7 Sector Address Tables (MBM29SL800TD)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	X	X	X	00000h to 0FFFFh	00000h to 07FFFh
SA1	0	0	0	1	X	X	X	10000h to 1FFFFh	08000h to 0FFFFh
SA2	0	0	1	0	X	X	X	20000h to 2FFFFh	10000h to 17FFFh
SA3	0	0	1	1	X	X	X	30000h to 3FFFFh	18000h to 1FFFFh
SA4	0	1	0	0	X	X	X	40000h to 4FFFFh	20000h to 27FFFh
SA5	0	1	0	1	X	X	X	50000h to 5FFFFh	28000h to 2FFFFh
SA6	0	1	1	0	X	X	X	60000h to 6FFFFh	30000h to 37FFFh
SA7	0	1	1	1	X	X	X	70000h to 7FFFFh	38000h to 3FFFFh
SA8	1	0	0	0	X	X	X	80000h to 8FFFFh	40000h to 47FFFh
SA9	1	0	0	1	X	X	X	90000h to 9FFFFh	48000h to 4FFFFh
SA10	1	0	1	0	X	X	X	A0000h to AFFFFh	50000h to 57FFFh
SA11	1	0	1	1	X	X	X	B0000h to BFFFFh	58000h to 5FFFFh
SA12	1	1	0	0	X	X	X	C0000h to CFFFFh	60000h to 67FFFh
SA13	1	1	0	1	X	X	X	D0000h to DFFFFh	68000h to 6FFFFh
SA14	1	1	1	0	X	X	X	E0000h to EFFFFh	70000h to 77FFFh
SA15	1	1	1	1	0	X	X	F0000h to F7FFFh	78000h to 7BFFFh
SA16	1	1	1	1	1	0	0	F8000h to F9FFFh	7C000h to 7CFFFh
SA17	1	1	1	1	1	0	1	FA000h to FBFFFh	7D000h to 7DFFFh
SA18	1	1	1	1	1	1	X	FC000h to FFFFFh	7E000h to 7FFFFh

Table 8 Sector Address Tables (MBM29SL800BD)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	0	0	X	00000h to 03FFFh	00000h to 01FFFh
SA1	0	0	0	0	0	1	0	04000h to 05FFFh	02000h to 02FFFh
SA2	0	0	0	0	0	1	1	06000h to 07FFFh	03000h to 03FFFh
SA3	0	0	0	0	1	X	X	08000h to 0FFFFh	04000h to 07FFFh
SA4	0	0	0	1	X	X	X	10000h to 1FFFFh	08000h to 0FFFFh
SA5	0	0	1	0	X	X	X	20000h to 2FFFFh	10000h to 17FFFh
SA6	0	0	1	1	X	X	X	30000h to 3FFFFh	18000h to 1FFFFh
SA7	0	1	0	0	X	X	X	40000h to 4FFFFh	20000h to 27FFFh
SA8	0	1	0	1	X	X	X	50000h to 5FFFFh	28000h to 2FFFFh
SA9	0	1	1	0	X	X	X	60000h to 6FFFFh	30000h to 37FFFh
SA10	0	1	1	1	X	X	X	70000h to 7FFFFh	38000h to 3FFFFh
SA11	1	0	0	0	X	X	X	80000h to 8FFFFh	40000h to 47FFFh
SA12	1	0	0	1	X	X	X	90000h to 9FFFFh	48000h to 4FFFFh
SA13	1	0	1	0	X	X	X	A0000h to AFFFFh	50000h to 57FFFh
SA14	1	0	1	1	X	X	X	B0000h to BFFFFh	58000h to 5FFFFh
SA15	1	1	0	0	X	X	X	C0000h to CFFFFh	60000h to 67FFFh
SA16	1	1	0	1	X	X	X	D0000h to DFFFFh	68000h to 6FFFFh
SA17	1	1	1	0	X	X	X	E0000h to EFFFFh	70000h to 77FFFh
SA18	1	1	1	1	X	X	X	F0000h to FFFFFh	78000h to 7FFFFh

■ FUNCTIONAL DESCRIPTION

Read Mode

The MBM29SL800TD/BD have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or change $\overline{CE}$ pin from “H” to “L”

Standby Mode

There are two ways to implement the standby mode on the MBM29SL800TD/BD devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 µA. The device can be read with standard access time (t_{CE}) from either of these standby modes. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = “H”.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE}$ = “H” or “L”) . Under this condition the current is consumed is less than 5 µA. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29SL800TD/800BD data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, MBM29SL800TD/800BD automatically switch themselves to low power mode when MBM29SL800TD/800BD addresses remain stably during access fine of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 µA (CMOS Level) .

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29SL800TD/800BD read-out the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}) , output from the devices are disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (10 V to 11 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON’T CARES except A_0, A_1, A_6, and A_{-1}. (See Table 6.1.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29SL800TD/BD are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 4. (Refer to Autoselect Command section.)

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer’s code (Fujitsu = 04h) and ($A_0 = V_{IH}$) represents the device identifier code (MBM29SL800TD = EAh and MBM29SL800BD = 6Bh for ×8 mode; MBM29SL800TD = 22EAh and

MBM29SL800BD = 226Bh for ×16 mode) . These two bytes/words are given in the tables 6.1 and 6.2. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See Tables 6.1 and 6.2.)

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The MBM29SL800TD/BD feature hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 18) . The sector protection feature is enabled using programming equipment at the user's site. The devices are shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL}, and A_6 = V_{IL}. The sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. Tables 7 and 8 define the sector address for each of the nineteen (19) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See Figures 16 and 25 for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the devices will read 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29SL800TD/BD devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}) . During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. See Figures 17 and 26.

$\overline{RESET}$

Hardware Reset

The MBM29SL800TD/BD devices may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode 20 µs after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the devices require an additional t_{RH} before it will allow read access. When the $\overline{RESET}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See Figure 12 for the timing diagram. Refer to Temporary Sector Unprotection for additional functionality.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits ($DQ_5 = 1$) to read/reset mode, the read/reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h for ×16 (XX02h for ×8) returns the device code (MBM29SL800TD = EAh and MBM29SL800BD = 6Bh for ×8 mode; MBM29SL800TD = 22EAh and MBM29SL800BD = 226Bh for ×16 mode) . (See Tables 6.1 and 6.2.) All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address XX02h for ×16 (XX04h for ×8) . Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. The programming verification should be perform margin mode on the protected sector. (See Tables 2 and 3.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See Table 9, Hardware Sequence Flags.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from read/reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 21 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function) . The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

Figure 22 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data = 30h) is latched on the rising edge of $\overline{WE}$. After time-out of 50 µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 4. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command (s) . If another falling edge of the $\overline{WE}$ occurs within the 50 µs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 18) .

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function) . When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{\text{Data}}$ polling must be performed at an address within any of the sectors being erased. Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

Figure 22 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. Writting the Erase Suspend command during the

Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command resumes the erase operation. The addresses are DON'T CARES when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20 µs to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{BY}$ output pin and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{Data}$ polling of DQ_7, or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29SL800TD/BD has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to the Figure 28 Extended algorithm.) The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) . (Refer to the Figure 28 Extended algorithm.)

(3) Extended Sector Protection

In addition to normal sector protection, the MBM29SL800TD/BD has Extended Sector Protection as extended function. This function enable to protect sector by forcing V_{ID} on $\overline{RESET}$ pin and write a commnad sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protect requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector to be protected (recommend to set V_{IL} for the other addresses pins) , and write extended sector protect command (60h) . A sector is typically protected in 150 µs. To verify programming of the protection circuitry, the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h) . Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", please repeat to write extended sector protect command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}.

Write Operation Status

Table 9 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle *1	0	0	1 *2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1: Performing successive read operations from any address will cause DQ_6 to toggle.

*2: Reading the byte address being programmed while in the erase-suspend program mode will indicate logic “1” at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

Notes : 1. DQ_0 and DQ_1 are reserve pins for future use.
2. DQ_4 is Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29SL800TD/BD devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 23.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the MBM29SL800TD/BD data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the devices are driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 9.)

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ$_6$

Toggle Bit I

The MBM29SL800TD/BD also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the devices will result in DQ$_6$ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ$_6$ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ$_6$ to toggle. In addition, an Erase Suspend/Resume command will cause the DQ$_6$ to toggle.

See Figure 10 for the Toggle Bit I timing specifications and diagrams.

DQ$_5$

Exceeded Timing Limits

DQ$_5$ will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ$_5$ will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the devices under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA) . The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Tables 2 and 3.

The DQ$_5$ failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ$_7$ bit and DQ$_6$ never stops toggling. Once the devices have exceeded timing limits, the DQ$_5$ bit will indicate a "1." Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

DQ$_3$

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ$_3$ will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ$_3$ may be used to determine if the sector erase timer window is still open. If DQ$_3$ is high ("1") the internally controlled erase cycle has begun. If DQ$_3$ is low ("0") the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ$_3$ prior to and following each subsequent Sector Erase command. If DQ$_3$ were high on the second status check, the command may not have been accepted.

See Table 9 : Hardware Sequence Flags.

DQ$_2$

Toggle Bit II

This toggle bit II, along with DQ$_6$, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ$_2$ to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause

DQ_2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also Table 9 and Figure 18.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase-Suspend Read (Erase-Suspended Sector) *1	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle *1	1 *2

*1: Performing successive read operations from any address will cause DQ_6 to toggle.

*2: Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

RY/$\overline{BY}$

Ready/Busy

The MBM29SL800TD/BD provide a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/write or erase operation. If the MBM29SL800TD/BD are placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth $\overline{WE}$ pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth $\overline{WE}$ pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during the $\overline{RESET}$ pulse. Refer to Figure 11 and 12 for a detailed timing diagram. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Byte/Word Configuration

The $\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29SL800TD/BD devices. When this pin is driven high, the devices operate in the word (16-bit) mode. The data is read and programmed at DQ_0 to DQ_{15}. When this pin is driven low, the devices operate in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_8 to DQ_{14} bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_0 to DQ_7 and the DQ_8 to DQ_{15} bits are ignored. Refer to Figures 13, 14 and 15 for the timing diagram.

Data Protection

The MBM29SL800TD/BD are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector (s) cannot be used.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, and $\overline{RESET}$ *1	V_{IN}, V_{OUT}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+3.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *2	V_{IN}	–0.5	+11.5	V

*1: Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$ and $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} - V_{CC}) does not exceed 9.0 V. Maximum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins is +11.5 V which may overshoot to +12.5 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Parameter	Symbol	Part No.	Value		Unit
			Min.	Max.	
Ambient Temperature	T_A	MBM29SL800TD/BD-10/12	–40	+85	°C
Power Supply Voltage	V_{CC}	MBM29SL800TD/BD-10/12	+1.8	+2.2	V

Note: Operating ranges define those limits between which the proper device function is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/UNDERSHOOT

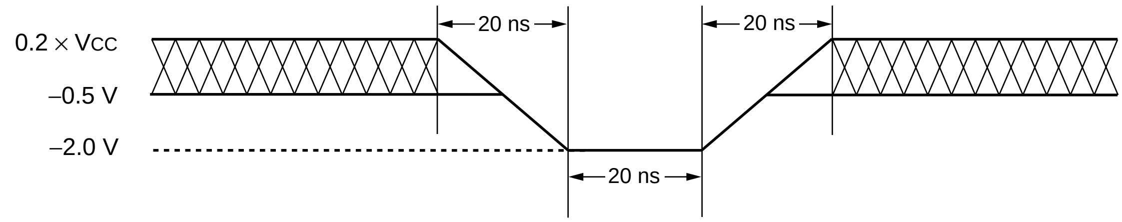


Figure 1 Maximum Undershoot Waveform

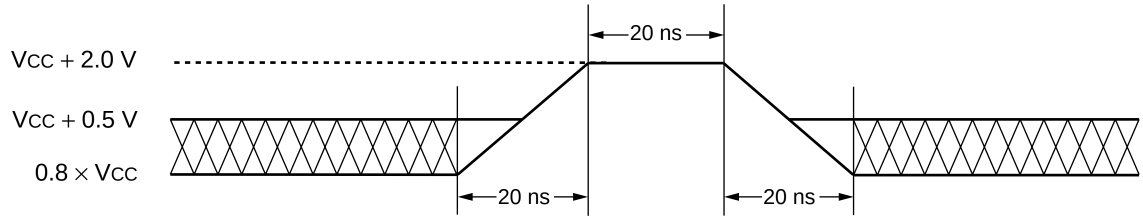
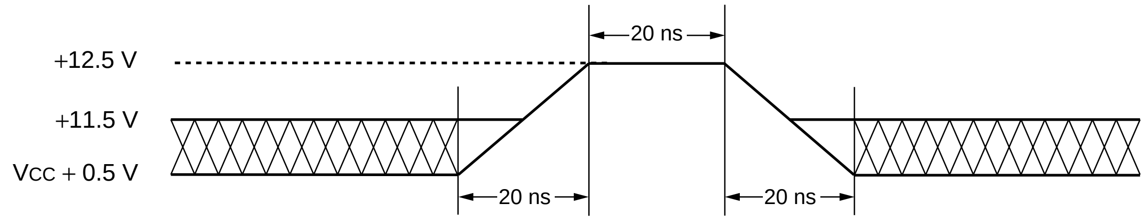


Figure 2 Maximum Overshoot Waveform 1



* : This waveform is applied for A9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions		Value Min.	Value Max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max. A_9, $\overline{OE}$, $\overline{RESET}$ = 11 V		—	35	µA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 10 MHz	Byte	—	20	mA
			Word		20	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz	Byte	—	10	mA
			Word		10	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	25	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	µA
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max., $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	µA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC5}	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	µA
Input Low Voltage Level	V_{IL}	—		–0.5	$0.2 \times V_{CC}$	V
Input High Voltage Level	V_{IH}	—		$0.8 \times V_{CC}$	$V_{CC} + 0.3$	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) *4, *5	V_{ID}	—		10	11	V
Output Low Voltage Level	V_{OL}	I_{OL} = 0.1 mA, $V_{CC} = V_{CC}$ Min.		—	0.1	V
Output High Voltage Level	V_{OH}	I_{OH} = –100 µA		$V_{CC} – 0.1$	—	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4: This timing is for Sector Protection operation.

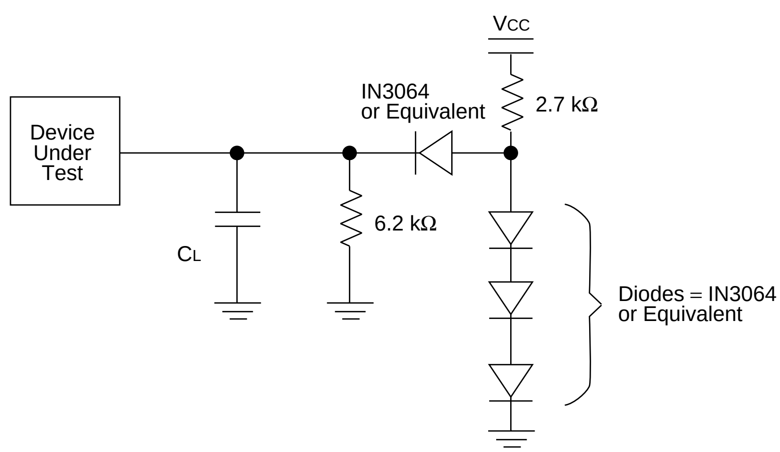
*5: Applicable for only V_{CC} applying.

■ AC CHARACTERISTICS

- **Read Only Operations Characteristics**

Parameter	Symbol		Test Setup	Value (Note)				Unit
				-10		-12		
	JEDEC	Standard		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{AVAV}	t_{RC}	—	100	—	120	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	—	120	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	100	—	120	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	35	—	50	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	30	—	40	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	30	—	40	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	—	20	µs
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	—	5	ns

Note : Test Conditions :
Output Load : 1 TTL gate and 30 pF (MBM29SL800TD/BD-10)
1 TTL gate and 100 pF (MBM29SL800TD/BD-12)
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to V_{CC}
Timing measurement reference level
Input : $0.5 \times V_{CC}$
Output : $0.5 \times V_{CC}$



Notes : C_L = 30 pF including jig capacitance (MBM29SL800TD/BD-10)
C_L = 100 pF including jig capacitance (MBM29SL800TD/BD-12)

Figure 4 Test Conditions

- **Write/Erase/Program Operations**

Parameter	Symbol		Value						Unit
			-10			-12			
	JEDEC	Standard	Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Cycle Time	t_{AVAV}	t_{WC}	100	—	—	120	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	50	—	—	60	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	50	—	—	60	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time	—	t_{OES}	0	—	—	0	—	—	ns
Output Enable Hold Time: Read	—	t_{OEH}	0	—	—	0	—	—	ns
Output Enable Hold Time: Toggle and $\overline{\text{Data}}$ Polling			10	—	—	10	—	—	ns
Read Recover Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write	t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Setup Time	t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Setup Time	t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Hold Time	t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	50	—	—	60	—	—	ns
$\overline{\text{CE}}$ Pulse Width	t_{ELEH}	t_{CP}	50	—	—	60	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	30	—	—	30	—	—	ns
$\overline{\text{CE}}$ Pulse Width High	t_{EHEL}	t_{CPH}	30	—	—	30	—	—	ns
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	—	10.6	—	—	10.6	—	µs
Sector Erase Operation *1	t_{WHWH2}	t_{WHWH2}	—	1.5	—	—	1.5	—	s
V_{CC} Setup Time	—	t_{VCS}	50	—	—	50	—	—	µs
Rise Time to V_{ID} *2	—	t_{VIDR}	500	—	—	500	—	—	ns
Voltage Transition Time *2	—	t_{VLHT}	4	—	—	4	—	—	µs
Write Pulse Width *2	—	t_{WPP}	100	—	—	100	—	—	µs
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active *2	—	t_{OESP}	4	—	—	4	—	—	µs
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active *2	—	t_{CSP}	4	—	—	4	—	—	µs
Recover Time From RY/$\overline{\text{BY}}$	—	t_{RB}	0	—	—	0	—	—	ns
$\overline{\text{RESET}}$ Pulse Width	—	t_{RP}	500	—	—	500	—	—	ns
$\overline{\text{RESET}}$ Hold Time Before Read	—	t_{RH}	200	—	—	200	—	—	ns
$\overline{\text{BYTE}}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	30	—	—	40	ns
$\overline{\text{BYTE}}$ Switching High to Output Active	—	t_{FHQV}	30	—	—	40	—	—	ns
Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay	—	t_{BUSY}	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	100	—	—	120	ns
Power On/Off Timing	—	t_{PS}	0	—	—	0	—	—	ns

*1: This does not include the preprogramming time.

*2: This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Remarks
	Min.	Typ.	Max.		
Sector Erase Time	—	1.5	15	s	Excludes programming time prior to erasure
Word Programming Time	—	14.6	360	µs	Excludes system-level overhead
Byte Programming Time	—	10.6	300	µs	
Chip Programming Time	—	7.7	200	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ TSOP (I) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ.	Max.	
Input Capacitance	C_{IN}	$V_{IN} = 0$	7.5	9.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8	10	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	10	13	pF

Note : Test conditions $T_A = 25$ °C, f = 1.0 MHz

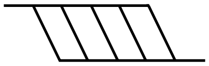
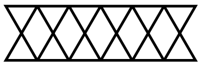
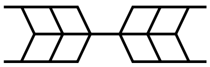
■ FBGA PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ.	Max.	
Input Capacitance	C_{IN}	$V_{IN} = 0$	7.5	9.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8	10	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	10	13	pF

Note : Test conditions $T_A = 25$ °C, , f = 1.0 MHz

■ TIMING DIAGRAM

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

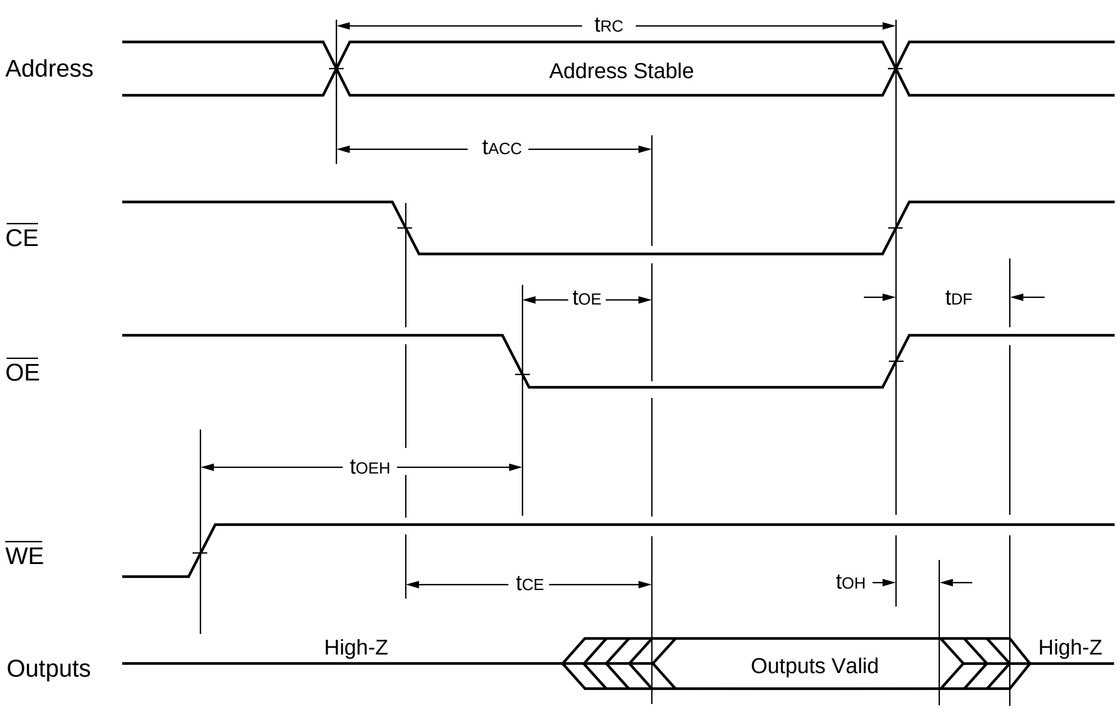


Figure 5.1 Read Operation Timing Diagram

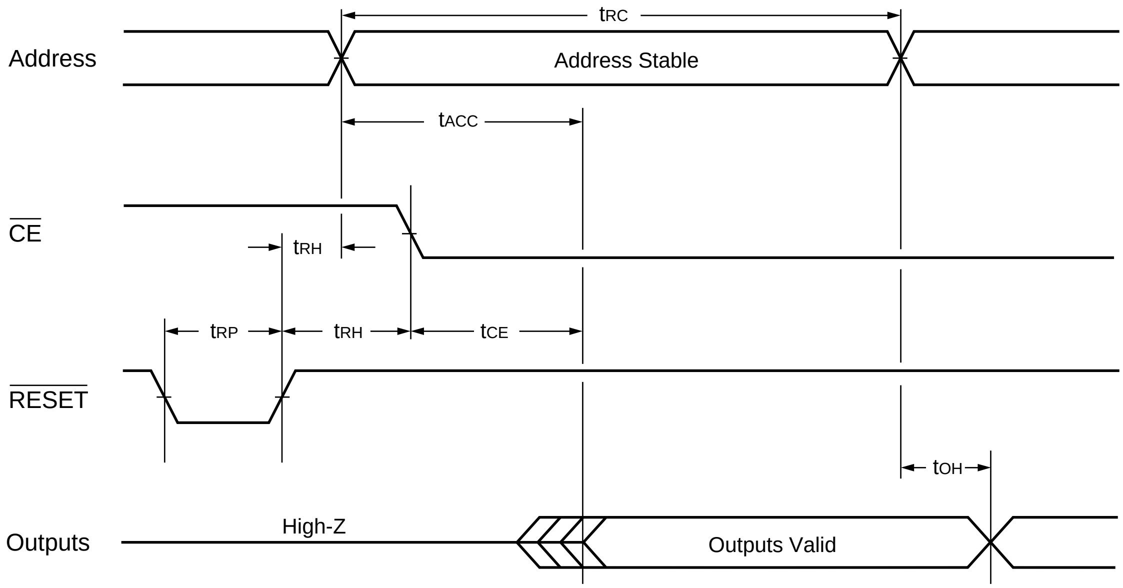
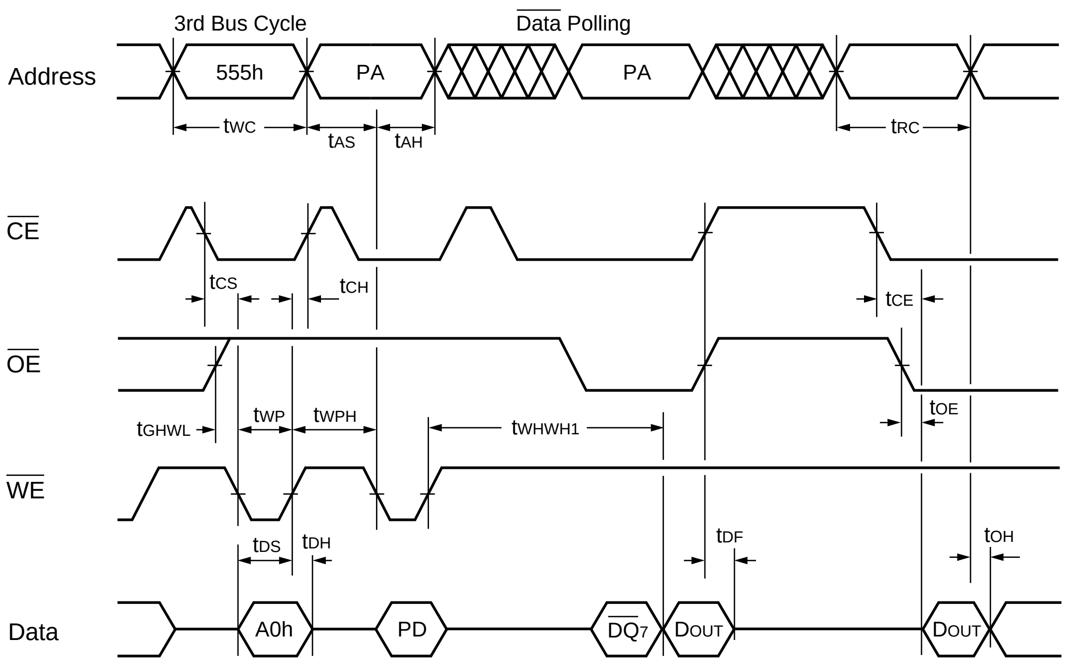
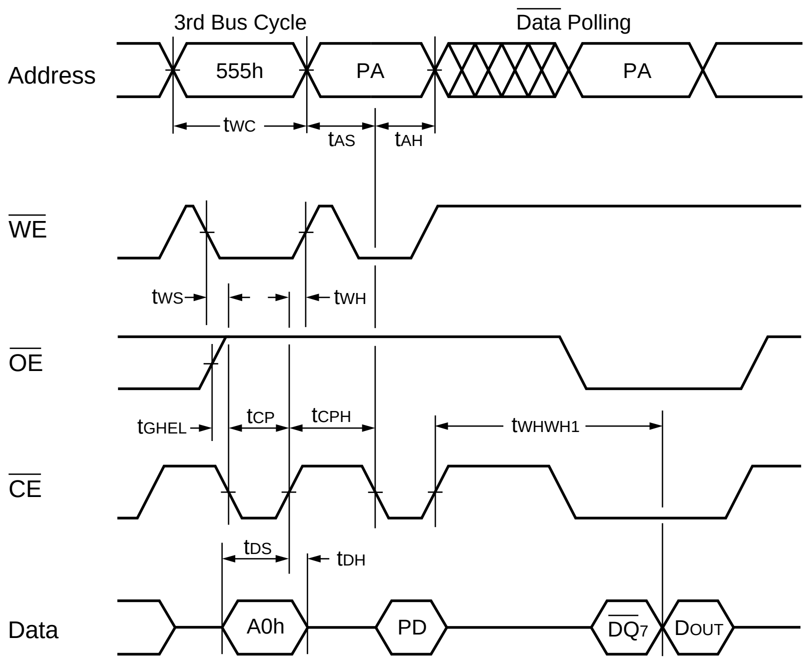


Figure 5.2 Hardware Reset/Read Operation Timing Diagram



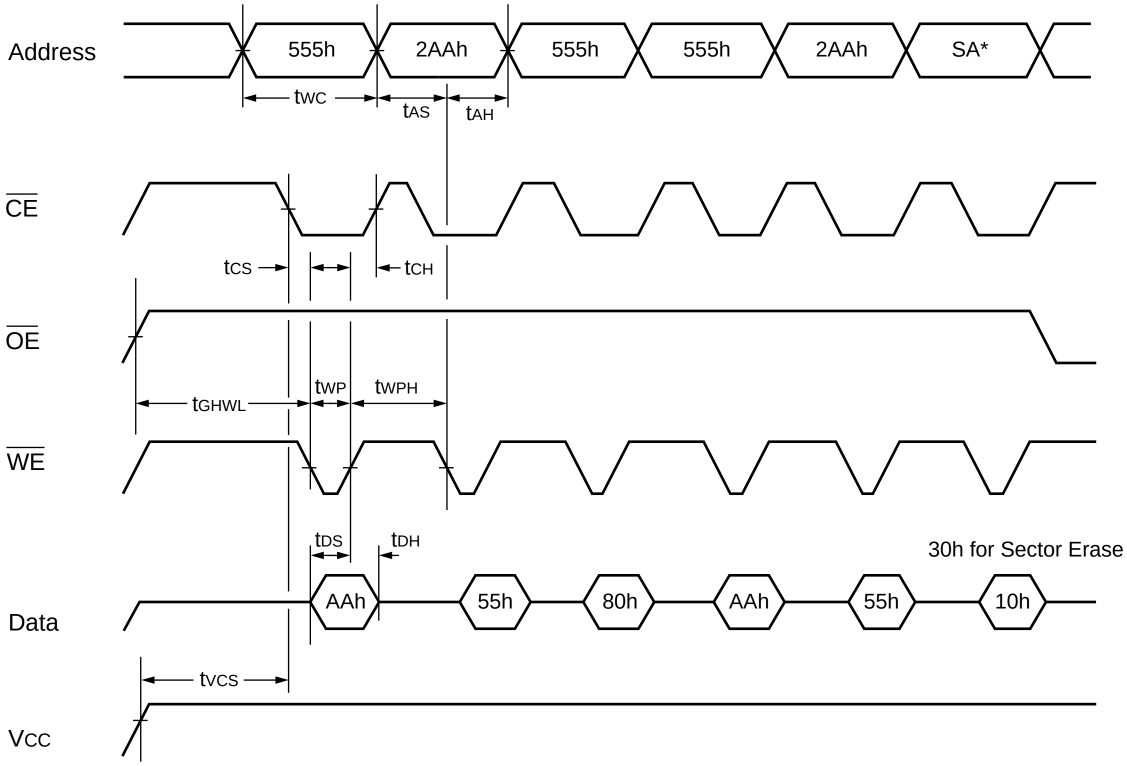
Notes : 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 6 Alternate $\overline{\text{WE}}$ Controlled Program Operation Timing Diagram



Notes : 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

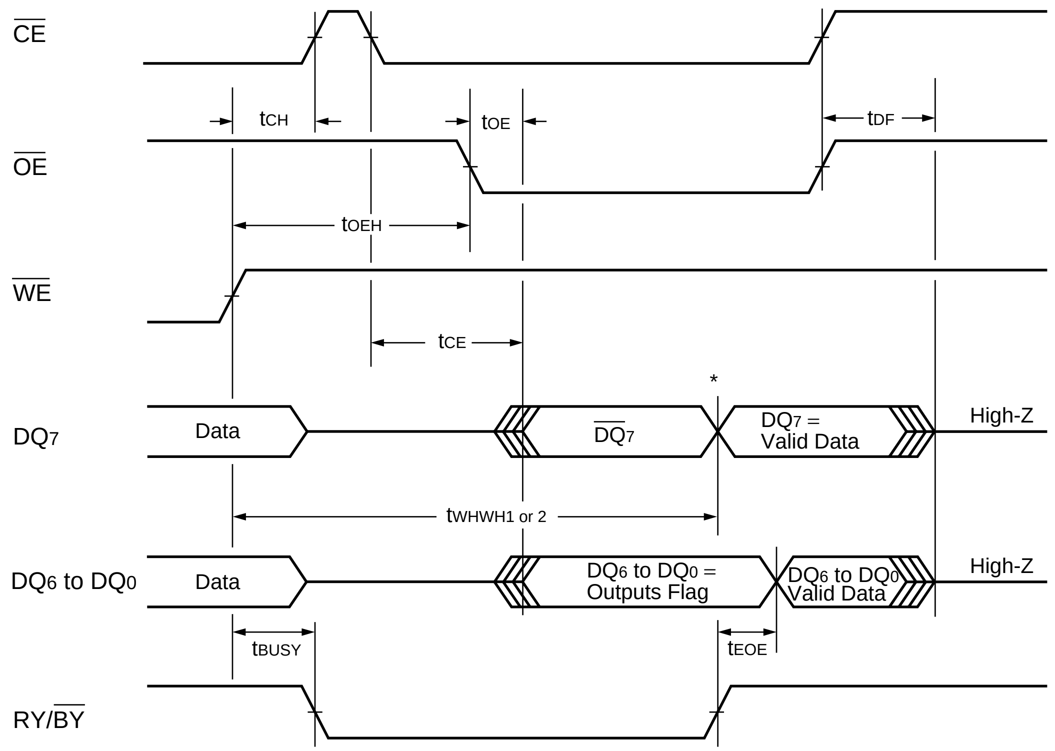
Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

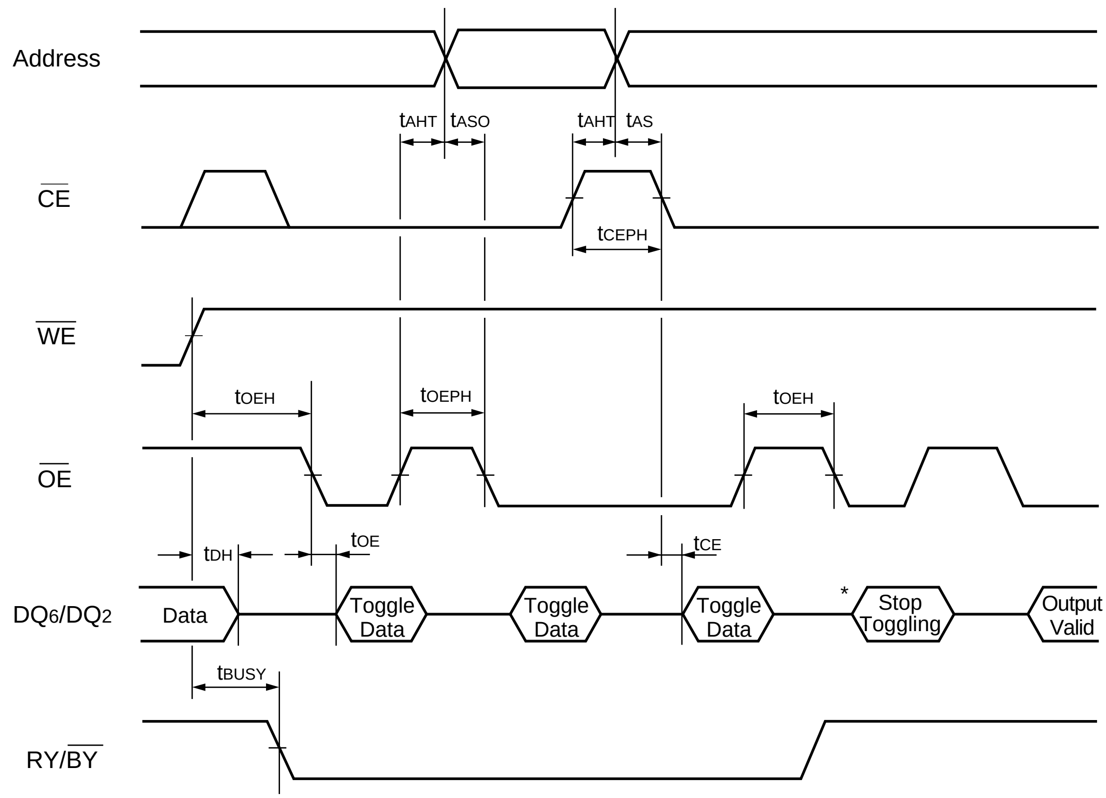
Note : These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 8 Chip/Sector Erase Operation Timing Diagram



* : DQ_7 = Valid Data (The device has completed the Embedded operation) .

Figure 9 Data Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_6 stops toggling (The device has completed the Embedded operation) .

Figure 10 AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

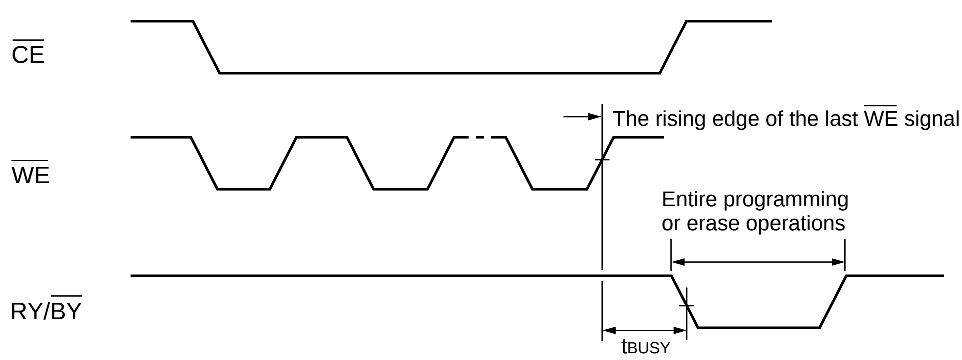


Figure 11 RY/BY Timing Diagram during Program/Erase Operation Timing Diagram

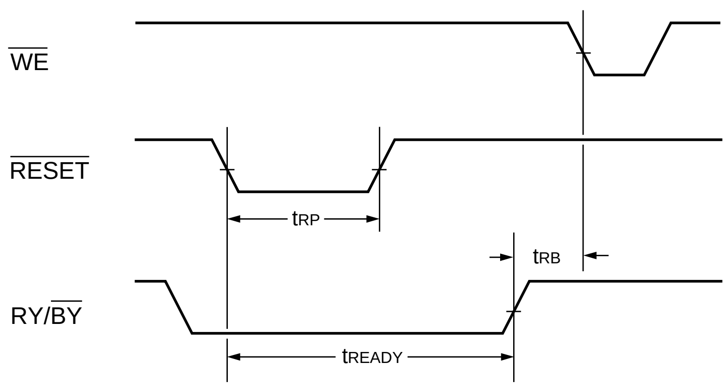


Figure 12 RESET, RY/BY Timing Diagram

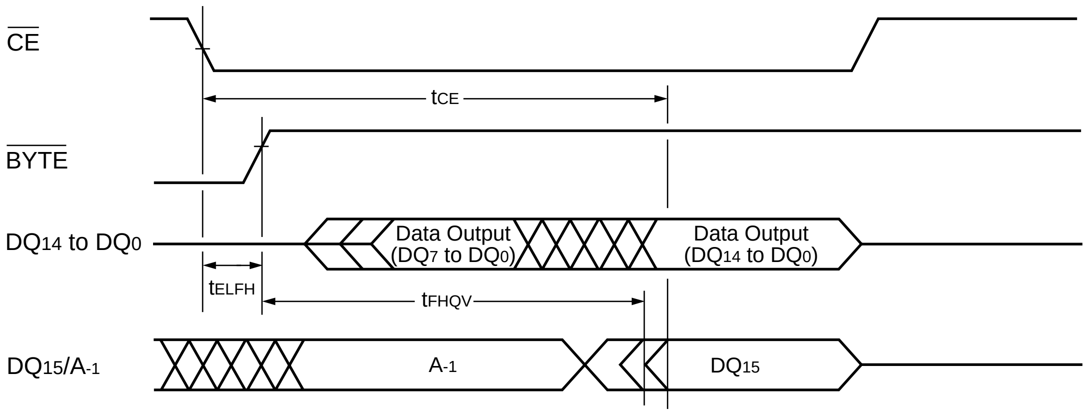


Figure 13 Timing Diagram for Word Mode Configuration

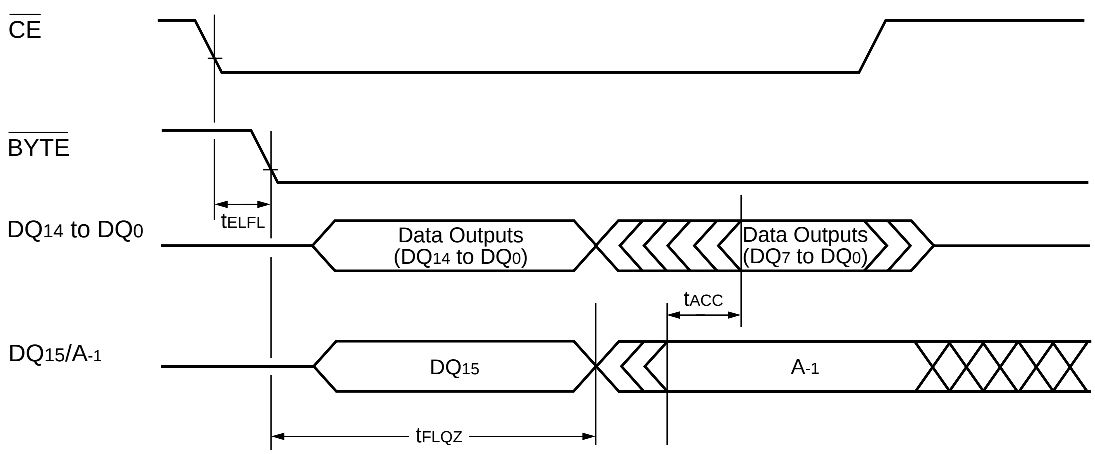


Figure 14 Timing Diagram for Byte Mode Configuration

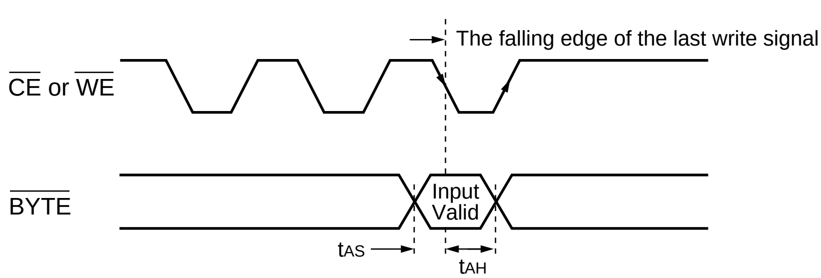
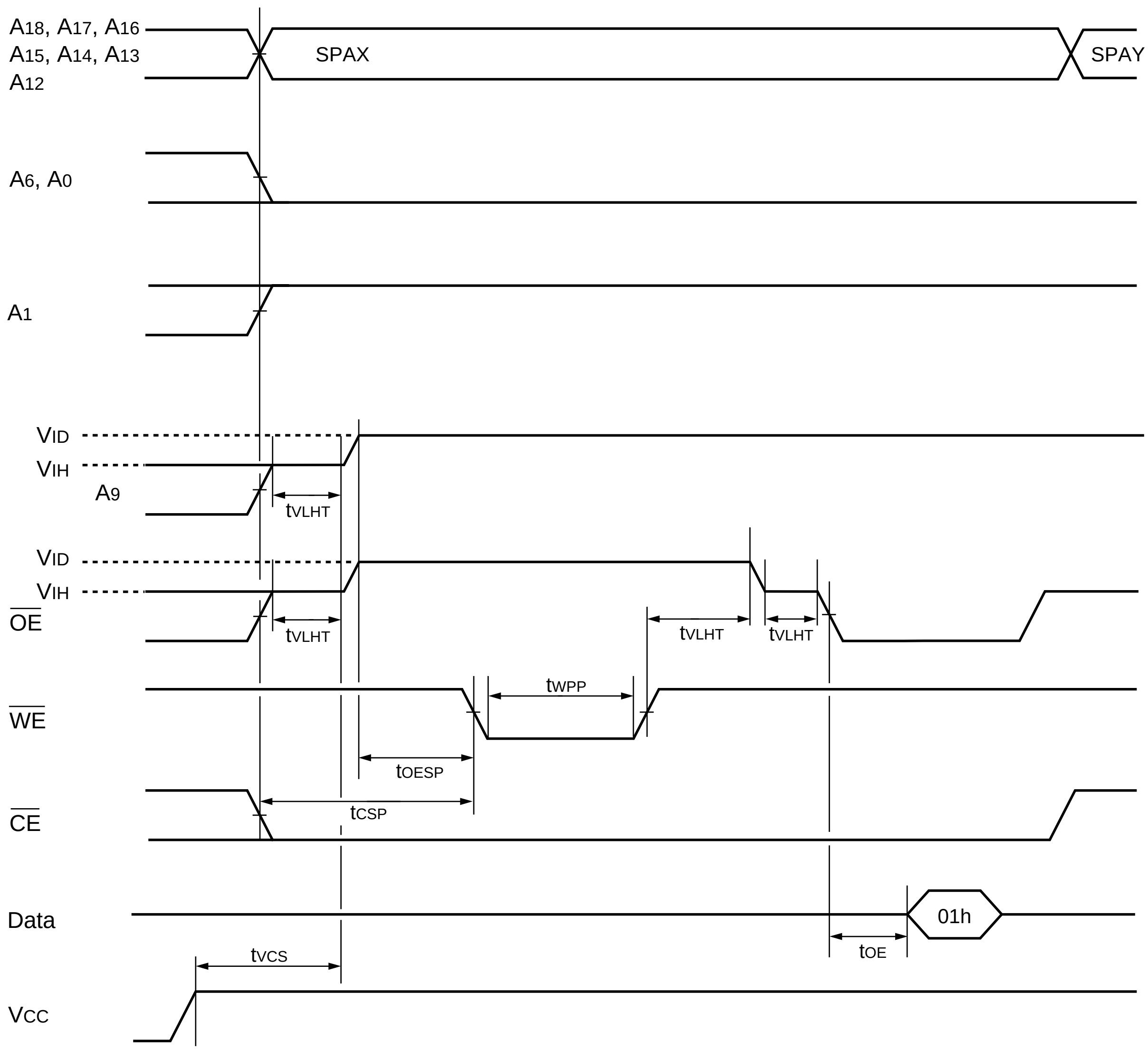


Figure 15 $\overline{\text{BYTE}}$ Timing Diagram for Write Operations



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
Note : A_{-1} is V_{IL} on byte mode.

Figure 16 Sector Protection Timing Diagram

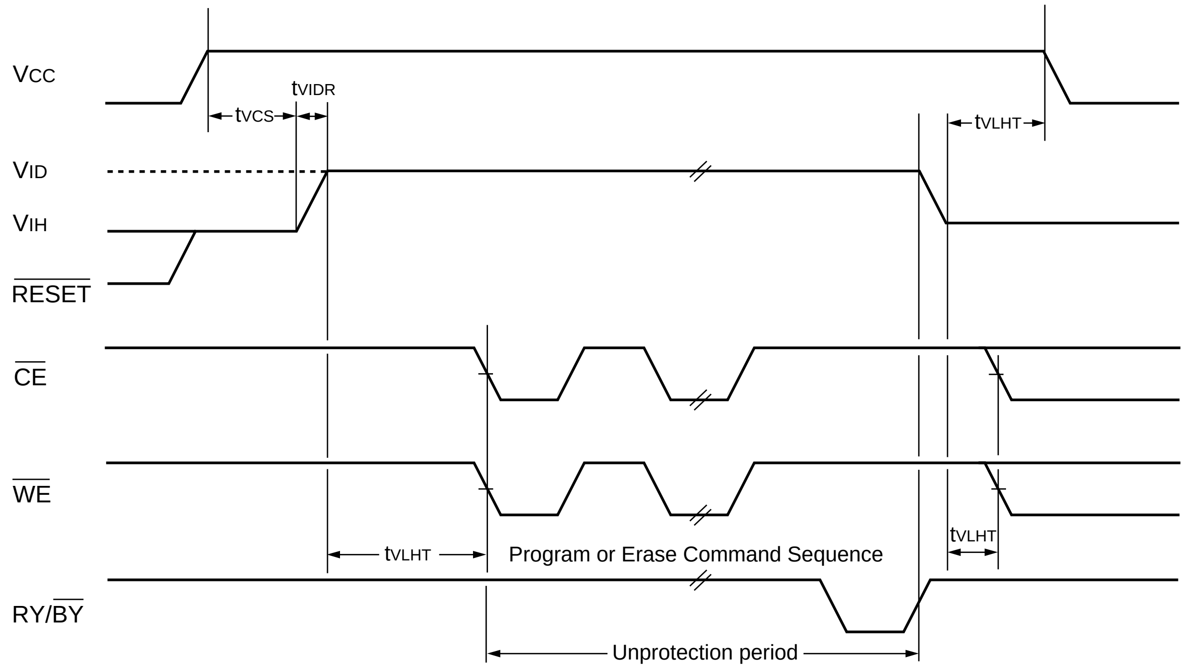
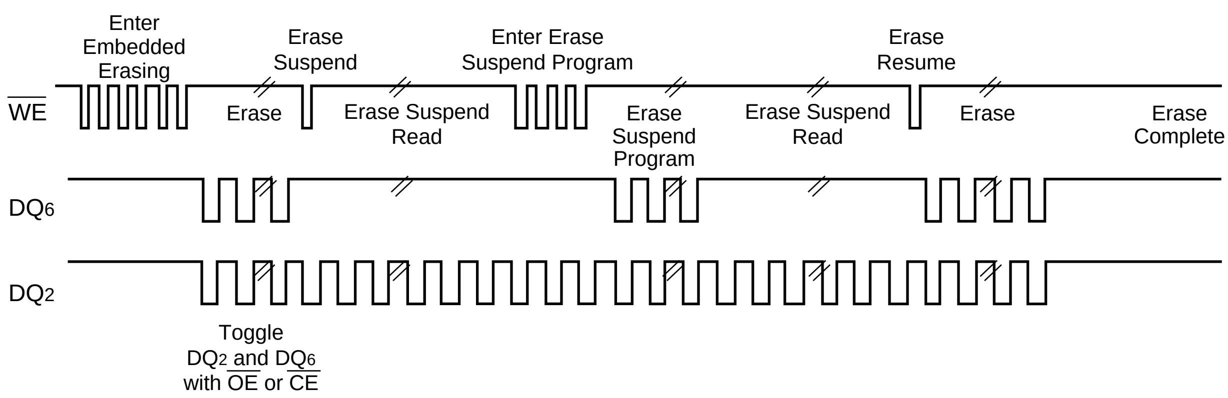
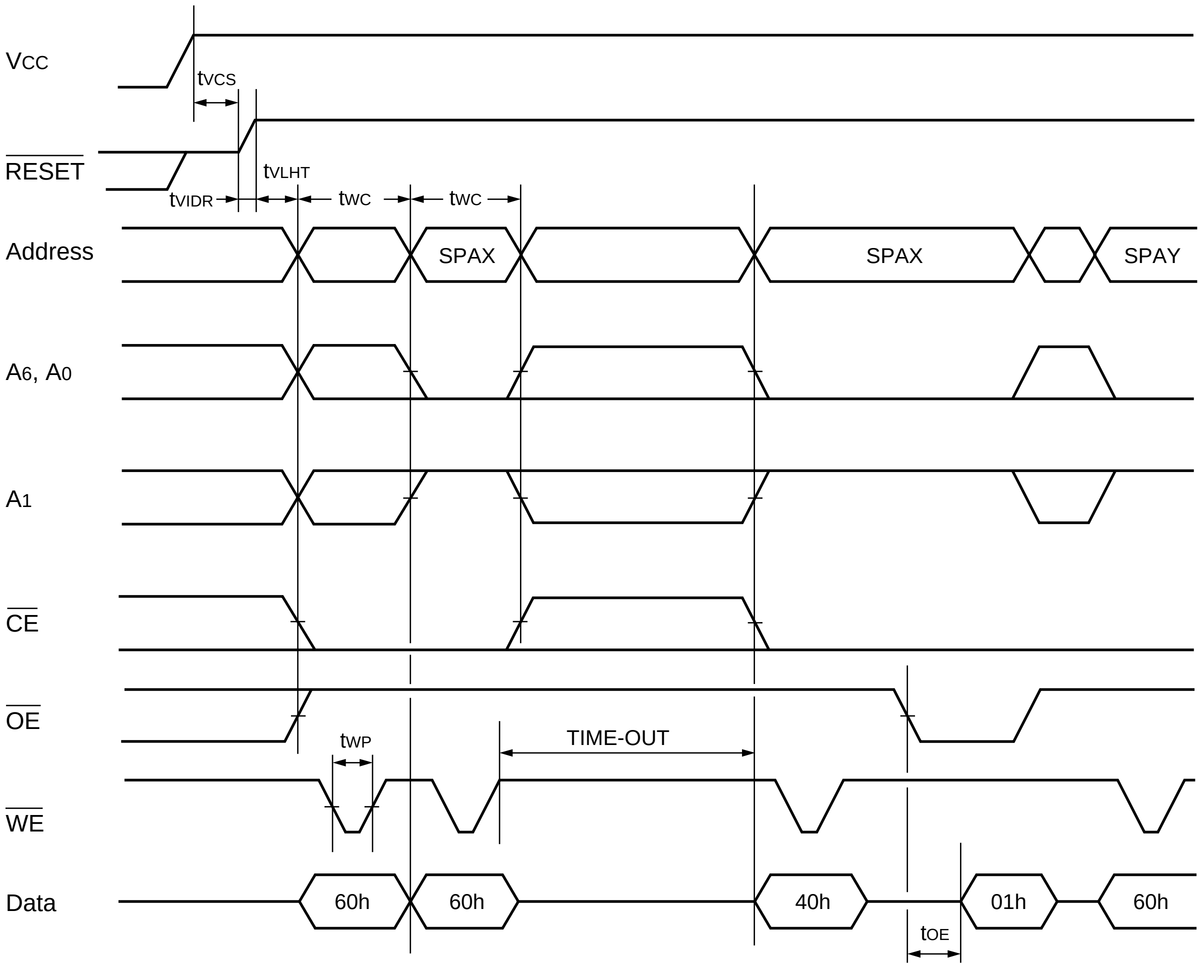


Figure 17　Temporary Sector Unprotection Timing Diagram



Note : DQ_2 is read from the erase-suspended sector.

Figure 18　DQ_2 vs. DQ_6



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 µs (Min.)

Figure 19 Extended Sector Protection Timing Diagram

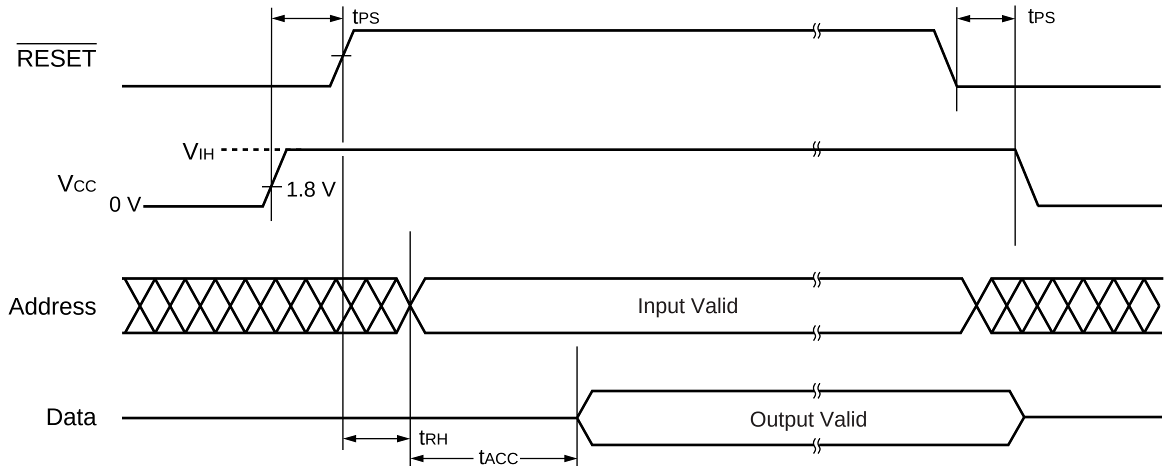
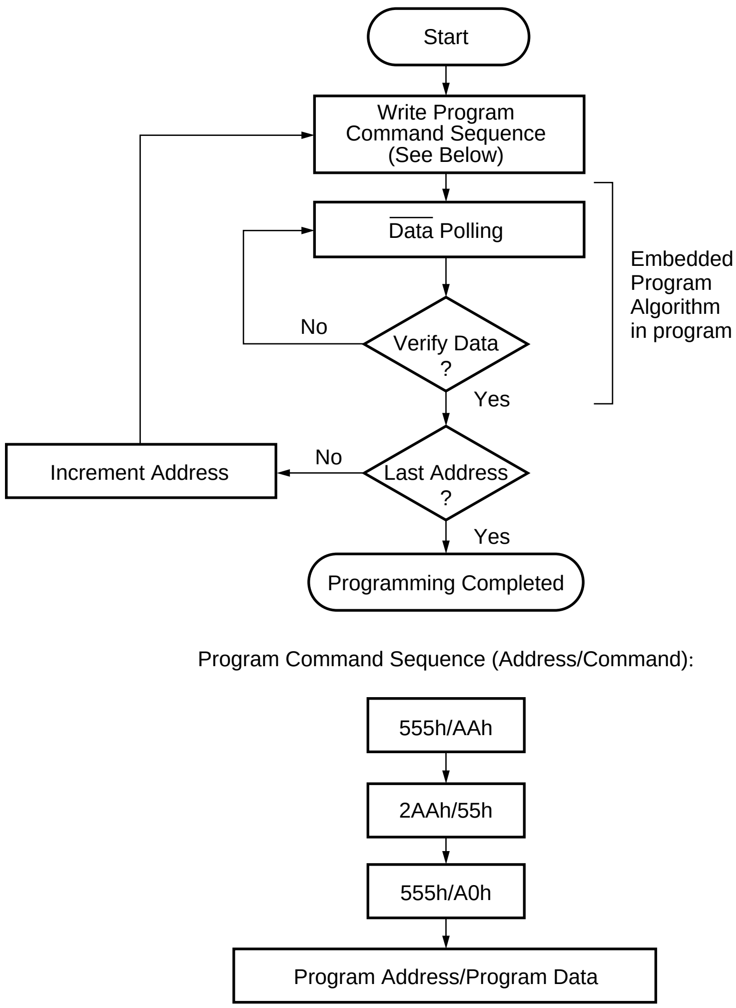


Figure 20 Power ON/OFF Timing Diagram

■ FLOW CHART

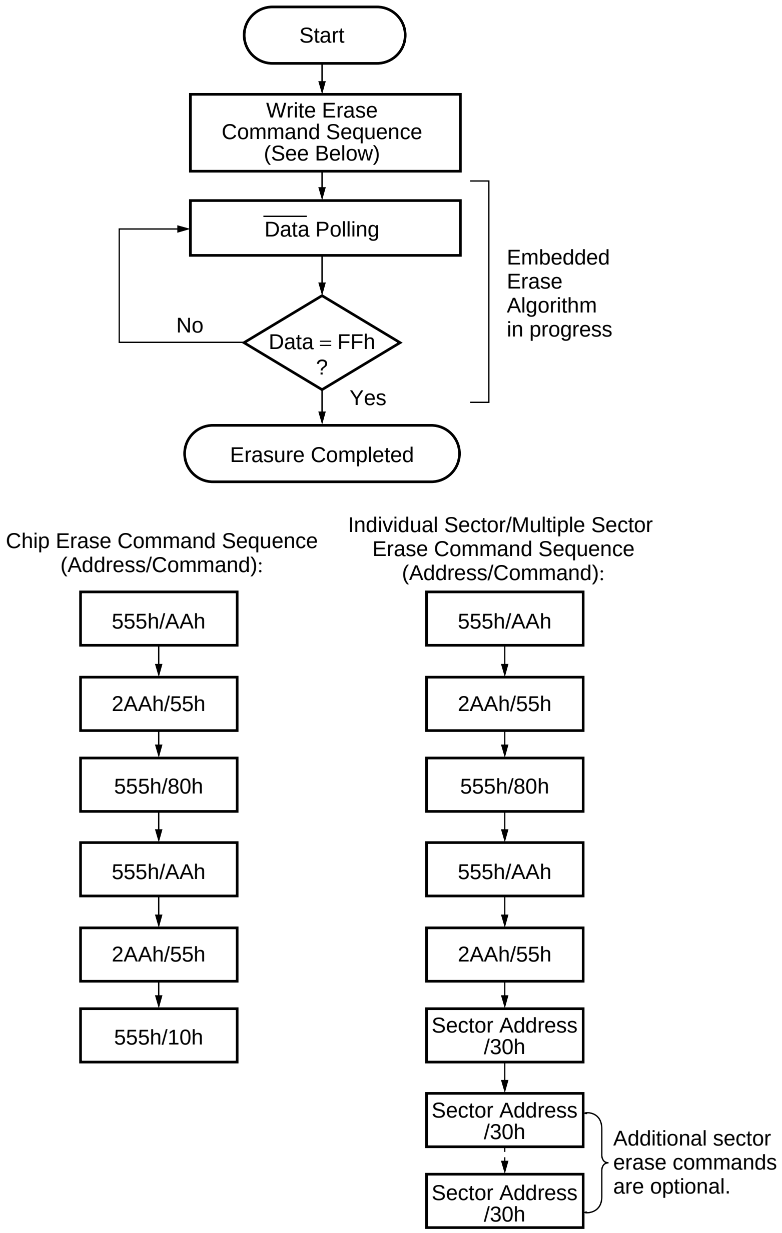
EMBEDDED ALGORITHM



Note : The sequence is applied for × 16 mode.
The addresses differ from × 8 mode.

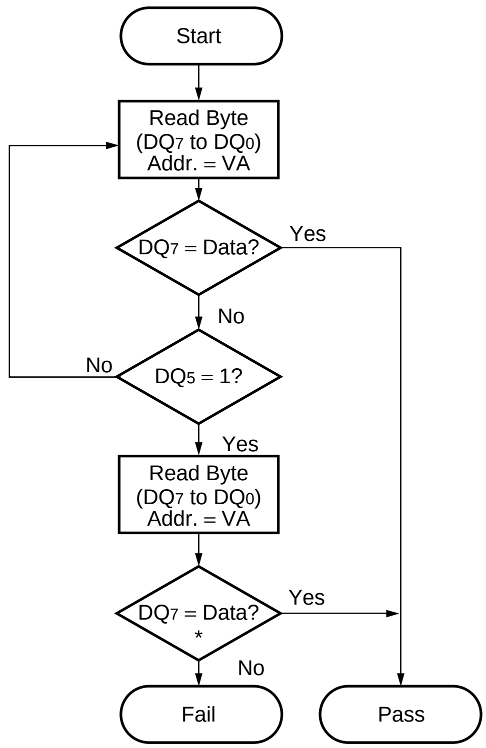
Figure 21 Embedded Program™ Algorithm

EMBEDDED ALGORITHM



Note : The sequence is applied for × 16 mode.
The addresses differ from × 8 mode.

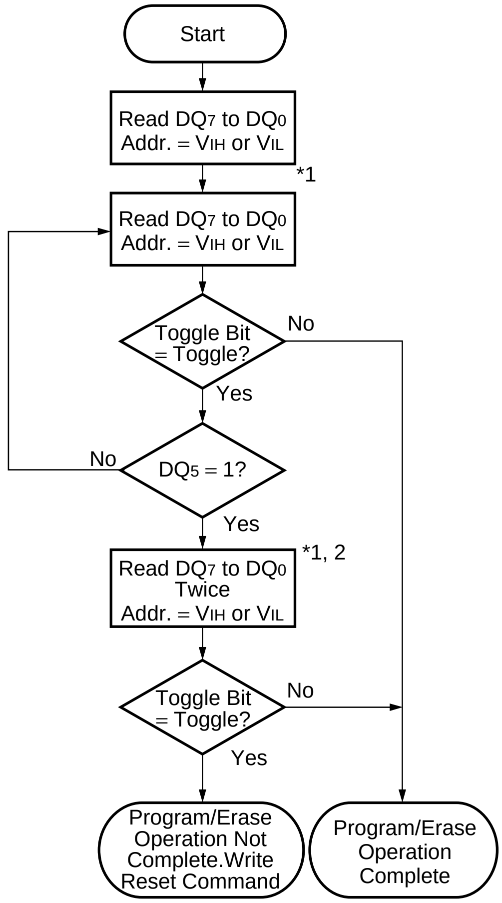
Figure 22 Embedded Erase™ Algorithm



VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

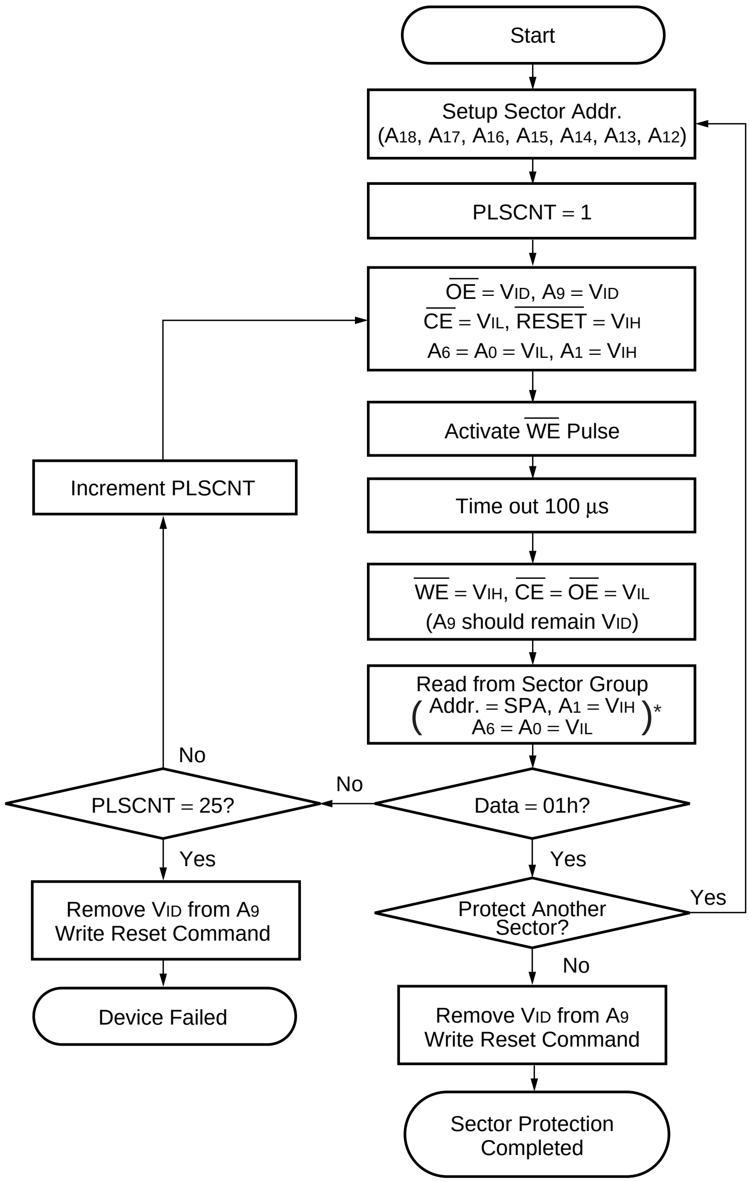
Figure 23 $\overline{\text{Data}}$ Polling Algorithm



*1 : Read toggle bit twice to determine whether or not it is toggling.

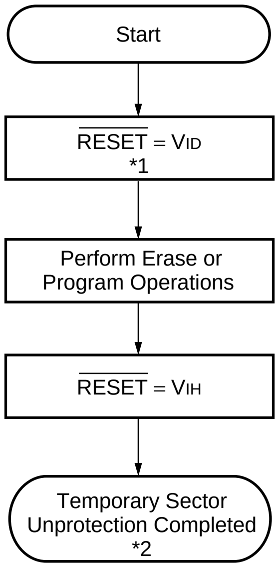
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to "1".

Figure 24　Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

Figure 25 Sector Protection Algorithm



*1 : All protected sectors are unprotected.

*2 : All previously protected sectors are protected once again.

Figure 26 Temporary Sector Unprotection Algorithm

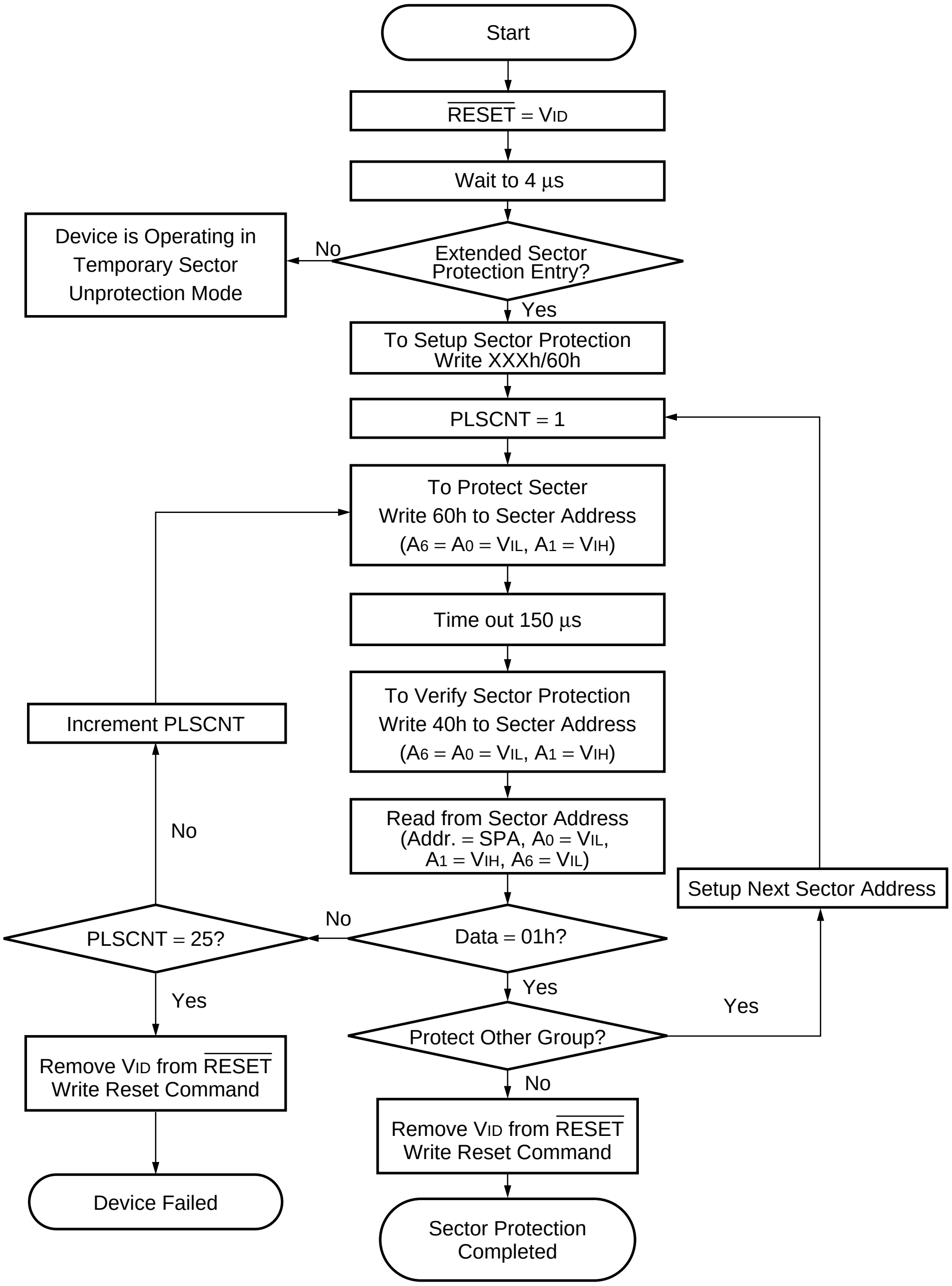
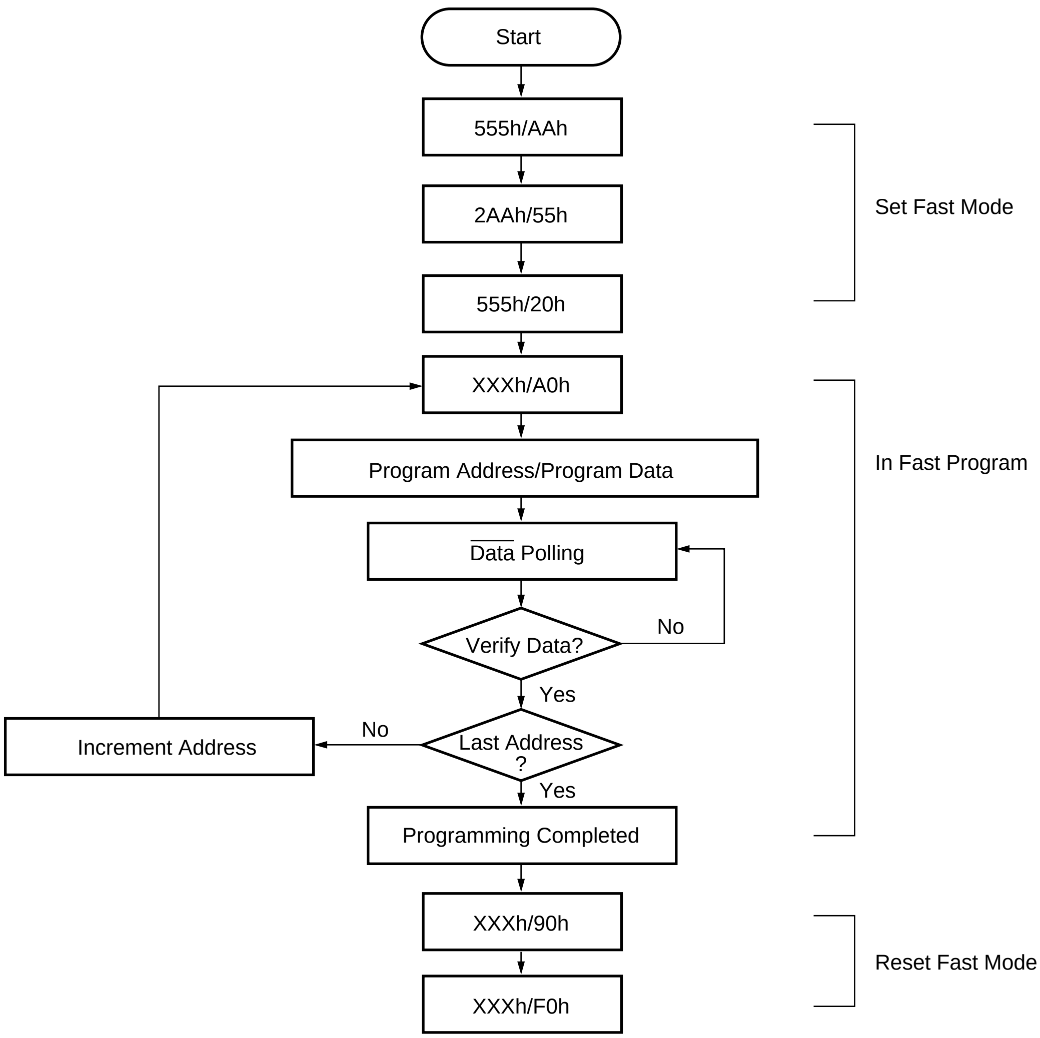


Figure 27　Extended Sector Protection Algorithm

FAST MODE ALGORITHM



Note : The sequence is applied for $\times$ 16 mode.
The addresses differ from $\times$ 8 mode.

Figure 28 Embedded Programming Algorithm for Fast Mode

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of :

MBM29SL800 T D – 10 TN

PACKAGE TYPE
TN = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout
TR = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout
PBT = 48-Ball Fine Pitch Ball Grid Array Package (FBGA)

SPEED OPTION
See Product Selector Guide

Device Revision

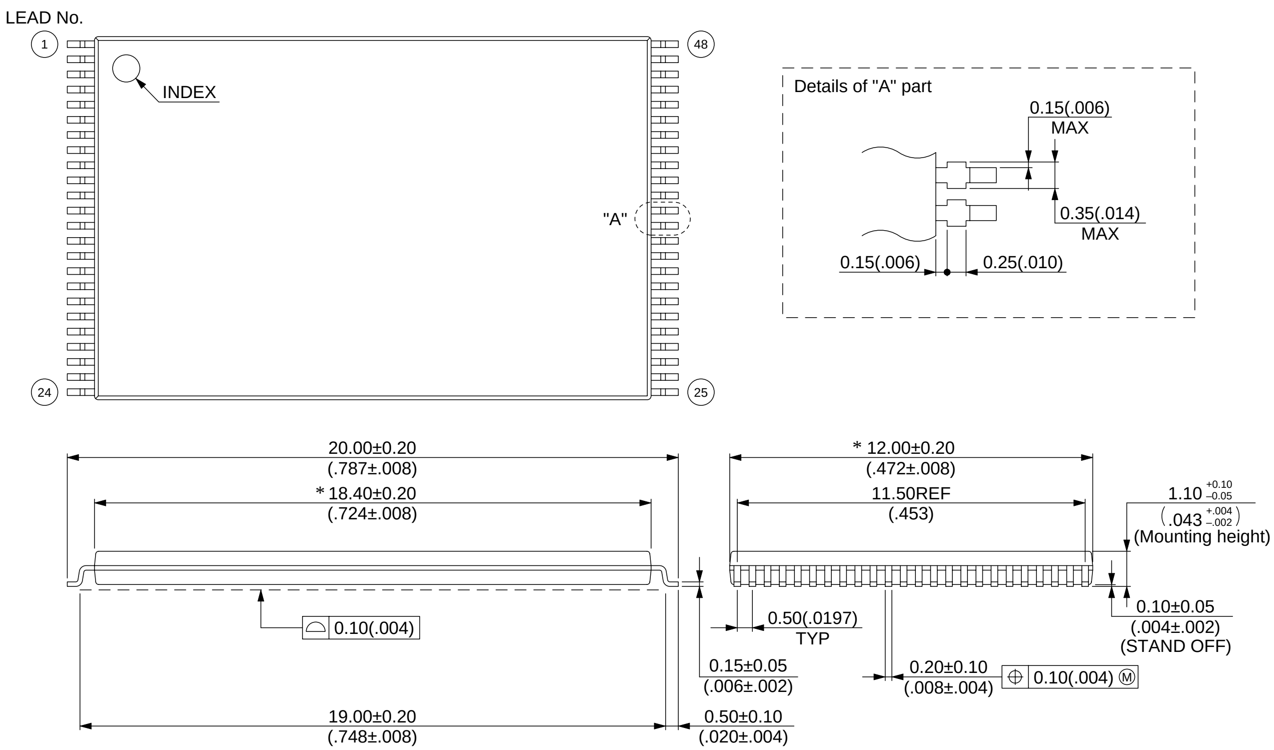
BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29SL800
8 Mega-bit (1 M × 8-Bit or 512 K × 16-Bit) CMOS Flash Memory
1.8 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP (I)
(FPT-48P-M19)

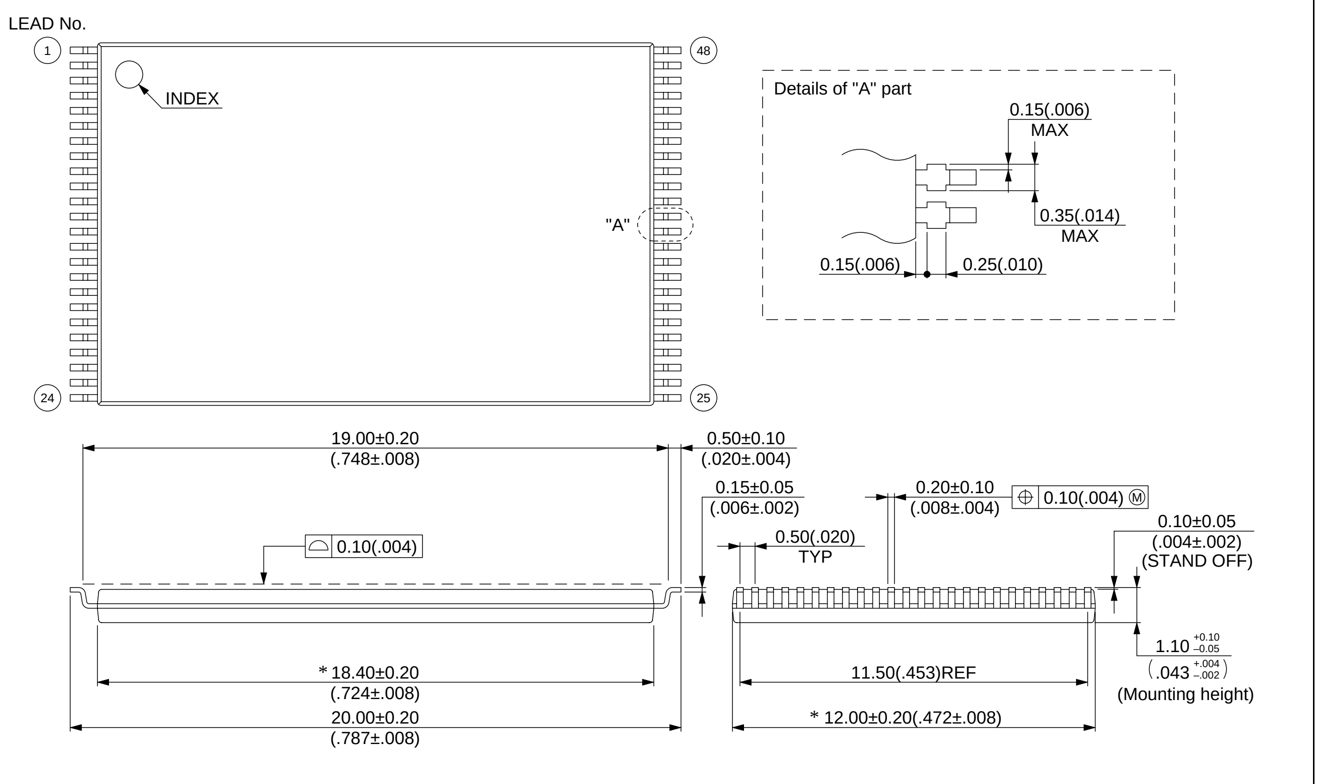
* Resin Protrusion. (Each Side : 0.15 (.006) Max)



© 2000 FUJITSU LIMITED F48029S-3c-4

Dimensions in mm (inches)

48-pin plastic TSOP (I)
(FPT-48P-M20)



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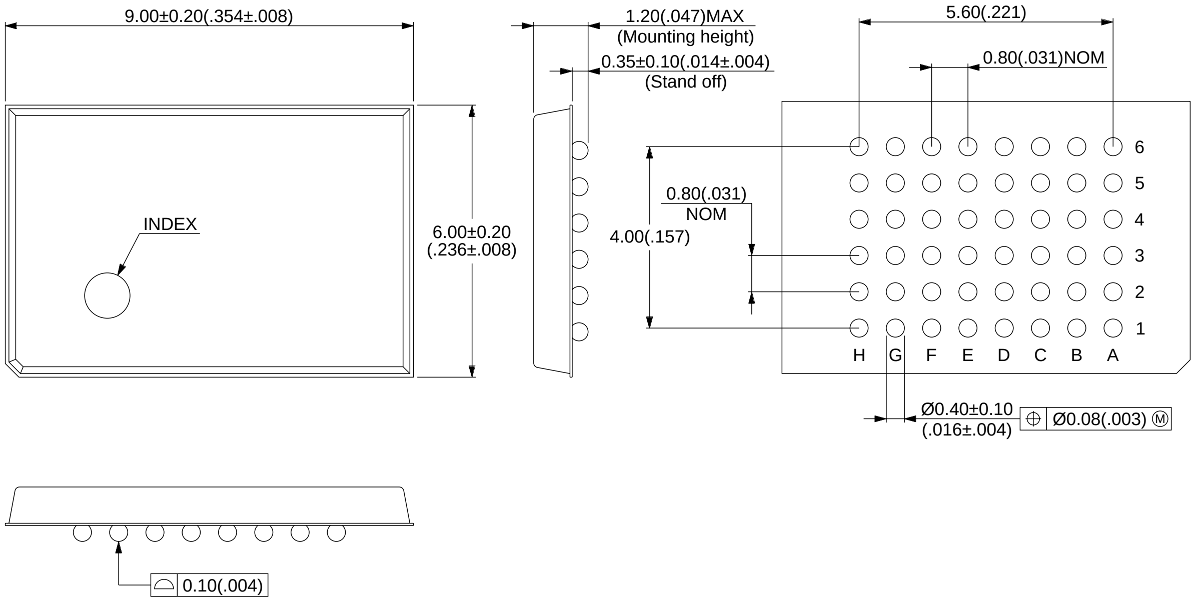
Dimensions in mm (inches)

48-ball plastic FBGA
(BGA-48P-M02)

Note : The actual shape of corners may differ from the dimension.



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Dimensions in mm (inches)

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