FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20889-1E

*FLASH MEMORY*

**CMOS**

# 32M (2M × 16) BIT Page Dual Operation

# MBM29PDS322TE/BE 10/11



## ■ DESCRIPTION

The MBM29PDS322TE/BE is 32M-bit, 1.8 V-only Flash memory organized as 2M words of 16 bits each. The device is offered in 63-ball FBGA package. This device is designed to be programmed in system with standard system 1.8 V $V_{CC}$ supply. 12.0 V $V_{PP}$ and 5.0 V $V_{CC}$ are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The device is organized into two banks, Bank 1 and Bank 2, which can be considered to be two separate memory arrays as far as certain operations are concerned. This device is the same as Fujitsu's standard 1.8 V only Flash memories with the additional capability of allowing a normal non-delayed read access from a non-busy bank of the array while an embedded write (either a program or an erase) operation is simultaneously taking place on the other bank.

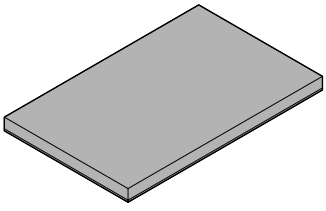
*(Continued)*

## ■ PRODUCT LINE-UP

| Part No. | | MBM29PDS322TE/BE | |
|---|---|---|---|
| Ordering Part No. | $V_{CC}$ = 2.0 V $^{+0.2\ V}_{-0.2\ V}$ | 10 | 11 |
| Max. Random Address Access Time (ns) | | 100 | 115 |
| Max. Page Address Access Time (ns) | | 45 | 45 |
| Max. $\overline{CE}$ Access Time (ns) | | 100 | 115 |
| Max. $\overline{OE}$ Access Time (ns) | | 35 | 45 |

## ■ PACKAGE

63-ball plastic FBGA



(BGA-63P-M01)

*(Continued)*

The device provides truly high performance non-volatile Flash memory solution. The device offers fast page access times of 45 ns with random access times of 100 ns and 115 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls. The page size is 4 words.

The device is pin and command set compatible with JEDEC standard $E^2$PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The device features single 1.8 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low $V_{CC}$ detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of $DQ_7$, by the Toggle Bit feature on $DQ_6$, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

The device also has a hardware $\overline{RESET}$ pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm is terminated. The internal state machine is then reset to the read mode. The $\overline{RESET}$ pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device is automatically reset to the read mode and will have erroneous data stored in the address locations being programmed or erased. These locations need re-writing after the Reset. Resetting the device enables the system's microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of EPROM and $E^2$PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

## ■ FEATURES

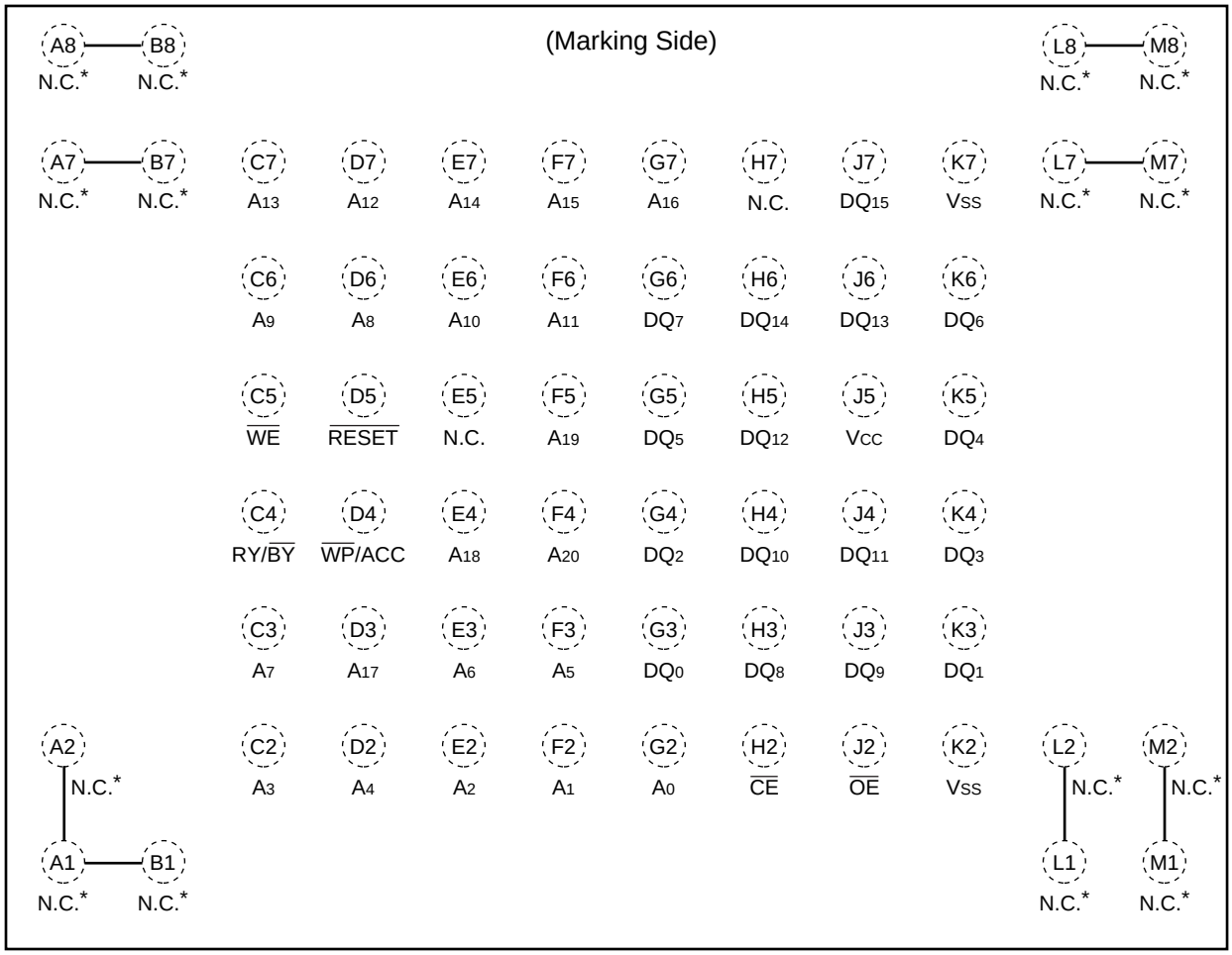
- **0.23 μm Process Technology**
- **Simultaneous Read/Write operations (Dual Bank)**
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.
  Read-while-erase
  Read-while-program
- **High performance Page Mode**
  45 ns maximum page access time (100 ns random access time)
  4 words Page Size
- **Single 1.8 V read, program, and erase**
  Minimized system level power requirements
- **Compatible with JEDEC-standard commands**
  Use the same software commands as $E^2$PROMs.
- **Compatible with JEDEC-standard world-wide pinouts**
  63-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **Sector erase architecture**
  Eight 4 Kword and sixty-three 32 Kword sectors in word mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Hidden ROM (Hi-ROM) region**
  64 Kbyte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC input pin**
  At $V_{IL}$, allows protection of boot sectors, regardless of sector protection/unprotection status.
  At $V_{IH}$, allows removal of boot sector protection.
  At $V_{ACC}$, increases program performance.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector.
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address.
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device.
- **Sector group protection**
  Hardware method disables any combination of sector groups from program or erase operations.
- **Sector Group Protection Set function by Extended sector group protection command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
  Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin.

**Table 1: MBM29PDS322TE/BE Device Bank Division**

| Device Part Number | Organization | Bank 1 | | Bank 2 | |
|---|---|---|---|---|---|
| | | Megabits | Sector Sizes | Megabits | Sector Sizes |
| MBM29PDS322TE/BE | × 16 | 4 Mbit | Eight 4 Kword, seven 32 Kword | 28 Mbit | Fifty-six 32 Kword |

## ■ PIN ASSIGNMENT

(TOP VIEW)




(BGA-63P-M01)

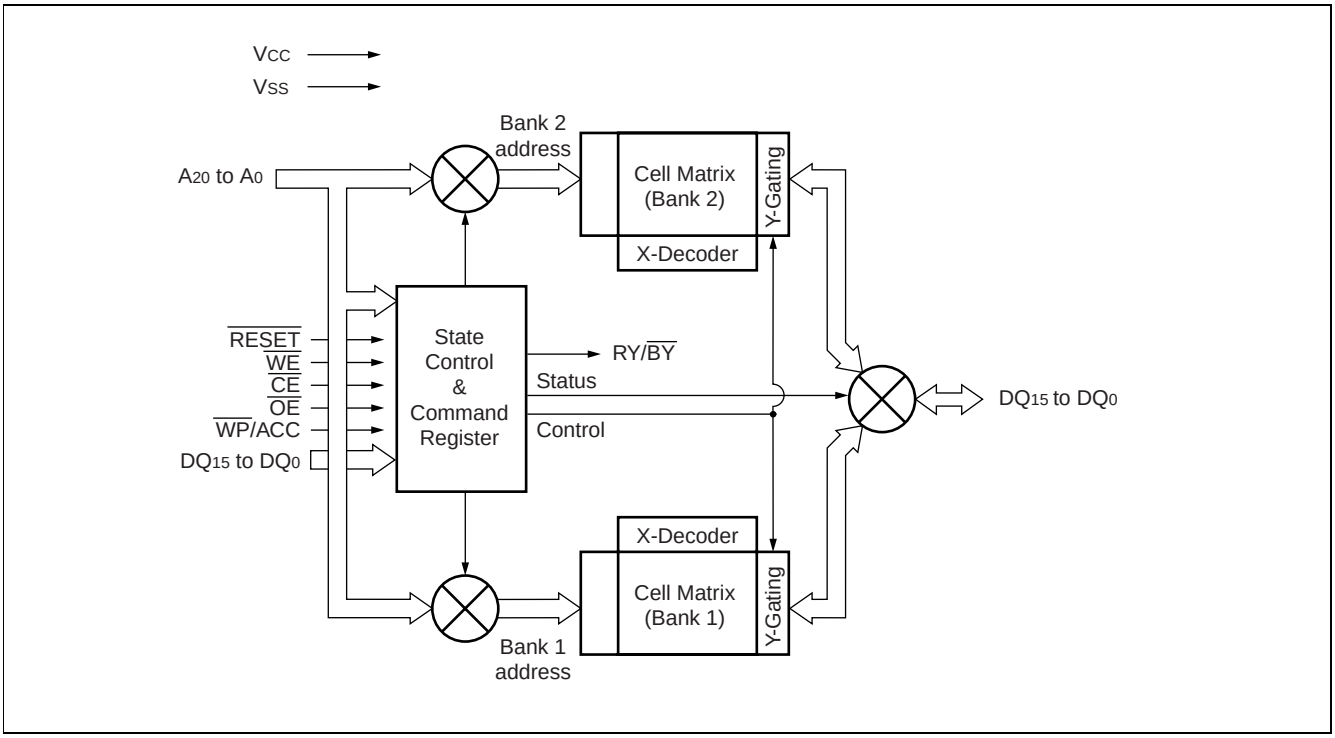
*: Peripheral balls on each corner are shorted together via the substrate but not connected to the die.

## ■ PIN DESCRIPTION

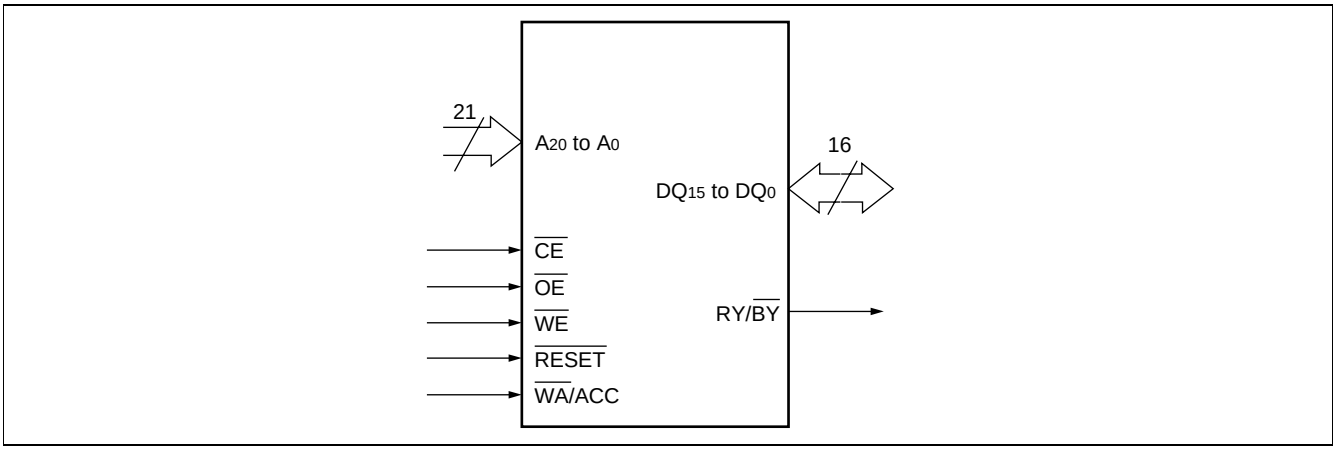
**Table 2: MBM29PDS322TE/BE Pin Configuration**

| Pin name | Function |
|---|---|
| $A_{20}$ to $A_0$ | Address Inputs |
| $DQ_{15}$ to $DQ_0$ | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| RY/$\overline{BY}$ | Ready/Busy Output |
| $\overline{RESET}$ | Hardware Reset Pin/Temporary Sector Group Unprotection |
| $\overline{WP}$/ACC | Hardware Write Protection/Program Acceleration |
| N.C. | No Internal Connection |
| $V_{SS}$ | Device Ground |
| $V_{CC}$ | Device Power Supply |

## ■ BLOCK DIAGRAM




## ■ LOGIC SYMBOL



## ■ DEVICE BUS OPERATION

**Table 3: MBM29PDS322TE/BE User Bus Operations**

| Operation | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_6$ | $A_9$ | $DQ_{15}$ to $DQ_0$ | RESET | $\overline{WP}$/ ACC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Auto-Select Manufacturer Code *1 | L | L | H | L | L | L | L | L | $V_{ID}$ | Code | H | X |
| Auto-Select Device Code *1 | L | L | H | H | L | L | L | L | $V_{ID}$ | Code | H | X |
| Extended Auto-Select Device Code *1 | L | L | H | L/H | H | H | H | L | $V_{ID}$ | Code | H | X |
| Read *3 | L | L | H | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_6$ | $A_9$ | $D_{OUT}$ | H | X |
| Standby | H | X | X | X | X | X | X | X | X | High-Z | H | X |
| Output Disable | L | H | H | X | X | X | X | X | X | High-Z | H | X |
| Write (Program/Erase) | L | H | L | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_6$ | $A_9$ | $D_{IN}$ | H | X |
| Enable Sector Group Protection *2, *4 | L | $V_{ID}$ | ⎍ | L | H | L | L | L | $V_{ID}$ | X | H | X |
| Verify Sector Group Protection *2, *4 | L | L | H | L | H | L | L | L | $V_{ID}$ | Code | H | X |
| Temporary Sector Group Unprotection *5 | X | X | X | X | X | X | X | X | X | X | $V_{ID}$ | X |
| Reset (Hardware) / Standby | X | X | X | X | X | X | X | X | X | High-Z | L | X |
| Boot Block Sector Write Protection *6 | X | X | X | X | X | X | X | X | X | X | X | L |

Legend: L = $V_{IL}$, H = $V_{IH}$, X = $V_{IL}$ or $V_{IH}$, ⎍ = Pulse input. See DC Characteristics for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See Table 3.

*2: Refer to section on Sector Group Protection.

*3: $\overline{WE}$ can be $V_{IL}$ if $\overline{OE}$ is $V_{IL}$, $\overline{OE}$ at $V_{IH}$ initiates the write operations.

*4: $V_{CC}$ must be between the minimum and maximum of the operation range.

*5: It is also used for the extended sector group protection.

*6: Protect “outermost” 2 × 4 Kwords of the boot block sectors.

**Table 4: MBM29PDS322TE/BE Command Definitions**

| Command Sequence | | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/Reset | Word | 1 | XXXh | F0h | — | — | — | — | — | — | — | — | — | — |
| Read/Reset | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | F0h | RA | RD | — | — | — | — |
| Auto select | Word | 3 | 555h | AAh | 2AAh | 55h | (BA) 555h | 90h | — | — | — | — | — | — |
| Program | Word | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | PA | PD | — | — | — | — |
| Chip Erase | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | 555h | 10h |
| Sector Erase | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | SA | 30h |
| Erase Suspend | | 1 | BA | B0h | — | — | — | — | — | — | — | — | — | — |
| Erase Resume | | 1 | BA | 30h | — | — | — | — | — | — | — | — | — | — |
| Set to Fast Mode | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | 20h | — | — | — | — | — | — |
| Fast Program *1 | Word | 2 | XXXh | A0h | PA | PD | — | — | — | — | — | — | — | — |
| Reset from Fast Mode *1 | Word | 2 | BA | 90h | XXXh | *4 F0h | — | — | — | — | — | — | — | — |
| Extended Sector Group Protection *2 | Word | 4 | XXXh | 60h | SPA | 60h | SPA | 40h | SPA | SD | — | — | — | — |
| Query | Word | 1 | (BA) 55h | 98h | — | — | — | — | — | — | — | — | — | — |
| Hi-ROM Entry | Word | 3 | 555h | AAh | 2AAh | 55h | 555h | 88h | — | — | — | — | — | — |
| Hi-ROM Program *3 | Word | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | (HRA) PA | PD | — | — | — | — |
| Hi-ROM Erase *3 | Word | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | HRA | 30h |
| Hi-ROM Exit *3 | Word | 4 | 555h | AAh | 2AAh | 55h | (HRBA) 555h | 90h | XXXh | 00h | — | — | — | — |

*1: This command is valid while Fast Mode.

*2: This command is valid while $\overline{RESET} = V_{ID}$.

*3: This command is valid while Hi-ROM mode.

*4: The data "00h" is also acceptable.

Note 1.Address bits $A_{20}$ to $A_{12}$ = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA).
2.Bus operations are defined in Table 8.
3.RA = Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of $A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$, and $A_{12}$ will uniquely select any sector.
BA = Bank Address ($A_{20}$ to $A_{15}$)

4.RD = Data read from location RA during the read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.

5.SPA = Sector group address to be protected. Set sector group address (SGA) and ($A_6$, $A_1$, $A_0$) = (0, 1, 0).
SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

6.HRA = Address of the Hi-ROM area
29PDS322TE (Top Boot Type)Word Mode:1F8000h to 1FFFFFh
29PDS322BE (Bottom Boot Type)Word Mode:000000h to 007FFFh

7.HRBA =Bank Address of the Hi-ROM area
29PDS322TE (Top Boot Type):$A_{20} = A_{19} = A_{18} = A_{17} = A_{16} = A_{15} = 1$
29PDS322BE (Bottom Boot Type):$A_{20} = A_{19} = A_{18} = A_{17} = A_{16} = A_{15} = 0$

8.The system should generate the following address patterns:
Word Mode: 555h or 2AAh to addresses $A_{10}$ to $A_0$

9.Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

**Table 5.1 MBM29PDS322TE Sector Group Protection Verify Autoselect Codes**

| Type | | $A_{20}$ to $A_{12}$ | $A_6$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Code (HEX) |
|---|---|---|---|---|---|---|---|---|
| Manufacture's Code | | BA*2 | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 04h |
| Device Code | Word | BA*2 | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 227Eh |
| Extended Device Code *3 | Word | BA*2 | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | 2206h |
| | Word | BA*2 | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | 2201h |
| Sector Group Protection | | Sector Group Addresses | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 01h*1 |

*1:Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2:When $V_{ID}$ is applied, both Bank 1 and Bank 2 become Autoselect mode, which leads to the simultaneous operation unable to be executed. Consequently, specifying the bank address is not demanded. However, the bank address needs to be indicated when Autoselect mode is read out at command mode; because then it becomes OK to activate simultaneous operation.

*3:A read cycle at address (BA)01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore, the system may continue reading out these Extended Device Codes at the address of (BA)0Eh, as well as at (BA)0Fh.

**Table 5.2 Expanded Autoselect Code Table**

| Type | | Code | $DQ_{15}$ | $DQ_{14}$ | $DQ_{13}$ | $DQ_{12}$ | $DQ_{11}$ | $DQ_{10}$ | $DQ_9$ | $DQ_8$ | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_4$ | $DQ_3$ | $DQ_2$ | $DQ_1$ | $DQ_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | 04h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Device Code | (W) | 227Eh | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Extended Device Code | (W) | 2206h | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | (W) | 2201h | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Sector Group Protection | | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

(W): Word mode

**Table 5.3 MBM29PDS322BE Sector Group Protection Verify Autoselect Codes**

| Type | | $A_{20}$ to $A_{12}$ | $A_6$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Code (HEX) |
|---|---|---|---|---|---|---|---|---|
| Manufacture's Code | | BA*2 | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 04h |
| Device Code | Word | BA*2 | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 227Eh |
| Extended Device Code *3 | Word | BA*2 | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | 2206h |
| | Word | BA*2 | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | 2200h |
| Sector Group Protection | | Sector Group Addresses | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | 01h*1 |

*1:Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2:When $V_{ID}$ is applied, both Bank 1 and Bank 2 become Autoselect mode, which leads to the simultaneous operation unable to be executed. Consequently, specifying the bank address is not demanded. However, the bank address needs to be indicated when Autoselect mode is read out at command mode; because then it becomes OK to activate simultaneous operation.

* 3:A read cycle at address (BA)01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore, the system may continue reading out these Extended Device Codes at the address of (BA)0Eh, as well as at (BA)0Fh.

**Table 5.4 Expanded Autoselect Code Table**

| Type | | Code | $DQ_{15}$ | $DQ_{14}$ | $DQ_{13}$ | $DQ_{12}$ | $DQ_{11}$ | $DQ_{10}$ | $DQ_9$ | $DQ_8$ | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_4$ | $DQ_3$ | $DQ_2$ | $DQ_1$ | $DQ_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | | 04h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Device Code | (W) | 227Eh | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Extended Device Code | (W) | 2206h | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | (W) | 2200h | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sector Group Protection | | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

(W): Word mode

## ■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

**Table 6.1 Sector Address Tables (MBM29PDS322TE)**

| Bank | Sector | Sector Address | | | | | | | | | Sector Size (Kwords) | (×16) Address Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bank Address | | | | | | $A_{14}$ | $A_{13}$ | $A_{12}$ | | |
| | | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | | | | | |
| Bank 2 | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 32 | 000000h to 007FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 32 | 008000h to 00FFFFh |
| | SA2 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | 32 | 010000h to 017FFFh |
| | SA3 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | 32 | 018000h to 01FFFFh |
| | SA4 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | 32 | 020000h to 027FFFh |
| | SA5 | 0 | 0 | 0 | 1 | 0 | 1 | X | X | X | 32 | 028000h to 02FFFFh |
| | SA6 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 32 | 030000h to 037FFFh |
| | SA7 | 0 | 0 | 0 | 1 | 1 | 1 | X | X | X | 32 | 038000h to 03FFFFh |
| | SA8 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | 32 | 040000h to 047FFFh |
| | SA9 | 0 | 0 | 1 | 0 | 0 | 1 | X | X | X | 32 | 048000h to 04FFFFh |
| | SA10 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | X | 32 | 050000h to 057FFFh |
| | SA11 | 0 | 0 | 1 | 0 | 1 | 1 | X | X | X | 32 | 058000h to 05FFFFh |
| | SA12 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | 32 | 060000h to 067FFFh |
| | SA13 | 0 | 0 | 1 | 1 | 0 | 1 | X | X | X | 32 | 068000h to 06FFFFh |
| | SA14 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 32 | 070000h to 077FFFh |
| | SA15 | 0 | 0 | 1 | 1 | 1 | 1 | X | X | X | 32 | 078000h to 07FFFFh |
| | SA16 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 32 | 080000h to 087FFFh |
| | SA17 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | 32 | 088000h to 08FFFFh |
| | SA18 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | 32 | 090000h to 097FFFh |
| | SA19 | 0 | 1 | 0 | 0 | 1 | 1 | X | X | X | 32 | 098000h to 09FFFFh |
| | SA20 | 0 | 1 | 0 | 1 | 0 | 0 | X | X | X | 32 | 0A0000h to 0A7FFFh |
| | SA21 | 0 | 1 | 0 | 1 | 0 | 1 | X | X | X | 32 | 0A8000h to 0AFFFFh |
| | SA22 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | X | 32 | 0B0000h to 0B7FFFh |
| | SA23 | 0 | 1 | 0 | 1 | 1 | 1 | X | X | X | 32 | 0B8000h to 0BFFFFh |
| | SA24 | 0 | 1 | 1 | 0 | 0 | 0 | X | X | X | 32 | 0C0000h to 0C7FFFh |
| | SA25 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X | 32 | 0C8000h to 0CFFFFh |
| | SA26 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | 32 | 0D0000h to 0D7FFFh |
| | SA27 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | X | 32 | 0D8000h to 0DFFFFh |
| | SA28 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | 32 | 0E0000h to 0E7FFFh |
| | SA29 | 0 | 1 | 1 | 1 | 0 | 1 | X | X | X | 32 | 0E8000h to 0EFFFFh |
| | SA30 | 0 | 1 | 1 | 1 | 1 | 0 | X | X | X | 32 | 0F0000h to 0F7FFFh |
| | SA31 | 0 | 1 | 1 | 1 | 1 | 1 | X | X | X | 32 | 0F8000h to 0FFFFFh |
| | SA32 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | 32 | 100000h to 107FFFh |
| | SA33 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 32 | 108000h to 10FFFFh |
| | SA34 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | 32 | 110000h to 117FFFh |

*(Continued)*

*(Continued)*

| Bank | Sector | Sector Address | | | | | | | | | Sector Size (Kwords) | (×16) Address Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bank Address | | | | | | $A_{14}$ | $A_{13}$ | $A_{12}$ | | |
| | | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | | | | | |
| Bank 2 | SA35 | 1 | 0 | 0 | 0 | 1 | 1 | X | X | X | 32 | 118000h to 11FFFFh |
| | SA36 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | 32 | 120000h to 127FFFh |
| | SA37 | 1 | 0 | 0 | 1 | 0 | 1 | X | X | X | 32 | 128000h to 12FFFFh |
| | SA38 | 1 | 0 | 0 | 1 | 1 | 0 | X | X | X | 32 | 130000h to 137FFFh |
| | SA39 | 1 | 0 | 0 | 1 | 1 | 1 | X | X | X | 32 | 138000h to 13FFFFh |
| | SA40 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | 32 | 140000h to 147FFFh |
| | SA41 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | 32 | 148000h to 14FFFFh |
| | SA42 | 1 | 0 | 1 | 0 | 1 | 0 | X | X | X | 32 | 150000h to 157FFFh |
| | SA43 | 1 | 0 | 1 | 0 | 1 | 1 | X | X | X | 32 | 158000h to 15FFFFh |
| | SA44 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | 32 | 160000h to 167FFFh |
| | SA45 | 1 | 0 | 1 | 1 | 0 | 1 | X | X | X | 32 | 168000h to 16FFFFh |
| | SA46 | 1 | 0 | 1 | 1 | 1 | 0 | X | X | X | 32 | 170000h to 177FFFh |
| | SA47 | 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | 32 | 178000h to 17FFFFh |
| | SA48 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | 32 | 180000h to 187FFFh |
| | SA49 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | 32 | 188000h to 18FFFFh |
| | SA50 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | 32 | 190000h to 197FFFh |
| | SA51 | 1 | 1 | 0 | 0 | 1 | 1 | X | X | X | 32 | 198000h to 19FFFFh |
| | SA52 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | 32 | 1A0000h to 1A7FFFh |
| | SA53 | 1 | 1 | 0 | 1 | 0 | 1 | X | X | X | 32 | 1A8000h to 1AFFFFh |
| | SA54 | 1 | 1 | 0 | 1 | 1 | 0 | X | X | X | 32 | 1B0000h to 1B7FFFh |
| | SA55 | 1 | 1 | 0 | 1 | 1 | 1 | X | X | X | 32 | 1B8000h to 1BFFFFh |
| Bank 1 | SA56 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 32 | 1C0000h to 1C7FFFh |
| | SA57 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | X | 32 | 1C8000h to 1CFFFFh |
| | SA58 | 1 | 1 | 1 | 0 | 1 | 0 | X | X | X | 32 | 1D0000h to 1D7FFFh |
| | SA59 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X | 32 | 1D8000h to 1DFFFFh |
| | SA60 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | 32 | 1E0000h to 1E7FFFh |
| | SA61 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | X | 32 | 1E8000h to 1EFFFFh |
| | SA62 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | X | 32 | 1F0000h to 1F7FFFh |
| | SA63 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 4 | 1F8000h to 1F8FFFh |
| | SA64 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 4 | 1F9000h to 1F9FFFh |
| | SA65 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 4 | 1FA000h to 1FAFFFh |
| | SA66 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 4 | 1FB000h to 1FBFFFh |
| | SA67 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 4 | 1FC000h to 1FCFFFh |
| | SA68 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 4 | 1FD000h to 1FDFFFh |
| | SA69 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 4 | 1FE000h to 1FEFFFh |
| | SA70 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 1FF000h to 1FFFFFh |

**MBM29PDS322TE Top Boot Sector Architecture**

**Table 6.2 Sector Address Tables (MBM29PDS322BE)**

| Bank | Sector | Sector Address | | | | | | | | | Sector Size (Kwords) | (×16) Address Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bank Address | | | | | | $A_{14}$ | $A_{13}$ | $A_{12}$ | | |
| | | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | | | | | |
| Bank 2 | SA70 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X | 32 | 1F8000h to 1FFFFFh |
| | SA69 | 1 | 1 | 1 | 1 | 1 | 0 | X | X | X | 32 | 1F0000h to 1F7FFFh |
| | SA68 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | X | 32 | 1E8000h to 1EFFFFh |
| | SA67 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | 32 | 1E0000h to 1E7FFFh |
| | SA66 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X | 32 | 1D8000h to 1DFFFFh |
| | SA65 | 1 | 1 | 1 | 0 | 1 | 0 | X | X | X | 32 | 1D0000h to 1D7FFFh |
| | SA64 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | X | 32 | 1C8000h to 1CFFFFh |
| | SA63 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 32 | 1C0000h to 1C7FFFh |
| | SA62 | 1 | 1 | 0 | 1 | 1 | 1 | X | X | X | 32 | 1B8000h to 1BFFFFh |
| | SA61 | 1 | 1 | 0 | 1 | 1 | 0 | X | X | X | 32 | 1B0000h to 1B7FFFh |
| | SA60 | 1 | 1 | 0 | 1 | 0 | 1 | X | X | X | 32 | 1A8000h to 1AFFFFh |
| | SA59 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | 32 | 1A0000h to 1A7FFFh |
| | SA58 | 1 | 1 | 0 | 0 | 1 | 1 | X | X | X | 32 | 198000h to 19FFFFh |
| | SA57 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | 32 | 190000h to 197FFFh |
| | SA56 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | 32 | 188000h to 18FFFFh |
| | SA55 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | 32 | 180000h to 187FFFh |
| | SA54 | 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | 32 | 178000h to 17FFFFh |
| | SA53 | 1 | 0 | 1 | 1 | 1 | 0 | X | X | X | 32 | 170000h to 177FFFh |
| | SA52 | 1 | 0 | 1 | 1 | 0 | 1 | X | X | X | 32 | 168000h to 16FFFFh |
| | SA51 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | 32 | 160000h to 167FFFh |
| | SA50 | 1 | 0 | 1 | 0 | 1 | 1 | X | X | X | 32 | 158000h to 15FFFFh |
| | SA49 | 1 | 0 | 1 | 0 | 1 | 0 | X | X | X | 32 | 150000h to 157FFFh |
| | SA48 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | 32 | 148000h to 14FFFFh |
| | SA47 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | 32 | 140000h to 147FFFh |
| | SA46 | 1 | 0 | 0 | 1 | 1 | 1 | X | X | X | 32 | 138000h to 13FFFFh |
| | SA45 | 1 | 0 | 0 | 1 | 1 | 0 | X | X | X | 32 | 130000h to 137FFFh |
| | SA44 | 1 | 0 | 0 | 1 | 0 | 1 | X | X | X | 32 | 128000h to 12FFFFh |
| | SA43 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | 32 | 120000h to 127FFFh |
| | SA42 | 1 | 0 | 0 | 0 | 1 | 1 | X | X | X | 32 | 118000h to 11FFFFh |
| | SA41 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | 32 | 110000h to 117FFFh |
| | SA40 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 32 | 108000h to 10FFFFh |
| | SA39 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | 32 | 100000h to 107FFFh |
| | SA38 | 0 | 1 | 1 | 1 | 1 | 1 | X | X | X | 32 | 0F8000h to 0FFFFFh |
| | SA37 | 0 | 1 | 1 | 1 | 1 | 0 | X | X | X | 32 | 0F0000h to 0F7FFFh |
| | SA36 | 0 | 1 | 1 | 1 | 0 | 1 | X | X | X | 32 | 0E8000h to 0EFFFFh |
| | SA35 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | 32 | 0E0000h to 0E7FFFh |

*(Continued)*

*(Continued)*

| Bank | Sector | Sector Address | | | | | | | | | Sector Size (Kwords) | (×16) Address Range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bank Address | | | | | | $A_{14}$ | $A_{13}$ | $A_{12}$ | | |
| | | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | | | | | |
| Bank 2 | SA34 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | X | 32 | 0D8000h to 0DFFFFh |
| | SA33 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | 32 | 0D0000h to 0D7FFFh |
| | SA32 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X | 32 | 0C8000h to 0CFFFFh |
| | SA31 | 0 | 1 | 1 | 0 | 0 | 0 | X | X | X | 32 | 0C0000h to 0C7FFFh |
| | SA30 | 0 | 1 | 0 | 1 | 1 | 1 | X | X | X | 32 | 0B8000h to 0BFFFFh |
| | SA29 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | X | 32 | 0B0000h to 0B7FFFh |
| | SA28 | 0 | 1 | 0 | 1 | 0 | 1 | X | X | X | 32 | 0A8000h to 0AFFFFh |
| | SA27 | 0 | 1 | 0 | 1 | 0 | 0 | X | X | X | 32 | 0A0000h to 0A7FFFh |
| | SA26 | 0 | 1 | 0 | 0 | 1 | 1 | X | X | X | 32 | 098000h to 09FFFFh |
| | SA25 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | 32 | 090000h to 097FFFh |
| | SA24 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | 32 | 088000h to 08FFFFh |
| | SA23 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 32 | 080000h to 087FFFh |
| | SA22 | 0 | 0 | 1 | 1 | 1 | 1 | X | X | X | 32 | 078000h to 07FFFFh |
| | SA21 | 0 | 0 | 1 | 1 | 1 | 0 | X | X | X | 32 | 070000h to 077FFFh |
| | SA20 | 0 | 0 | 1 | 1 | 0 | 1 | X | X | X | 32 | 068000h to 06FFFFh |
| | SA19 | 0 | 0 | 1 | 1 | 0 | 0 | X | X | X | 32 | 060000h to 067FFFh |
| | SA18 | 0 | 0 | 1 | 0 | 1 | 1 | X | X | X | 32 | 058000h to 05FFFFh |
| | SA17 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | X | 32 | 050000h to 057FFFh |
| | SA16 | 0 | 0 | 1 | 0 | 0 | 1 | X | X | X | 32 | 048000h to 04FFFFh |
| | SA15 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | 32 | 040000h to 047FFFh |
| Bank 1 | SA14 | 0 | 0 | 0 | 1 | 1 | 1 | X | X | X | 32 | 038000h to 03FFFFh |
| | SA13 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | 32 | 030000h to 037FFFh |
| | SA12 | 0 | 0 | 0 | 1 | 0 | 1 | X | X | X | 32 | 028000h to 02FFFFh |
| | SA11 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | 32 | 020000h to 027FFFh |
| | SA10 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | 32 | 018000h to 01FFFFh |
| | SA9 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | 32 | 010000h to 017FFFh |
| | SA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | 32 | 008000h to 00FFFFh |
| | SA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 4 | 007000h to 007FFFh |
| | SA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 4 | 006000h to 006FFFh |
| | SA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 4 | 005000h to 005FFFh |
| | SA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | 004000h to 004FFFh |
| | SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 | 003000h to 003FFFh |
| | SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4 | 002000h to 002FFFh |
| | SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 4 | 001000h to 001FFFh |
| | SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 000000h to 000FFFh |

**MBM29PDS322BE Bottom Boot Sector Architecture**

**Table 7.1 Sector Group Address Table (MBM29PDS322TE) (Top Boot Block)**

| Sector Group | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | Sectors |
|---|---|---|---|---|---|---|---|---|---|---|
| SGA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | SA0 |
| SGA1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | SA1 to SA3 |
| | | | | | 1 | 0 | | | | |
| | | | | | 1 | 1 | | | | |
| SGA2 | 0 | 0 | 0 | 1 | X | X | X | X | X | SA4 to SA7 |
| SGA3 | 0 | 0 | 1 | 0 | X | X | X | X | X | SA8 to SA11 |
| SGA4 | 0 | 0 | 1 | 1 | X | X | X | X | X | SA12 to SA15 |
| SGA5 | 0 | 1 | 0 | 0 | X | X | X | X | X | SA16 to SA19 |
| SGA6 | 0 | 1 | 0 | 1 | X | X | X | X | X | SA20 to SA23 |
| SGA7 | 0 | 1 | 1 | 0 | X | X | X | X | X | SA24 to SA27 |
| SGA8 | 0 | 1 | 1 | 1 | X | X | X | X | X | SA28 to SA31 |
| SGA9 | 1 | 0 | 0 | 0 | X | X | X | X | X | SA32 to SA35 |
| SGA10 | 1 | 0 | 0 | 1 | X | X | X | X | X | SA36 to SA39 |
| SGA11 | 1 | 0 | 1 | 0 | X | X | X | X | X | SA40 to SA43 |
| SGA12 | 1 | 0 | 1 | 1 | X | X | X | X | X | SA44 to SA47 |
| SGA13 | 1 | 1 | 0 | 0 | X | X | X | X | X | SA48 to SA51 |
| SGA14 | 1 | 1 | 0 | 1 | X | X | X | X | X | SA52 to SA55 |
| SGA15 | 1 | 1 | 1 | 0 | X | X | X | X | X | SA56 to SA59 |
| SGA16 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | SA60 to SA62 |
| | | | | | 0 | 1 | | | | |
| | | | | | 1 | 0 | | | | |
| SGA17 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | SA63 |
| SGA18 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | SA64 |
| SGA19 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | SA65 |
| SGA20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | SA66 |
| SGA21 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | SA67 |
| SGA22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | SA68 |
| SGA23 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | SA69 |
| SGA24 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | SA70 |

**Table 7.2 Sector Group Address Table (MBM29PDS322BE) (Bottom Boot Block)**

| Sector Group | $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | $A_{16}$ | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | Sectors |
|---|---|---|---|---|---|---|---|---|---|---|
| SGA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SA0 |
| SGA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SA1 |
| SGA2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SA2 |
| SGA3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | SA3 |
| SGA4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SA4 |
| SGA5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SA5 |
| SGA6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | SA6 |
| SGA7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | SA7 |
| SGA8 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | SA8 to SA10 |
| | | | | | 1 | 0 | | | | |
| | | | | | 1 | 1 | | | | |
| SGA9 | 0 | 0 | 0 | 1 | X | X | X | X | X | SA11 to SA14 |
| SGA10 | 0 | 0 | 1 | 0 | X | X | X | X | X | SA15 to SA18 |
| SGA11 | 0 | 0 | 1 | 1 | X | X | X | X | X | SA19 to SA22 |
| SGA12 | 0 | 1 | 0 | 0 | X | X | X | X | X | SA23 to SA26 |
| SGA13 | 0 | 1 | 0 | 1 | X | X | X | X | X | SA27 to SA30 |
| SGA14 | 0 | 1 | 1 | 0 | X | X | X | X | X | SA31 to SA34 |
| SGA15 | 0 | 1 | 1 | 1 | X | X | X | X | X | SA35 to SA38 |
| SGA16 | 1 | 0 | 0 | 0 | X | X | X | X | X | SA39 to SA42 |
| SGA17 | 1 | 0 | 0 | 1 | X | X | X | X | X | SA43 to SA46 |
| SGA18 | 1 | 0 | 1 | 0 | X | X | X | X | X | SA47 to SA50 |
| SGA19 | 1 | 0 | 1 | 1 | X | X | X | X | X | SA51 to SA54 |
| SGA20 | 1 | 1 | 0 | 0 | X | X | X | X | X | SA55 to SA58 |
| SGA21 | 1 | 1 | 0 | 1 | X | X | X | X | X | SA59 to SA62 |
| SGA22 | 1 | 1 | 1 | 0 | X | X | X | X | X | SA63 to SA66 |
| SGA23 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X | SA67 to SA69 |
| | | | | | 0 | 1 | | | | |
| | | | | | 1 | 0 | | | | |
| SGA24 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X | SA70 |

## ■ FUNCTIONAL DESCRIPTION

### Simultaneous Operation

The device has feature, which is capable of reading data from one bank of memory while a program or erase operation is in progress in the other bank of memory (simultaneous operation), in addition to the conventional features (read, program, erase, erase-suspend read, and erase-suspend program). The bank selection can be selected by bank address ($A_{20}$ to $A_{15}$) with zero latency.

The device has two banks which contain
Bank 1 (4 KW × eight sectors, 32 KW × seven sectors) and Bank 2 (32 KW × fifty-six sectors).

The simultaneous operation can not execute multi-function mode in the same bank. Table 8 shows the possible combinations for simultaneous operation. (Refer to Figure 12 Back-to-Back Read/Write Timing Diagram.)

**Table 8 Simultaneous Operation**

| Case | Bank 1 Status | Bank 2 Status |
|---|---|---|
| 1 | Read mode | Read mode |
| 2 | Read mode | Autoselect mode |
| 3 | Read mode | Program mode |
| 4 | Read mode | Erase mode * |
| 5 | Autoselect mode | Read mode |
| 6 | Program mode | Read mode |
| 7 | Erase mode * | Read mode |

*: An erase operation may also be suspended to read from or program to a sector not being erased.

### Read Mode

The device has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used as the gate data to the output pins if a device is selected.

Address access time ($t_{ACC}$) is equal to delay from stable addresses to valid output data. The chip enable access time ($t_{CE}$) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time ($t_{OE}$) is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least $t_{ACC}$-$t_{OE}$ time.) When reading out data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” or “L”.

### Page Mode Read

The device is capable of fast Page mode read operation. This mode provides faster read access speed for random locations within a page. The Page size of the device is 4 words, within the appropriate Page being selected by the higher address bits $A_{20}$ to $A_2$ and the LSB bits $A_1$ and $A_0$ within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is equal to $t_{ACC}$ and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to $t_{PACC}$. Here again, $\overline{CE}$ selects the device and $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping $A_{20}$ to $A_2$ constant and changing $A_1$ and $A_0$ to select the specific word, within that page. See Figure 5.4 for timing specifications.

### Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC}$ ± 0.3 V. Under this condition, the current consumed is less than 5 µA Max. During Embedded Algorithm operation, $V_{CC}$ active current ($I_{CC2}$) is required even $\overline{CE}$ = "H". The device can be read with standard access time ($t_{CE}$) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS}$ ± 0.3 V ($\overline{CE}$ = "H" or "L"). Under this condition the current consumed is less than 5 µA Max. Once the $\overline{RESET}$ pin is taken high, the device requires $t_{RH}$ as wake up time for outputs to be valid for read access.

In the standby mode, the outputs are in the high impedance state, independently of the $\overline{OE}$ input.

### Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of the device data. This mode can be useful in the application such as a handy terminal which requires low power consumption.

To activate this mode, the device automatically switches themselves to low power mode when the device addresses remain stable during access time of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 50 µA (CMOS Level).

During simultaneous operation, $V_{CC}$ active current ($I_{CC2}$) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically, and the device reads the data for changed addresses.

### Output Disable

With the $\overline{OE}$ input at a logic high level ($V_{IH}$), output from the device is disabled. This will cause the output pins to be in a high impedance state.

### Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force $V_{ID}$ (10.0 V to 11.0 V) on address pin $A_9$. Two identifier bytes may then be sequenced from the device outputs by toggling address $A_0$ from $V_{IL}$ to $V_{IH}$. All addresses are DON'T CARES except $A_6$, $A_3$, $A_2$, $A_1$, and $A_0$. (See Table 3.)

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the $A_9$ pin. The command sequence is illustrated in Table 4. (Refer to Autoselect Command section.)

In the command Autoselect mode, the bank addresses BA; ($A_{20}$ to $A_{12}$) must point to a specific bank during the third write bus cycle of the Autoselect command. Then the Autoselect data will be read from that bank while array data can be read from the other bank.

A read cycle from address (BA)00h returns the manufacturer's code (Fujitsu = 04h). And a read cycle from address (BA)01h, (BA)0Eh to (BA)0Fh returns the device code. (See Tables 5.1 to 5.4.)

In case of applying $V_{ID}$ on $A_9$, since both Bank 1 and Bank 2 enter Autoselect mode, the simultaneous operation can not be executed.

### Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to $V_{IL}$, while $\overline{CE}$ is at $V_{IL}$ and $\overline{OE}$ is at $V_{IH}$. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

### Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of twenty five sector groups of memory. (See Table 7.) The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force $V_{ID}$ on address pin $A_9$ and control pin $\overline{OE}$, (suggest $V_{ID}$ = 11.5 V), $\overline{CE}$ = $V_{IL}$ and ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0). The sector group addresses ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$, and $A_{12}$) should be set to the sector to be protected. Tables 6.1 and 6.2 define the sector address for each of the seventy one (71) individual sectors, and tables 7.1 and 7.2 define the sector group address for each of the twenty five (25) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See Figures 16 and 24 for sector group protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force $V_{ID}$ on address pin $A_9$ with $\overline{CE}$ and $\overline{OE}$ at $V_{IL}$ and $\overline{WE}$ at $V_{IH}$. Scanning the sector group addresses ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$, and $A_{12}$) while ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0) will produce a logical "1" code at device output $DQ_0$ for a protected sector. Otherwise the device will produce "0" for unprotected sector. In this mode, the lower order addresses, except for $A_0$, $A_1$, $A_2$, $A_3$, and $A_6$ are DON'T CARES. Address locations with $A_1$ = $V_{IL}$ are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$, and $A_{12}$) are the desired sector group address will produce a logical "1" at $DQ_0$ for a protected sector group. See Tables 5.1 to 5.4 for Autoselect codes.

### Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the device in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage ($V_{ID}$). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the $V_{ID}$ is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to Figures 17 and 25.

### Extended Sector Group Protection

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables to protect sector group by forcing $V_{ID}$ on $\overline{RESET}$ pin and write a command sequence. Unlike conventional procedure, it is not necessary to force $V_{ID}$ and control timing for control pins. The only $\overline{RESET}$ pin requires $V_{ID}$ for sector group protection in this mode. The extended sector group protection requires $V_{ID}$ on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector group addresses pins ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$ and $A_{12}$) and ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0) should be set to the sector group to be protected (recommend to set $V_{IL}$ for the other addresses pins), and write extended sector group protection command (60h). A sector group is

typically protected in 250 µs. To verify programming of the protection circuitry, the sector group addresses pins ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$ and $A_{12}$) and ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0) should be set and write a command (40h). Following the command write, a logical "1" at device output $DQ_0$ will produce for protected sector in the read operation. If the output is logical "0", please repeat to write extended sector group protection command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to $V_{IH}$. (Refer to the Figures 18 and 26.)

**$\overline{RESET}$**

Hardware Reset

The device may be reset by driving the $\overline{RESET}$ pin to $V_{IL}$. The $\overline{RESET}$ pin vs. a pulse requirement and has to be kept low ($V_{IL}$) for at least "$t_{RP}$" in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode "$t_{READY}$" after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the device requires an additional "$t_{RH}$" before it will allow read access. When the $\overline{RESET}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See Figure 14 for the timing diagram. Refer to Temporary Sector Group Unprotection for additional functionality.

**Boot Block Sector Protection**

The Write Protection function provides a hardware method of protecting certain boot sectors without using $V_{ID}$. This function is one of two provided by the $\overline{WP}$/ACC pin.

If the system asserts $V_{IL}$ on the $\overline{WP}$/ACC pin, the device disables program and erase functions in the two "outermost" 4K word boot sectors independently of whether those sectors are protected or unprotected using the method described in "Sector Protection/Unprotection". The two outermost 4K word boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-congfigured device.
(MBM29PDS322TE: SA69 and SA70, MBM29PDS322BE: SA0 and SA1)

If the system asserts $V_{IH}$ on the $\overline{WP}$/ACC pin, the device reverts to whether the two outermost 4K word boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector protection/unprotection".

**Accelerated Program Operation**

The device offers accelerated program operation which enables the programming in high speed. If the system asserts $V_{ACC}$ to the $\overline{WP}$/ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing $V_{ACC}$ from the $\overline{WP}$/ACC pin returns the device to normal operation. Do not remove $V_{ACC}$ from $\overline{WP}$/ACC pin while programming. See Figure 19.

## ■ COMMAND DEFINITIONS

The device operations are selected by writing specific address and data sequences into the command register. Some commands require Bank Address (BA) input. When command sequences are inputted to bank being read, the commands have priority over reading. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover, both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at $DQ_7$ to $DQ_0$ and $DQ_{15}$ to $DQ_8$ bits are ignored.

### Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits ($DQ_5$ = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

### Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising $A_9$ to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by firstly writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data of memory cell can be read from the another bank.

Following the command write, a read cycle from address (BA)00h retrieves the manufacture code of 04h. A read cycle at address (BA)01h returns 7Eh to indicate that this device uses extended device code. The successive read cycle from (BA)0Eh to (BA)0Fh returns this extended device code for this device. (See Tables 5.1 to 5.4.)

The sector state (protection or unprotection) will be informed by address (BA)02h. Scanning the sector group addresses ($A_{20}$, $A_{19}$, $A_{18}$, $A_{17}$, $A_{16}$, $A_{15}$, $A_{14}$, $A_{13}$, and $A_{12}$) while ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0) will produce a logical “1” at device output $DQ_0$ for a protected sector group. The programming verification should be performed by verify sector group protection on the protected sector. (See Table 3.)

The manufacture and device codes can be allowed to read from selected bank. To read the manufacture and device codes and sector protection status from non-selected bank, it is necessary to write Read/Reset command sequence into the register and then Autoselect command should be written into the bank to be read.

If the software (program code) for Autoselect command is stored into the Flash memory, the device and manufacture codes should be read from the other bank which doesn’t contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, writing Read/Reset command sequence must precede the Autoselect command.

### Word Programming

The device is programmed on a word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using $DQ_7$ ($\overline{Data}$ Polling), $DQ_6$ (Toggle Bit), or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on $DQ_7$ is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. (See Table 9, Hardware Sequence Flags.) Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 20 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

### Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using $DQ_7$ ($\overline{Data}$ Polling), $DQ_6$ (Toggle Bit), or RY/$\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on $DQ_7$ is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time $\times$ All sectors + Chip Program Time (Preprogramming)

Figure 21 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

**Sector Erase**

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of “$t_{TOW}$” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table4. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “$t_{TOW}$” otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “$t_{TOW}$” from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the “$t_{TOW}$” time-out window the timer is reset. (Monitor $DQ_3$ to determine if the sector erase timer window is still open, see section $DQ_3$, Sector Erase Timer.) Resetting the device once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 70).

Sector erase does not require the user to program the device prior to erase. The device automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using $DQ_7$ ($\overline{Data}$ Polling), $DQ_6$ (Toggle Bit), or RY/$\overline{BY}$.

The sector erase begins after the “$t_{TOW}$” time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on $DQ_7$ is “1” (See Write Operation Status section.) at which time the device returns to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] $\times$ Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from bank (read-while-erase) can not perform.

Figure 21 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

**Erase Suspend/Resume**

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. Writing the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The bank addresses of sector being erased or erase-suspended should be set when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "$t_{SPD}$" to suspend the erase operation. When the device has entered the erase-suspended mode, the RY/$\overline{BY}$ output pin will be at Hi-Z and the $DQ_7$ bit will be at logic "1", and $DQ_6$ will stop toggling. The user must use the address of the erasing sector for reading $DQ_6$ and $DQ_7$ to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause $DQ_2$ to toggle. (See the section on $DQ_2$.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause $DQ_2$ to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{Data}$ polling of $DQ_7$ or by the Toggle Bit I ($DQ_6$) which is the same as the regular Program operation. Note that $DQ_7$ must be read from the Program address while $DQ_6$ can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30h) should be written to the bank being erase suspended. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

**Extended Command**

(1) Fast Mode

The device has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address. (Refer to the Figure 27.) The $V_{CC}$ active current is required even $\overline{CE}$ = $V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). (Refer to the Figure 27.)

### Hidden ROM (Hi-ROM) Region

The Hi-ROM feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Hi-ROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The Hi-ROM region is 32 Kwords in length and is stored at the same address as the 4 KW ×8 sectors. The MBM29PDS322TE occupies the address of the word mode 1F8000h to 1FFFFFh and the MBM29PDS322BE type occupies the address of the word mode 000000h to 007FFFh. After the system has written the Enter Hi-ROM command sequence, the system may read the Hi-ROM region by using the addresses normally occupied by the boot sectors. That is, the device sends all commands that would normally be sent to the boot sectors to the Hi-ROM region. This mode of operation continues until the system issues the Exit Hi-ROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

When reading the Hi-ROM region, either change addresses or change $\overline{CE}$ pin from "H" to "L". The same procedure should be taken (changing addresses or $\overline{CE}$ pin from "H" to "L") after the system issues the Exit Hi-ROM command sequence to read actual data of memory cell.

### Hidden ROM (Hi-ROM) Entry Command

The device has a Hidden ROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Program/erase is possible in this area until it is protected. However, once it is protected, it is impossible to unprotect, so please use this with caution.

Hidden ROM area is 32 K words and in the same address area as 4 KW sector. The address of top boot is 1F8000h to 1FFFFFh at word mode and the bottom boot is 000000h to 007FFFh at word mode. These areas are normally the boot block area (4 KW ×8 sector). Therefore, write the Hidden ROM entry command sequence to enter the Hidden ROM area. It is called Hidden ROM mode when the Hidden ROM area appears.

Sector other than the boot block area could be read during Hidden ROM mode. Read/program/erase of the Hidden ROM area is possible during Hidden ROM mode. Write the Hidden ROM reset command sequence to exit the Hidden ROM mode. The bank address of the Hidden ROM should be set on the third cycle of this reset command sequence.

### Hidden ROM (Hi-ROM) Program Command

To program the data to the Hidden ROM area, write the Hidden ROM program command sequence during Hidden ROM mode. This command is the same as the program command in usual except to write the command during Hidden ROM mode. Therefore the detection of completion method is the same as in the past, using the $DQ_7$ data poling, $DQ_6$ toggle bit and RY/$\overline{BY}$ pin. It is necessary to pay attention to the address to be programmed. If the address other than the Hidden ROM area is selected to program, data of the address will be changed.

### Hidden ROM (Hi-ROM) Erase Command

To erase the Hidden ROM area, write the Hidden ROM erase command sequence during Hidden ROM mode. This command is same as the sector erase command in the past except to write the command during Hidden ROM mode. Therefore the detection of completion method is the same as in the past, using the $DQ_7$ data poling, $DQ_6$ toggle bit and RY/$\overline{BY}$ pin. It is necessary to pay attention to the sector address to be erased. If the sector address other than the Hidden ROM area is selected, the data of the sector will be changed.

### Hidden ROM (Hi-ROM) Protect Command

There are two methods to protect the Hidden ROM area. One is to write the sector group protect setup command(60h), set the sector address in the Hidden ROM area and ($A_6$, $A_3$, $A_2$,$A_1$, $A_0$) = (0,0,0,1,0), and write the sector group protect command(60h) during the Hidden ROM mode. The same command sequence could be used because, it is the same as the extension sector group protect in the past except that it is in the Hidden ROM mode and it does not apply high voltage to $\overline{\text{RESET}}$ pin. Please refer to “Function Explanation Extended Sector Group Protection” for details of extension sector group protect setting.

The other is to apply high voltage ($V_{ID}$) to $A_9$ and $\overline{\text{OE}}$, set the sector address in the Hidden ROM area and ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0), and apply the write pulse during the Hidden ROM mode. To verify the protect circuit, apply high voltage ($V_{ID}$) to $A_9$, specify ($A_6$, $A_3$, $A_2$, $A_1$, $A_0$) = (0, 0, 0, 1, 0) and the sector address in the Hidden ROM area, and read. When “1” appears on $DQ_0$, the protect setting is completed. “0” will appear on $DQ_0$ if it is not protected. Please apply write pulse again. The same command sequence could be used for the above method because other than the Hidden ROM mode, it is the same as the sector group protect previously mentioned. Please refer to “Function Explanation Sector Group Protection” for details of the sector group protect setting.

Other sector group will be effected if the address other than those for Hidden ROM area is selected for the sector group address, so please be careful. Once it is protected, protection can not be cancelled, so please pay the closest attention.

### Write Operation Status

Detailed in Table 9 are all the status flags that can determine the status of the bank for the current mode operation. The read operation from the bank which doesn’t operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether a Embedded Algorithm is completed properly. The information on $DQ_2$ is address sensitive. This means that if an address from an erasing sector is consecutively read, then the $DQ_2$ bit will toggle. However, $DQ_2$ will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

The status flag is not output from bank (non-busy bank) which doesn’t execute Embedded Algorithm. For example, there is bank (busy bank) which is now executing Embedded Algorithm. When the read sequence is [1] <busy bank>, [2] <non-busy bank>, [3] <busy bank>, the $DQ_6$ is toggling in the case of [1] and [3]. In case of [2], the data of memory cells are outputted. In the erase-suspend read mode with the same read sequence, $DQ_6$ will not be toggled in the [1] and [3].

In the erase suspend read mode, $DQ_2$ is toggled in the [1] and [3]. In case of [2], the data of memory cell is outputted.

**Table 9 Hardware Sequence Flags**

| Status | | | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_3$ | $DQ_2$ |
|---|---|---|---|---|---|---|---|
| In Progress | Embedded Program Algorithm | | $\overline{DQ_7}$ | Toggle | 0 | 0 | 1 |
| | Embedded Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle * |
| | Erase Suspended Mode | Erase Suspend Read (Erase Suspended Sector) | 1 | 1 | 0 | 0 | Toggle |
| | | Erase Suspend Read (Non-Erase Suspended Sector) | Data | Data | Data | Data | Data |
| | | Erase Suspend Program (Non-Erase Suspended Sector) | $\overline{DQ_7}$ | Toggle | 0 | 0 | 1 * |
| Exceeded Time Limits | Embedded Program Algorithm | | $\overline{DQ_7}$ | Toggle | 1 | 0 | 1 |
| | Embedded Erase Algorithm | | 0 | Toggle | 1 | 1 | N/A |
| | Erase Suspended Mode | Erase Suspend Program (Non-Erase Suspended Sector) | $\overline{DQ_7}$ | Toggle | 1 | 0 | N/A |

*: Successive reads from the erasing or erase-suspend sector will cause $DQ_2$ to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the $DQ_2$ bit.

Note 1.$DQ_0$ and $DQ_1$ are reserve pins for future use.
2.$DQ_4$ is Fujitsu internal use.

**$DQ_7$**

$\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read device will produce a complement of data last written to $DQ_7$. Upon completion of the Embedded Program Algorithm, an attempt to read device will produce true data last written to $DQ_7$. During the Embedded Erase Algorithm, an attempt to read device will produce a "0" at the $DQ_7$ output. Upon completion of the Embedded Erase Algorithm an attempt to read device will produce a "1" on $DQ_7$. The flowchart for $\overline{\text{Data}}$ Polling ($DQ_7$) is shown in Figure 23.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address of sectors being erased, not protected sectors. Otherwise, the status may be invalid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on $DQ_7$ is active for approximately 1 µs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on $DQ_7$ is active for approximately 400 µs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to completion, the device data pins ($DQ_7$) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that device is driving status information on $DQ_7$ at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the $DQ_7$ output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and $DQ_7$ has a valid data, data outputs on $DQ_0$ to $DQ_6$ may be still invalid. The valid data on $DQ_0$ to $DQ_7$ will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 9.)

See Figure 10 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

**$DQ_6$**

Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will results in $DQ_6$ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, $DQ_6$ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, device will erase all selected sectors except for ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data unchanged.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause $DQ_6$ to toggle. In addition, an Erase Suspend/Resume command will cause $DQ_6$ to toggle.

The system can use $DQ_6$ to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress), $DQ_6$ toggles. When a bank enters the Erase Suspend mode, $DQ_6$ stops toggling. Successive read cycles during erase-suspend-program cause $DQ_6$ to toggle.

To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

See Figure 11 for the Toggle Bit I timing specifications and diagrams.

**$DQ_5$**

Exceeded Timing Limits

$DQ_5$ will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions $DQ_5$ will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of device under this condition. The $\overline{\text{CE}}$ circuit will partially power down device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 8.

The $DQ_5$ failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case the device locks out and never complete the Embedded Algorithm operation. Hence, the system never read valid data on $DQ_7$ bit and $DQ_6$ never stop toggling. Once device has exceeded timing limits, the $DQ_5$ bit will indicate a “1.” Please note that this is not a device failure condition since device was incorrectly used. If this occurs, reset device with command sequence.

**$DQ_3$**

Sector Erase Timer

After completion of the initial sector erase command sequence sector erase time-out will begin. $DQ_3$ will remain low until the time-out is completed. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates device has been written with a valid erase command, $DQ_3$ may be used to determine if the sector erase timer window is still open. If $DQ_3$ is high (“1”) the internally controlled erase cycle has begun.If $DQ_3$ is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of $DQ_3$ prior to and following each subsequent Sector Erase command. If $DQ_3$ were high on the second status check, the command may not have been accepted.

See Table 9: Hardware Sequence Flags.

**$DQ_2$**

Toggle Bit II

This toggle bit II, along with $DQ_6$, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause $DQ_2$ to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause $DQ_2$ to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the $DQ_2$ bit.

$DQ_6$ is different from $DQ_2$ in that $DQ_6$ toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of $DQ_7$, is summarized as follows:

For example, $DQ_2$ and $DQ_6$ can be used together to determine if the erase-suspend-read mode is in progress. ($DQ_2$ toggles while $DQ_6$ does not.) See also and.

Furthermore, $DQ_2$ can also be used to determine which sector is being erased. When device is in the erase mode, $DQ_2$ toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

### Reading Toggle Bits $DQ_6/DQ_2$

Whenever the system initially begins reading toggle bit status, it must read $DQ_7$ to $DQ_0$ at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on $DQ_7$ to $DQ_0$ on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of $DQ_5$ is high (see the section on $DQ_5$). If it is the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as $DQ_5$ went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and $DQ_5$ has not gone high. The system may continue to monitor the toggle bit and $DQ_5$ through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to Figure 23.)

**Table 10 Toggle Bit Status**

| Mode | $DQ_7$ | $DQ_6$ | $DQ_2$ |
|---|---|---|---|
| Program | $\overline{DQ_7}$ | Toggle | 1 |
| Erase | 0 | Toggle | Toggle (Note) |
| Erase-Suspend Read (Erase-Suspended Sector) | 1 | 1 | Toggle |
| Erase-Suspend Program | $\overline{DQ_7}$ | Toggle | 1 (Note) |

Note Successive reads from the erasing or erase-suspend sector will cause $DQ_2$ to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the $DQ_2$ bit.

### RY/$\overline{BY}$

Ready/Busy

The device provides a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or has been completed. If output is low, device is busy with either a program or erase operation. If output is high, device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, RY/$\overline{BY}$ output will be high.

During programming, RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. RY/$\overline{BY}$ pin will indicate a busy condition during $\overline{RESET}$ pulse. Refer to Figures 13 and 14 for a detailed timing diagram. RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to $V_{CC}$.

### Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from $V_{CC}$ power-up and power-down transitions or system noise.

### Power On/Off Timing

The RESET pin must be held low during $V_{CC}$ ramp up to insure that device power up correctly.
(Refer to Figure 5.3.)

### Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

### Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

### Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| Storage Temperature | Tstg | –55 | +125 | °C |
| Ambient Temperature with Power Applied | $T_A$ | –40 | +85 | °C |
| Voltage with Respect to Ground All pins except $A_9$, $\overline{OE}$, and $\overline{RESET}$ (Note 1) | $V_{IN}$, $V_{OUT}$ | –0.5 | $V_{CC}$+0.5 | V |
| Power Supply Voltage (Note 1) | $V_{CC}$ | –0.5 | +3.0 | V |
| $A_9$, $\overline{OE}$, and $\overline{RESET}$ (Note 2) | $V_{IN}$ | –0.5 | +11.5 | V |
| $\overline{WP}$/ACC (Note 3) | $V_{ACC}$ | –0.5 | +10.5 | V |

Notes: 1.Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}$ +0.5 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}$ +2.0 V for periods of up to 20 ns.

2.Minimum DC input voltage on $A_9$, $\overline{OE}$ and $\overline{RESET}$ pins is –0.5 V. During voltage transitions, $A_9$, $\overline{OE}$ and $\overline{RESET}$ pins may undershoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage ($V_{IN}$-$V_{CC}$) does not exceed +9.0V. Maximum DC input voltage on $A_9$, $\overline{OE}$ and $\overline{RESET}$ pins is +11.5 V which may positive overshoot to +12.5 V for periods of up to 20 ns.

3.Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may positive overshoot to +12.0 V for periods of up to 20ns when Vcc is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING RANGES

| Parameter | Symbol | Part No. | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Ambient Temperature | $T_A$ | MBM29PDS322TE/BE 10/11 | –40 | +85 | °C |
| Power Supply Voltage | $V_{CC}$ | MBM29PDS322TE/BE 10/11 | +1.8 | +2.2 | V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ MAXIMUM OVERSHOOT / UNDERSHOOT

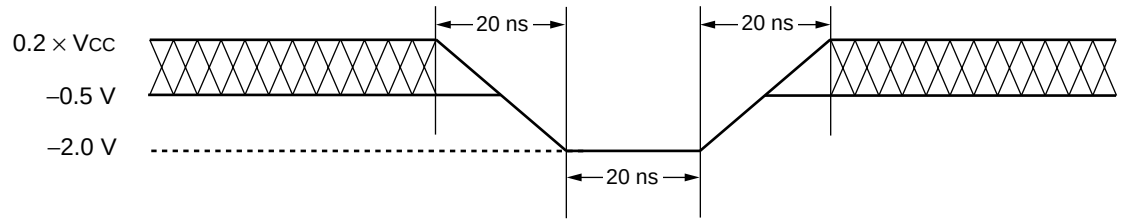



**Figure 1 Maximum Undershoot Waveform**

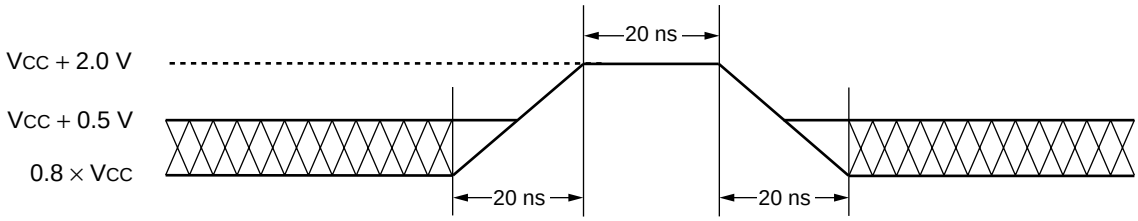
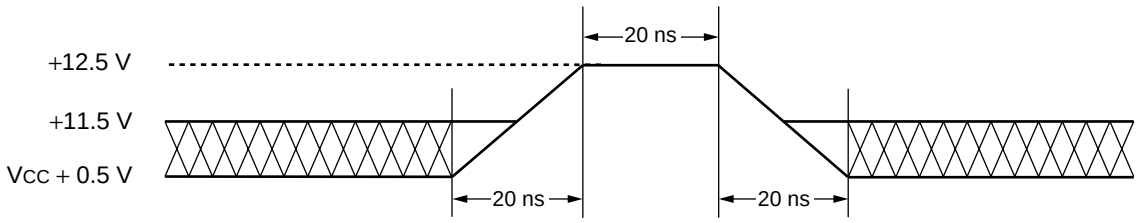



**Figure 2 Maximum Overshoot Waveform 1**




Note: This waveform is applied for $A_9$, $\overline{OE}$ and $\overline{RESET}$

**Figure 3 Maximum Overshoot Waveform 2**

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

| Parameter | Symbol | Conditions | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{SS}$ to $V_{CC}$, $V_{CC}$ = $V_{CC}$ Max. | –1.0 | +1.0 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$, $V_{CC}$ = $V_{CC}$ Max. | –1.0 | +1.0 | µA |
| $A_9$, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current | $I_{LIT}$ | $V_{CC}$ = $V_{CC}$ Max.<br>$A_9$, $\overline{OE}$, $\overline{RESET}$ = 11.0 V | — | 35 | µA |
| $V_{CC}$ Active Current *1 | $I_{CC1}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 8 MHz | — | 21 | mA |
| | | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 1 MHz | — | 3 | mA |
| $V_{CC}$ Active Current *2 | $I_{CC2}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | — | 30 | mA |
| $V_{CC}$ Current (Standby) | $I_{CC3}$ | $V_{CC}$ = $V_{CC}$ Max., $\overline{CE}$ = $V_{CC}$ ± 0.3 V, $\overline{RESET}$ = $V_{CC}$ ± 0.3 V | — | 5 | µA |
| $V_{CC}$ Current (Standby, Reset) | $I_{CC4}$ | $V_{CC}$ = $V_{CC}$ Max., $\overline{WE}$/ACC = $V_{CC}$ ± 0.3 V, $\overline{RESET}$ = $V_{SS}$ ± 0.3 V | — | 5 | µA |
| $V_{CC}$ Current (Automatic Sleep Mode) *3 | $I_{CC5}$ | $V_{CC}$ = $V_{CC}$ Max., $\overline{CE}$ = $V_{SS}$ ± 0.3 V, $\overline{RESET}$ = $V_{CC}$ ± 0.3 V<br>$V_{IN}$ = $V_{CC}$ ± 0.3 V or $V_{SS}$ ± 0.3 V | — | 5 | µA |
| $V_{CC}$ Active Current *5 (Read-While-Program) | $I_{CC6}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | — | 55 | mA |
| $V_{CC}$ Active Current *5 (Read-While-Erase) | $I_{CC7}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | — | 55 | mA |
| $V_{CC}$ Active Current (Erase-Suspend-Program) | $I_{CC8}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | — | 35 | mA |
| $V_{CC}$ Active Current (Intra-Page Read) | $I_{CC9}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 20 MHz | — | 5 | mA |
| $\overline{WP}$/ACC Accelerated Program Current | $I_{ACC}$ | $V_{CC}$ = $V_{CC}$ Max.<br>$\overline{WP}$/ACC = $V_{ACC}$ Max. | — | 20 | mA |
| Input Low Level | $V_{IL}$ | — | –0.5 | 0.2× $V_{CC}$ | V |
| Input High Level | $V_{IH}$ | — | 0.8× $V_{CC}$ | $V_{CC}$+0.3 | V |
| Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration *4 | $V_{ACC}$ | — | 8.5 | 12.5 | V |
| Voltage for Autoselect and Sector Protection ($A_9$, $\overline{OE}$, $\overline{RESET}$) *4 | $V_{ID}$ | — | 10.0 | 11.0 | V |
| Output Low Voltage Level | $V_{OL}$ | $I_{OL}$ = 100 µA, $V_{CC}$ = $V_{CC}$ Min. | — | 0.1 | V |
| Output High Voltage Level | $V_{OH}$ | $I_{OH}$ = –100 µA | $V_{CC}$–0.1 | — | V |

*1: The $I_{CC}$ current listed includes both the DC operating current and the frequency dependent component.

*2: $I_{CC}$ is active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only $V_{CC}$ applying.

*5: Embedded Algorithm (program or erase) is in progress. (@5 MHz)

## 2. AC Characteristics

- **Read Only Operations Characteristics**

| Parameter | Symbol | | Conditions | Value(Note) | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | 10 | | 11 | | |
| | JEDEC | Standard | | Min. | Max. | Min. | Max. | |
| Read Cycle Time | $t_{AVAV}$ | $t_{RC}$ | — | 100 | — | 115 | — | ns |
| Address to Output Delay | $t_{AVQV}$ | $t_{ACC}$ | $\overline{CE} = V_{IL}$<br>$\overline{OE} = V_{IL}$ | — | 100 | — | 115 | ns |
| Page Read Cycle Time | — | $t_{PRC}$ | — | 45 | — | 45 | — | ns |
| Page Address to Output Delay | — | $t_{PACC}$ | $\overline{CE} = V_{IL}$<br>$\overline{OE} = V_{IL}$ | — | 45 | — | 45 | ns |
| Chip Enable to Output Delay | $t_{ELQV}$ | $t_{CE}$ | $\overline{OE} = V_{IL}$ | — | 100 | — | 115 | ns |
| Output Enable to Output Delay | $t_{GLQV}$ | $t_{OE}$ | — | — | 35 | — | 45 | ns |
| Chip Enable to Output High-Z | $t_{EHQZ}$ | $t_{DF}$ | — | — | 30 | — | 30 | ns |
| Output Enable to Output High-Z | $t_{GHQZ}$ | $t_{DF}$ | — | — | 30 | — | 30 | ns |
| Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First | $t_{AXQX}$ | $t_{OH}$ | — | 0 | — | 0 | — | ns |
| $\overline{RESET}$ Pin Low to Read Mode | — | $t_{READY}$ | — | — | 20 | — | 20 | µs |

Note: Test Conditions:
Output Load: $C_L$ = 50 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 2.0 V
Timing measurement reference level
Input: 1.0 V
Output: 1.0 V

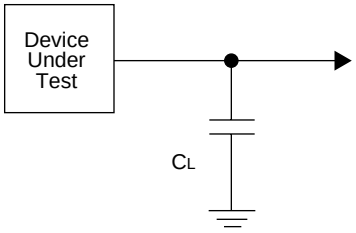



**Figure 4 Test Conditions**

• **Write/Erase/Program Operations**

| Parameter | | Symbol | | Value | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 10 | | | 11 | | | |
| | | JEDEC | Standard | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Write Cycle Time | | $t_{AVAV}$ | $t_{WC}$ | 100 | — | — | 115 | — | — | ns |
| Address Setup Time | | $t_{AVWL}$ | $t_{AS}$ | 0 | — | — | 0 | — | — | ns |
| Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling | | — | $t_{ASO}$ | 15 | — | — | 15 | — | — | ns |
| Address Hold Time | | $t_{WLAX}$ | $t_{AH}$ | 60 | — | — | 60 | — | — | ns |
| Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling | | — | $t_{AHT}$ | 0 | — | — | 0 | — | — | ns |
| Data Setup Time | | $t_{DVWH}$ | $t_{DS}$ | 60 | — | — | 60 | — | — | ns |
| Data Hold Time | | $t_{WHDX}$ | $t_{DH}$ | 0 | — | — | 0 | — | — | ns |
| Output Enable Hold Time | Read | — | $t_{OEH}$ | 0 | — | — | 0 | — | — | ns |
| | Toggle and $\overline{Data}$ Polling | | | 10 | — | — | 10 | — | — | ns |
| $\overline{CE}$ High During Toggle Bit Polling | | — | $t_{CEPH}$ | 20 | — | — | 20 | — | — | ns |
| $\overline{OE}$ High During Toggle Bit Polling | | — | $t_{OEPH}$ | 20 | — | — | 20 | — | — | ns |
| Read Recover Time Before Write | | $t_{GHWL}$ | $t_{GHWL}$ | 0 | — | — | 0 | — | — | ns |
| Read Recover Time Before Write | | $t_{GHEL}$ | $t_{GHEL}$ | 0 | — | — | 0 | — | — | ns |
| $\overline{CE}$ Setup Time | | $t_{ELWL}$ | $t_{CS}$ | 0 | — | — | 0 | — | — | ns |
| $\overline{WE}$ Setup Time | | $t_{WLEL}$ | $t_{WS}$ | 0 | — | — | 0 | — | — | ns |
| $\overline{CE}$ Hold Time | | $t_{WHEH}$ | $t_{CH}$ | 0 | — | — | 0 | — | — | ns |
| $\overline{WE}$ Hold Time | | $t_{EHWH}$ | $t_{WH}$ | 0 | — | — | 0 | — | — | ns |
| Write Pulse Width | | $t_{WLWH}$ | $t_{WP}$ | 60 | — | — | 60 | — | — | ns |
| $\overline{CE}$ Pulse Width | | $t_{ELEH}$ | $t_{CP}$ | 60 | — | — | 60 | — | — | ns |
| Write Pulse Width High | | $t_{WHWL}$ | $t_{WPH}$ | 60 | — | — | 60 | — | — | ns |
| $\overline{CE}$ Pulse Width High | | $t_{EHEL}$ | $t_{CPH}$ | 60 | — | — | 60 | — | — | ns |
| Programming Operation | | $t_{WHWH1}$ | $t_{WHWH1}$ | — | 16 | — | — | 16 | — | µs |
| Sector Erase Operation *1 | | $t_{WHWH2}$ | $t_{WHWH2}$ | — | 1 | — | — | 1 | — | s |
| $V_{CC}$ Setup Time | | — | $t_{VCS}$ | 50 | — | — | 50 | — | — | µs |
| Rise Time to $V_{ID}$ *2 | | — | $t_{VIDR}$ | 500 | — | — | 500 | — | — | ns |
| Rise Time to $V_{ACC}$ *3 | | — | $t_{VACCR}$ | 500 | — | — | 500 | — | — | ns |
| Voltage Transition Time *2 | | — | $t_{VLHT}$ | 4 | — | — | 4 | — | — | µs |
| Write Pulse Width *2 | | — | $t_{WPP}$ | 100 | — | — | 100 | — | — | µs |
| $\overline{OE}$ Setup Time to $\overline{WE}$ Active *2 | | — | $t_{OESP}$ | 4 | — | — | 4 | — | — | µs |

*(Continued)*

*(Continued)*

| Parameter | Symbol | | Value | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 10 | | | 11 | | | |
| | JEDEC | Standard | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $\overline{CE}$ Setup Time to $\overline{WE}$ Active *2 | — | $t_{CSP}$ | 4 | — | — | 4 | — | — | µs |
| Recover Time From RY/$\overline{BY}$ | — | $t_{RB}$ | 0 | — | — | 0 | — | — | ns |
| $\overline{RESET}$ Pulse Width | — | $t_{RP}$ | 500 | — | — | 500 | — | — | ns |
| $\overline{RESET}$ High Level Period Before Read | — | $t_{RH}$ | 200 | — | — | 200 | — | — | ns |
| Program/Erase Valid to RY/$\overline{BY}$ Delay | — | $t_{BUSY}$ | — | — | 90 | — | — | 90 | ns |
| Delay Time from Embedded Output Enable | — | $t_{EOE}$ | — | — | 90 | — | — | 115 | ns |
| Erase Time-out Time | — | $t_{TOW}$ | 50 | — | | 50 | — | — | µs |
| Erase Suspend Transition Time | — | $t_{SPD}$ | — | — | 20 | — | — | 20 | µs |
| Power On / Off Time | — | $t_{PS}$ | — | — | 100 | — | — | 115 | ns |

*1: This does not include the preprogramming time.

*2: This timing is for Sector Group Protection operation.

*3: This timing is for Accelerated Program operation.

## ■ ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Unit | Comments |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Sector Erase Time | — | 1 | 10 | s | Excludes programming time prior to erasure |
| Word Programming Time | — | 16 | 360 | µs | Excludes system-level overhead |
| Chip Programming Time | — | — | 100 | s | Excludes system-level overhead |
| Program/Erase Cycle | 100,000 | — | — | cycle | — |

**FBGA PIN CAPACITANCE**

| Parameter | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Typ. | Max. | |
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0 | TBD | TBD | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 | TBD | TBD | pF |
| Control Pin Capacitance | $C_{IN2}$ | $V_{IN}$ = 0 | TBD | TBD | pF |
| $\overline{WP}$/ACC Pin Capacitance | $C_{IN3}$ | $V_{IN}$ = 0 | TBD | TBD | pF |

Note: Test conditions $T_A$ = 25°C, f = 1.0 MHz

## ■ TIMING DIAGRAM

- **Key to Switching Waveforms**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must Be Steady | Will Be Steady |
| | May Change from H to L | Will Be Changing from H to L |
| | May Change from L to H | Will Be Changing from L to H |
| | "H" or "L": Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High-Impedance "Off" State |

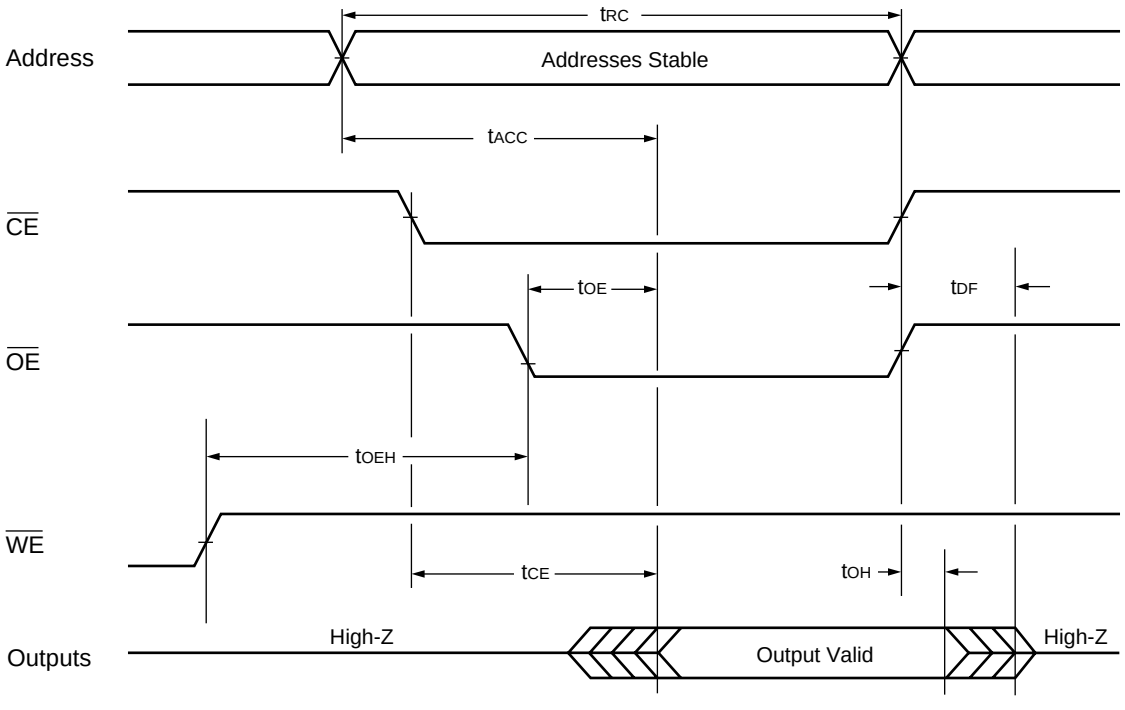



**Figure 5.1 Read Operation Timing Diagram**

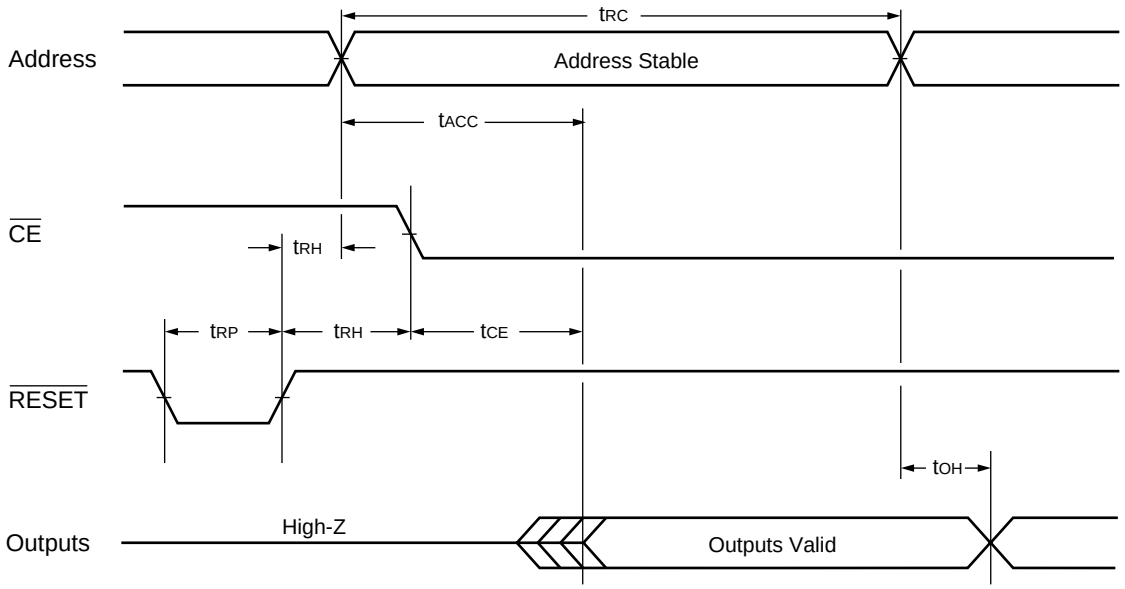



**Figure 5.2 Hardware Reset/Read Operation Timing Diagram**

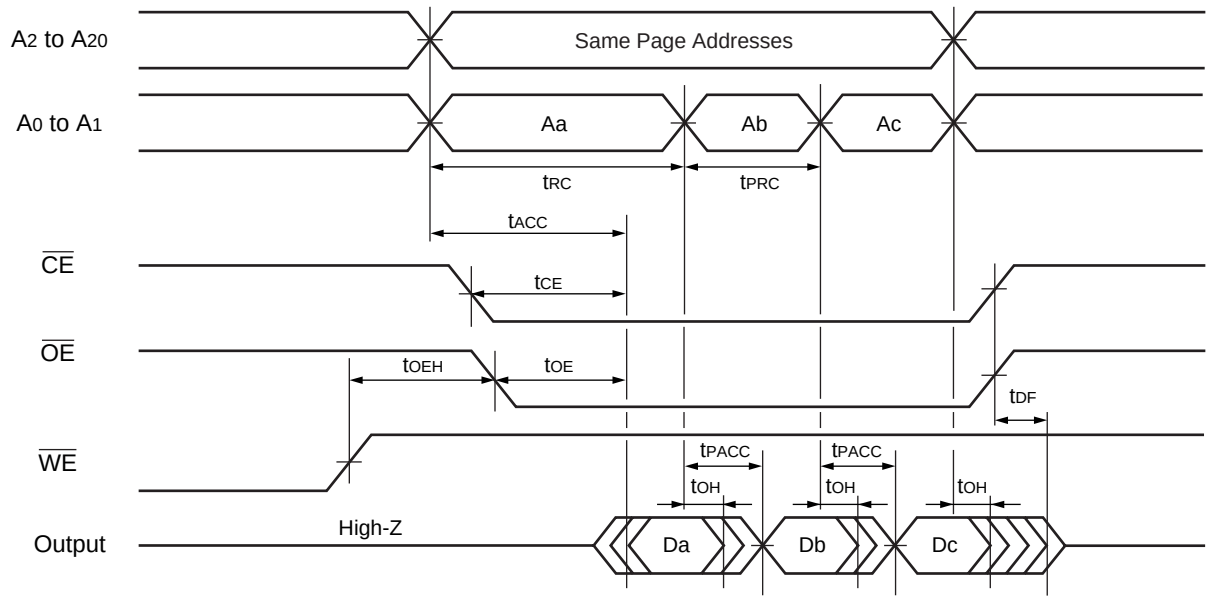
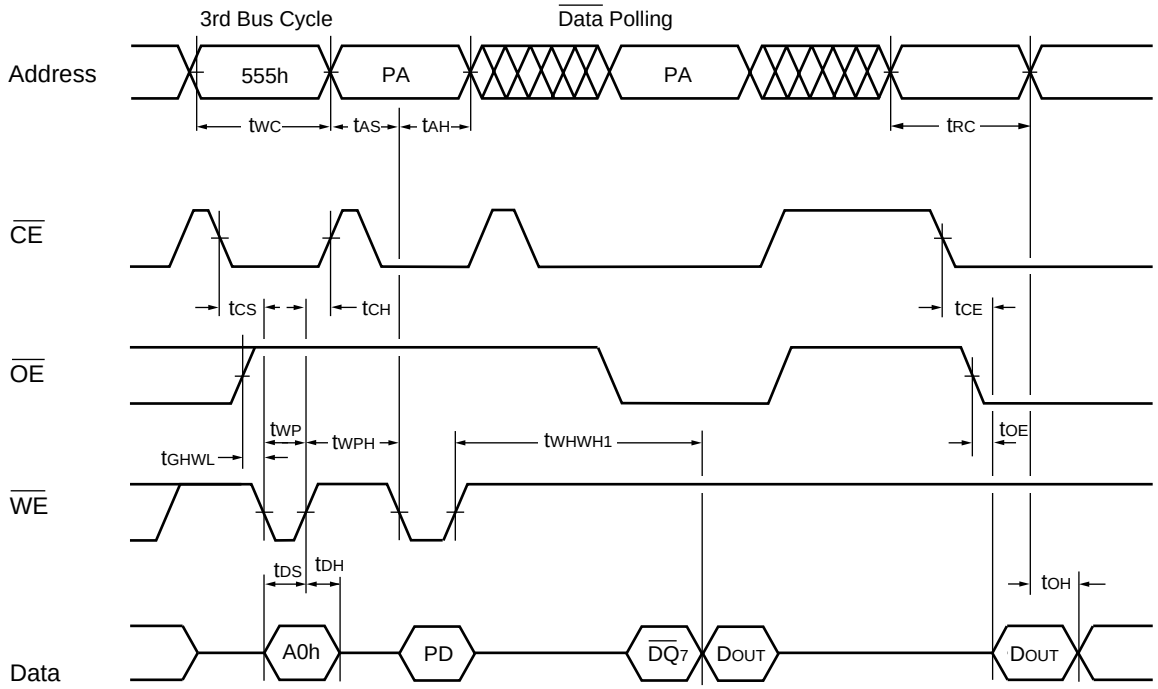
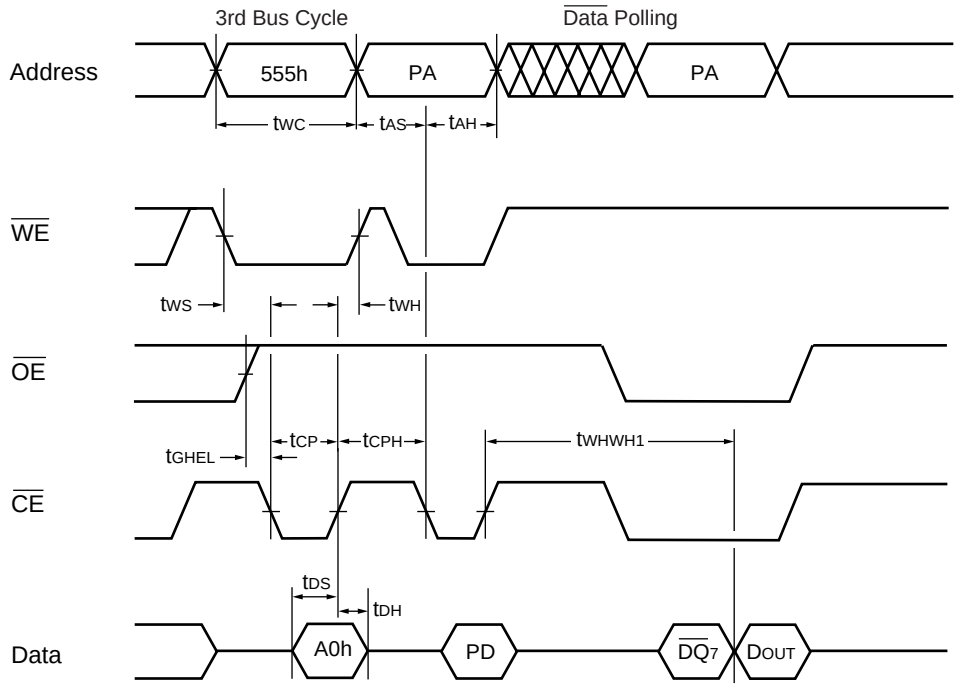



**Figure 5.3 Page Read Operation Timing Diagram**



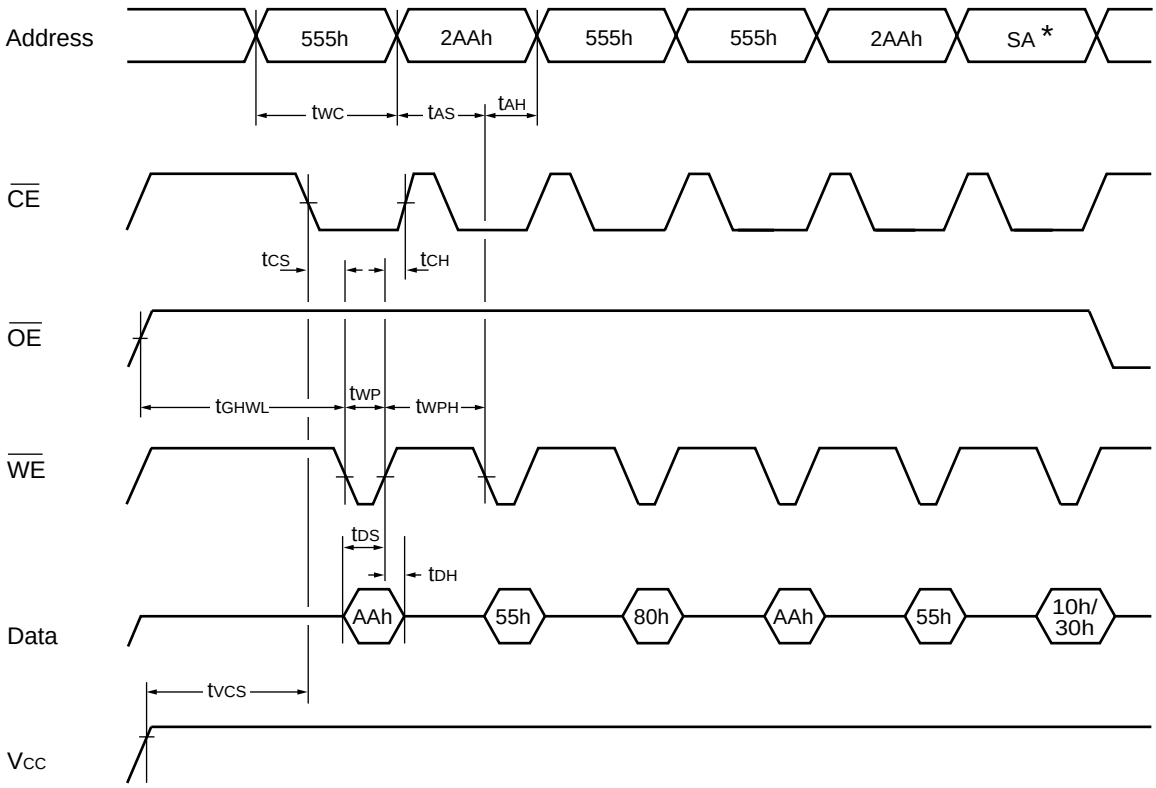

Notes: 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at word address.
3.$\overline{DQ_7}$ is the output of the complement of the data written to the device.
4.$D_{OUT}$ is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.

**Figure 6 Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram**



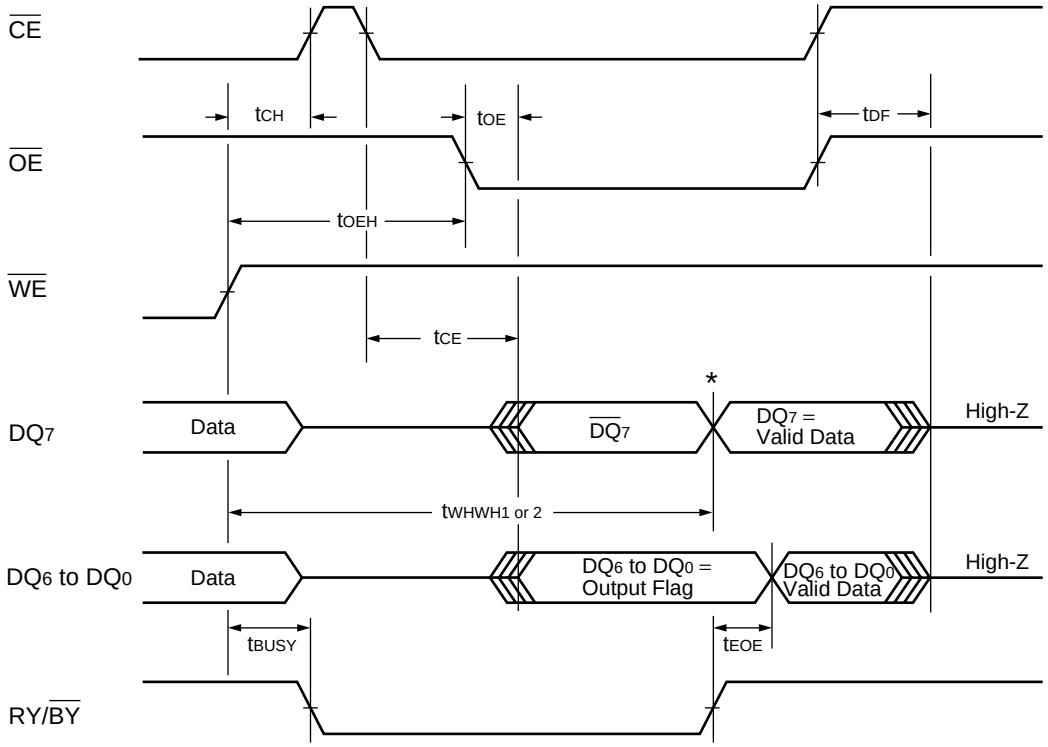

Notes: 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at word address.
3.$\overline{DQ_7}$ is the output of the complement of the data written to the device.
4.$D_{OUT}$ is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.

**Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram**



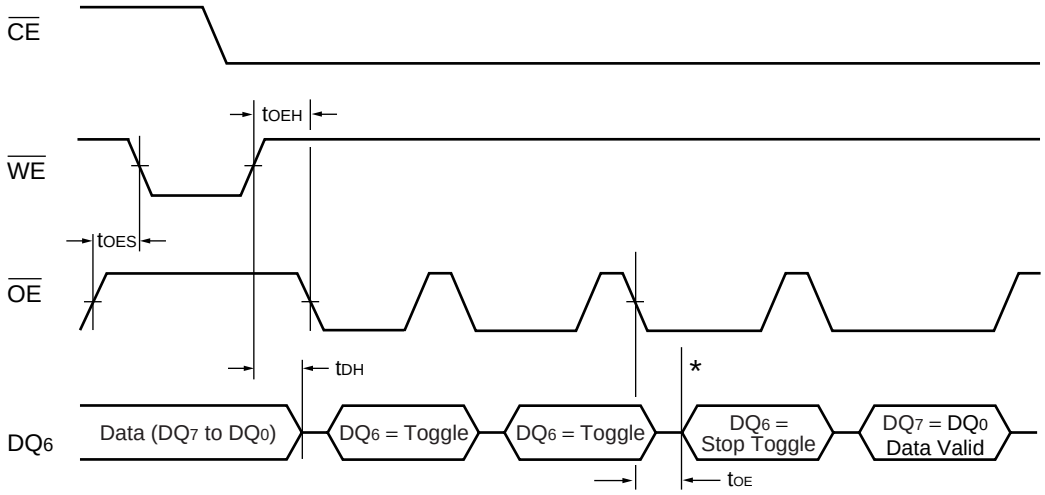

*: SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

**Figure 8 Chip/Sector Erase Operation Timing Diagram**



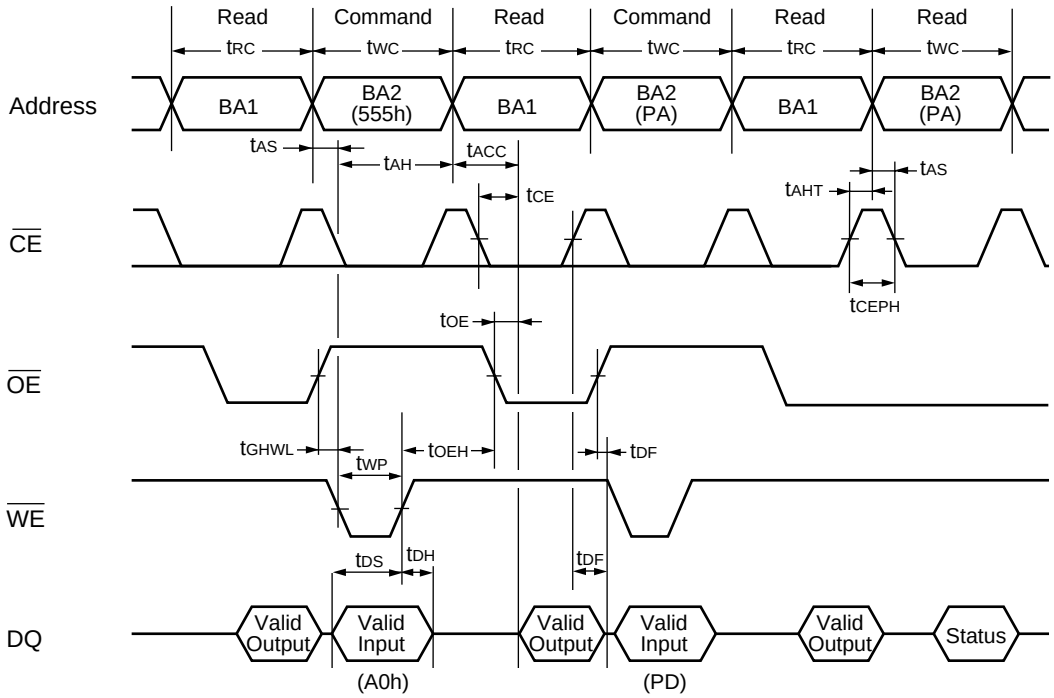

*: $DQ_7$ = Valid Data (The device has completed the Embedded operation).

**Figure 9 $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram**



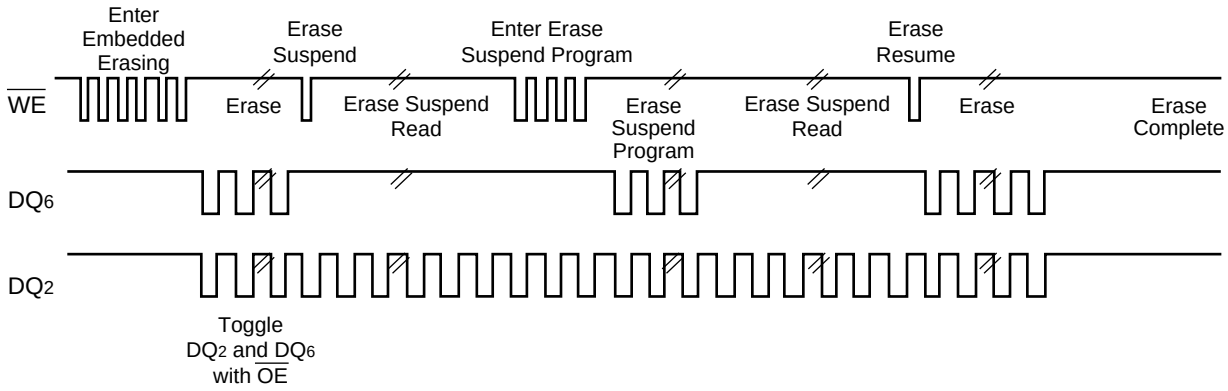

*: $DQ_6$ stops toggling (The device has completed the Embedded operation).

**Figure 10 Toggle Bit I during Embedded Algorithm Operation Timing Diagram**




Note: This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

**Figure 11 Bank-to-Bank Read/Write Timing Diagram**




Note: $DQ_2$ is read from the erase-suspended sector.

**Figure 12 $DQ_2$ vs. $DQ_6$**

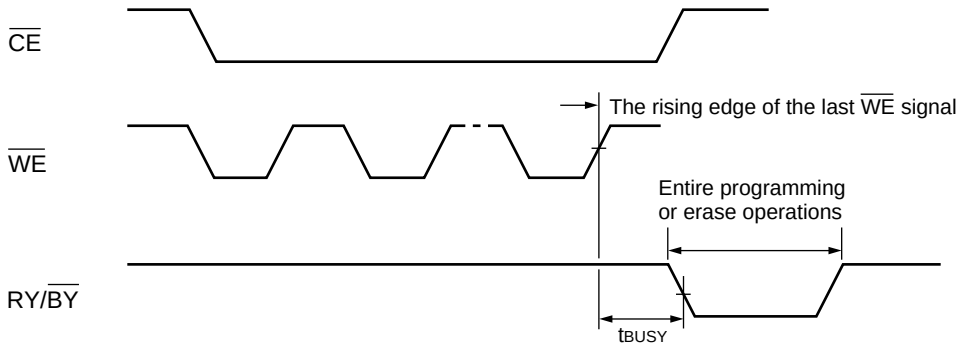



**Figure 13 RY/BY Timing Diagram during Program/Erase Operation Timing Diagram**

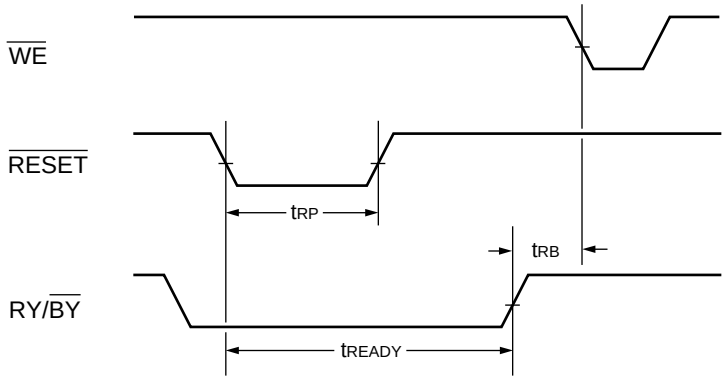



**Figure 14 RESET, RY/BY Timing Diagram**

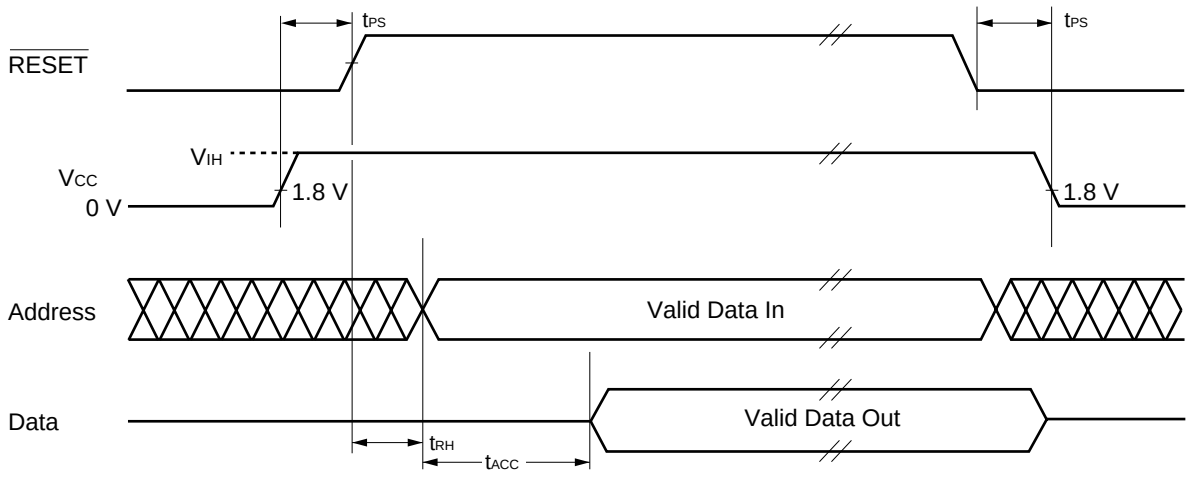
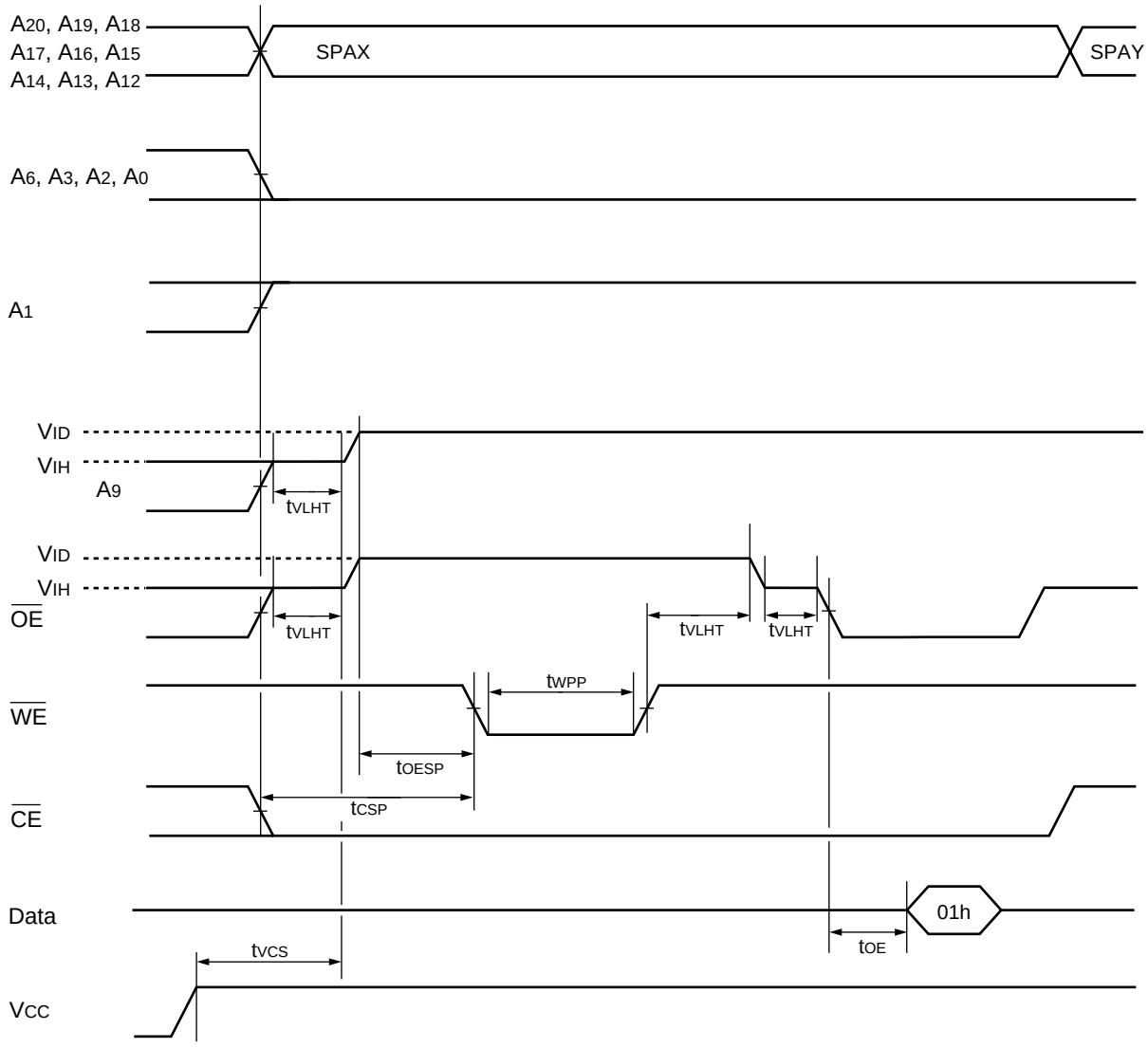



**Figure 15 Power On / Off Timing Diagram**




SPAX: Sector Group Address for initial sector
SPAY: Sector Group Address for next sector

**Figure 16 Sector Group Protection Timing Diagram**

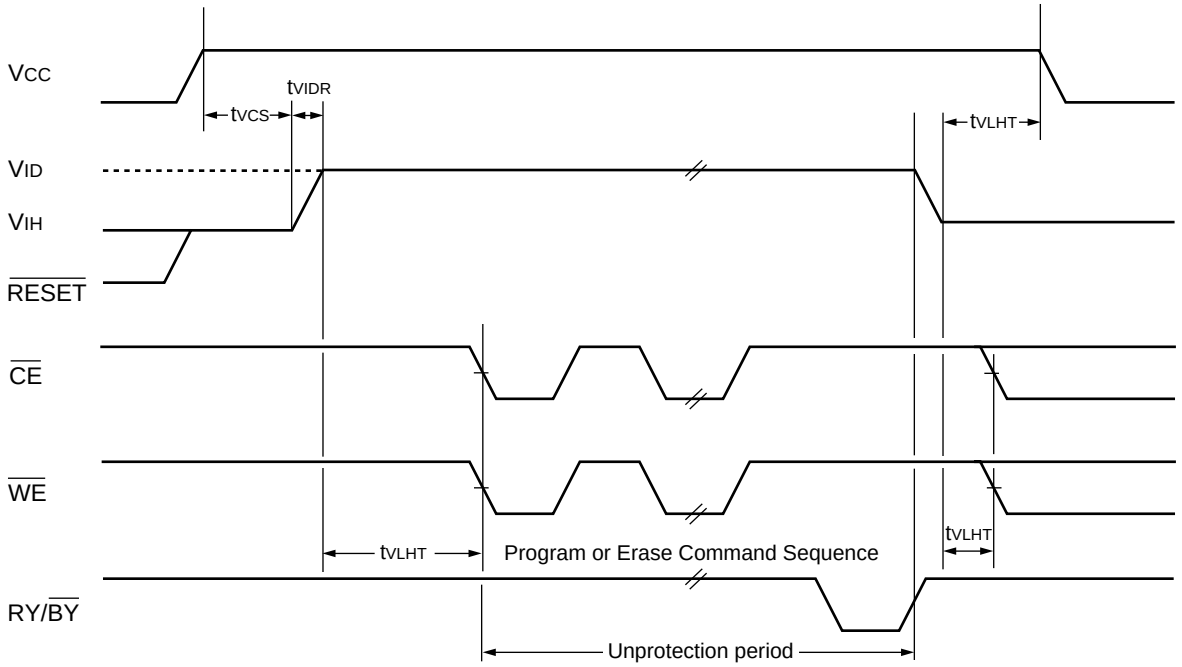
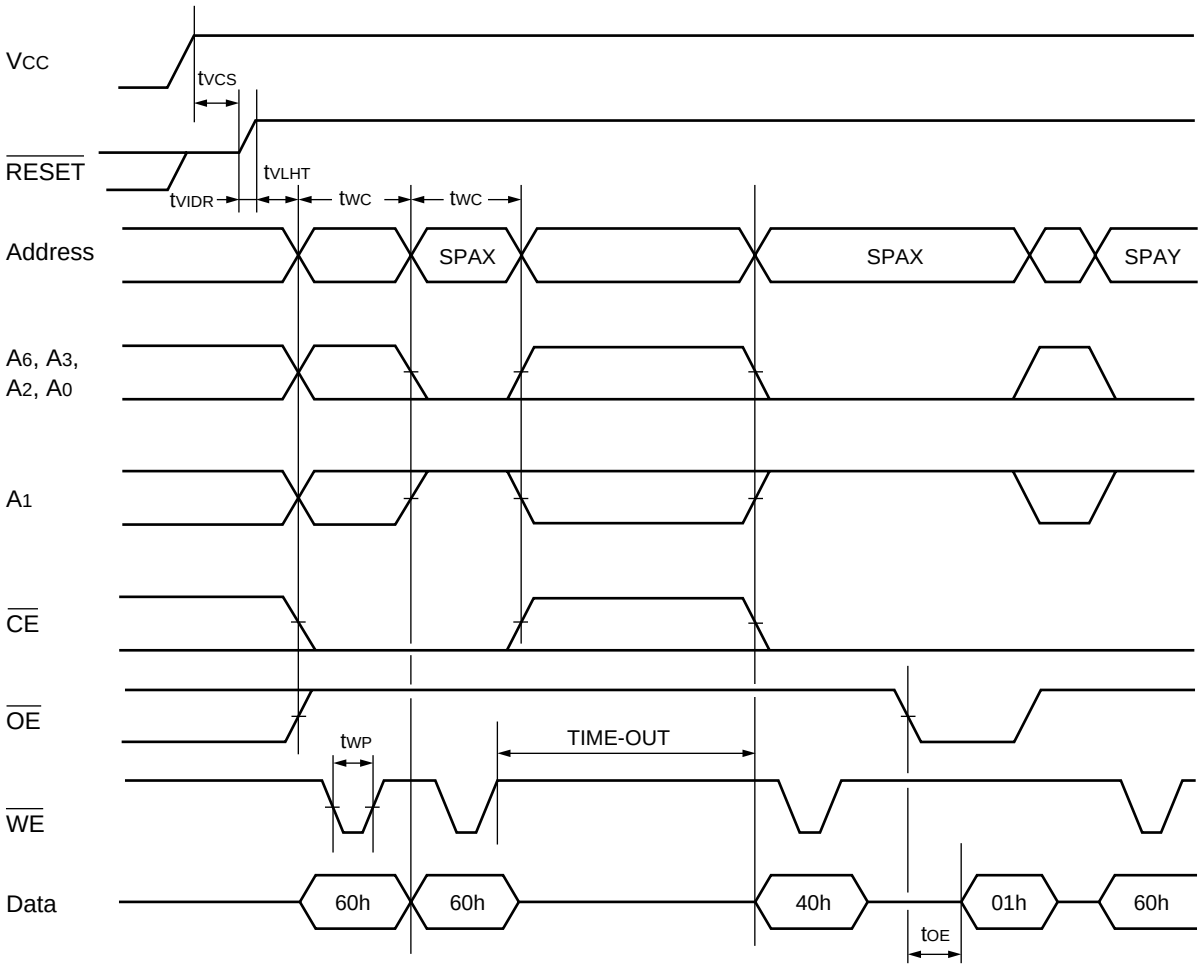



**Figure 17 Temporary Sector Group Unprotection Timing Diagram**




SPAX: Sector Group Address to be protected
SPAY: Next Sector Group Address to be protected
TIME-OUT: Time-Out window = 250 µs (Min.)

**Figure 18 Extended Sector Group Protection Timing Diagram**

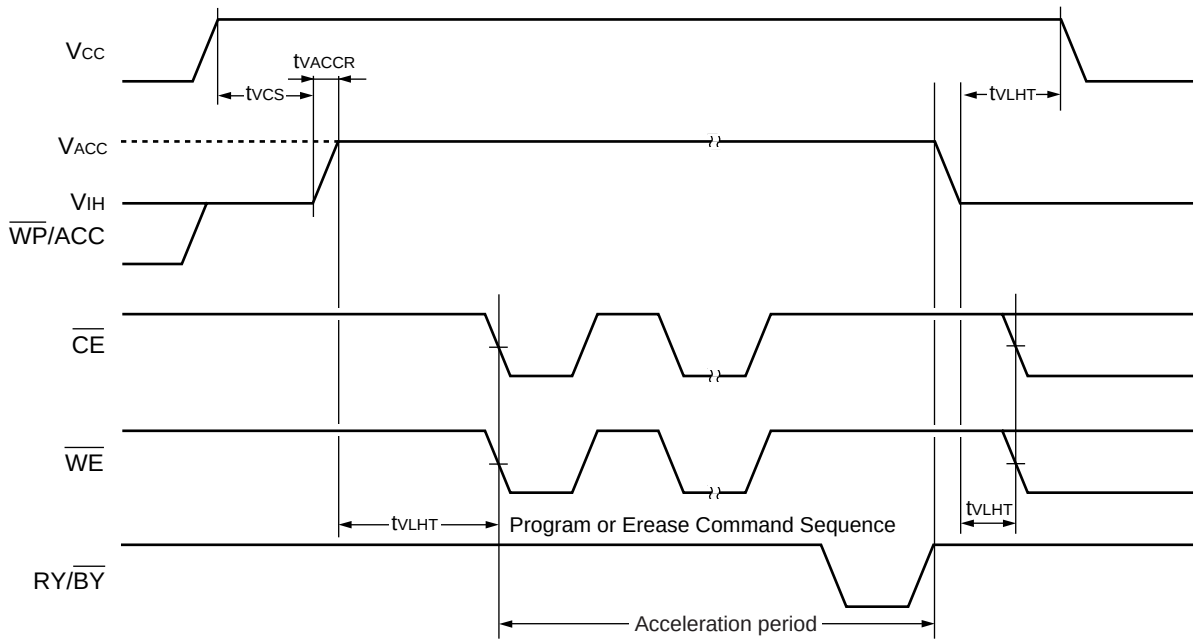
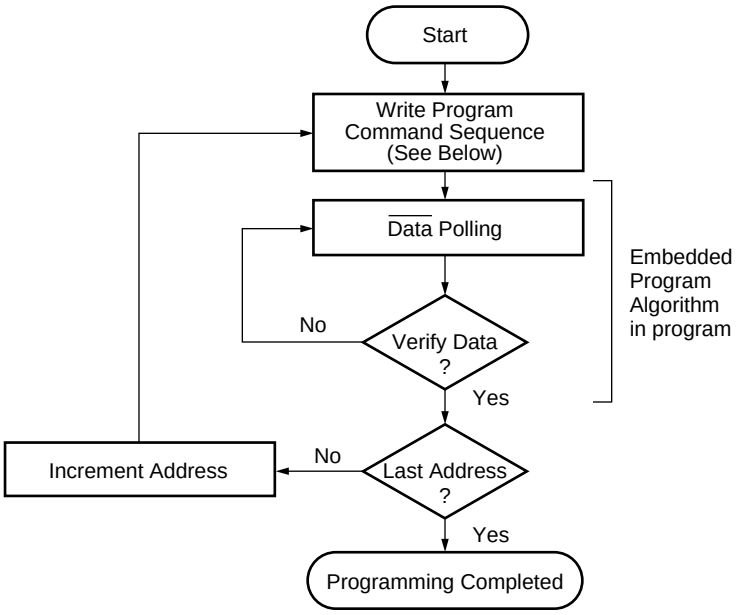



**Figure 19 Accelerated Program Timing Diagram**

## ■ FLOW CHARTS

**EMBEDDED ALGORITHM**




Program Command Sequence (Address/Command):

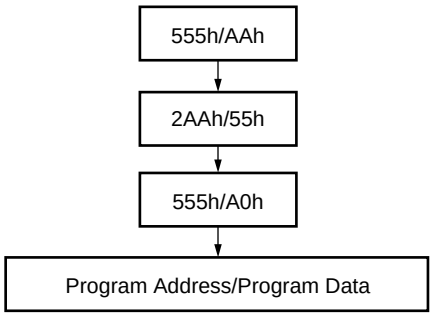



**Figure 20 Embedded Program™ Algorithm**

**EMBEDDED ALGORITHM**

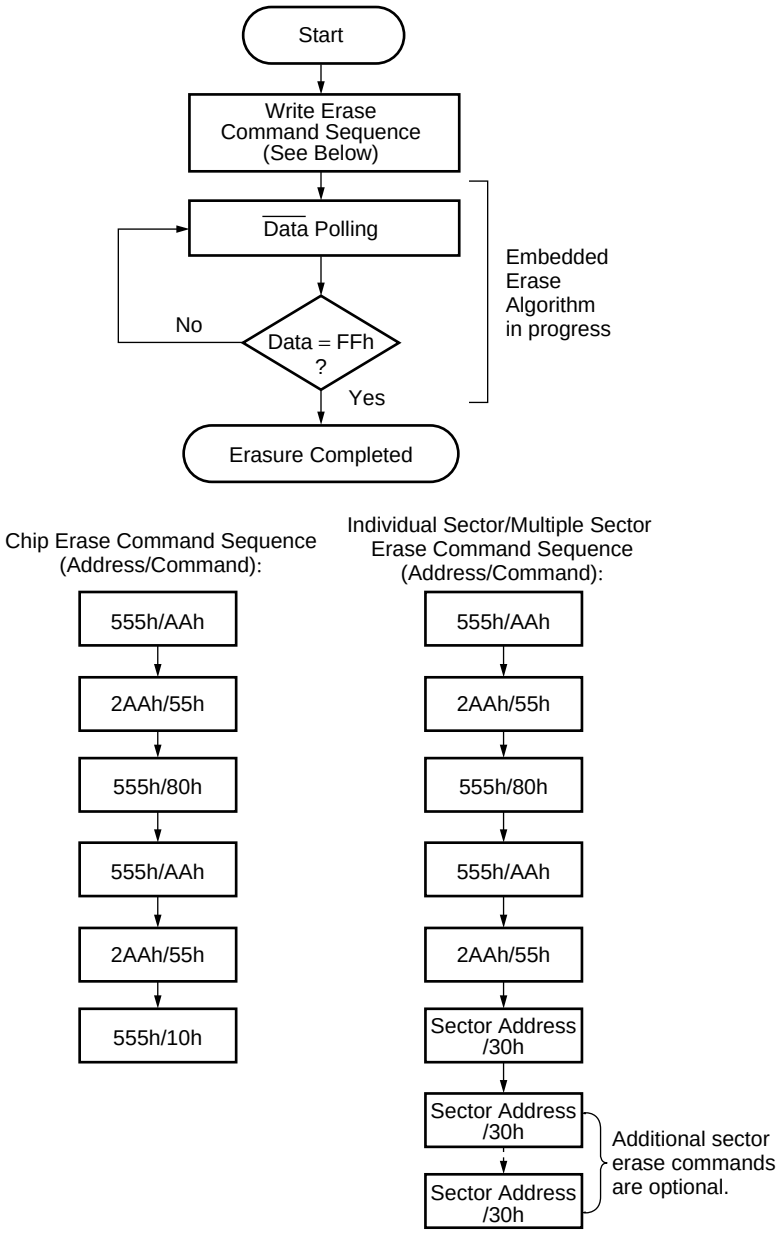
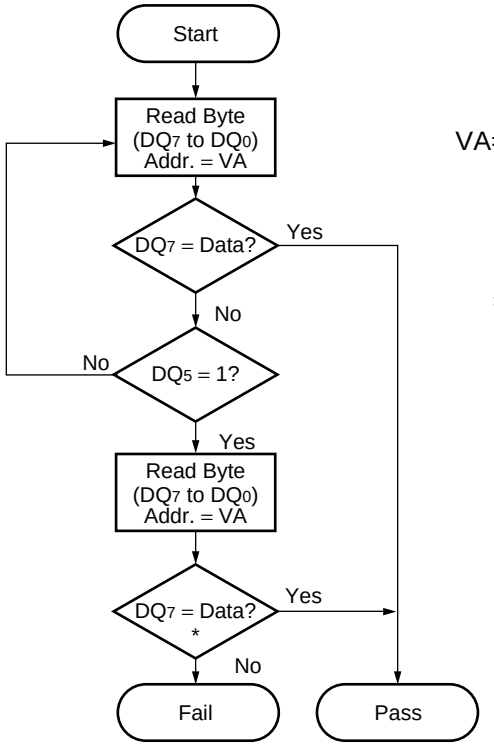


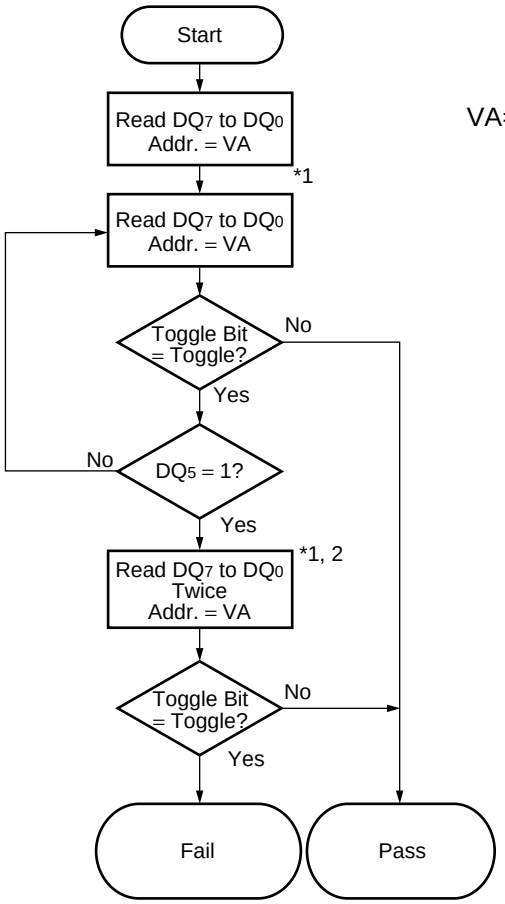

**Figure 21 Embedded Erase™ Algorithm**




VA=Address for programming
=Any of the sector address within the sector being erased during sector erase or multiple sector erases operation
=Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

*: $DQ_7$ is rechecked even if $DQ_5$ = "1" because $DQ_7$ may change simultaneously with $DQ_5$.

**Figure 22 $\overline{\text{Data}}$ Polling Algorithm**




VA=Bank address being executed Embedded Algorithm.

*1: Read toggle bit twice to determine whether or not it is toggling.

*2: Recheck toggle bit because it may stop toggling as $DQ_5$ changes to “1”.

**Figure 23 Toggle Bit Algorithm**

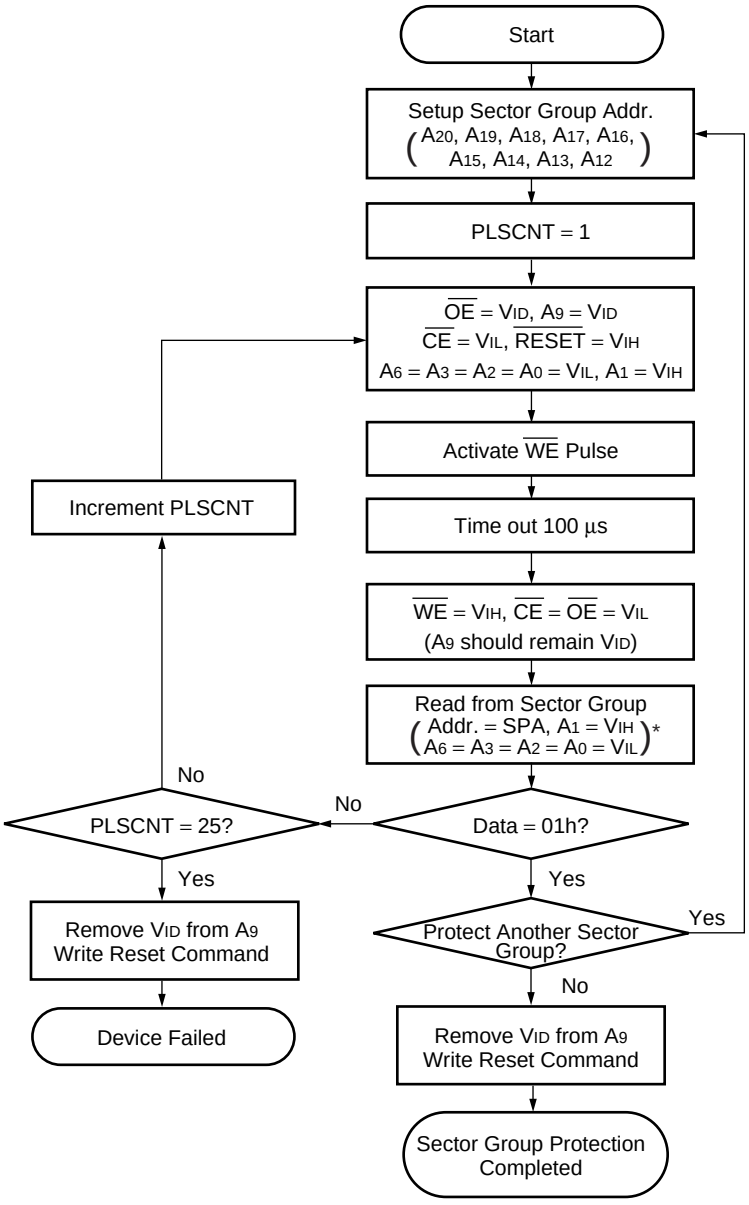
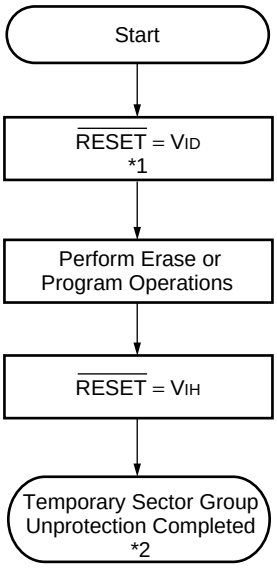



**Figure 24 Sector Group Protection Algorithm**




*1: All protected sector groups are unprotected.

*2: All previously protected sector groups are protected once again.

**Figure 25 Temporary Sector Group Unprotection Algorithm**

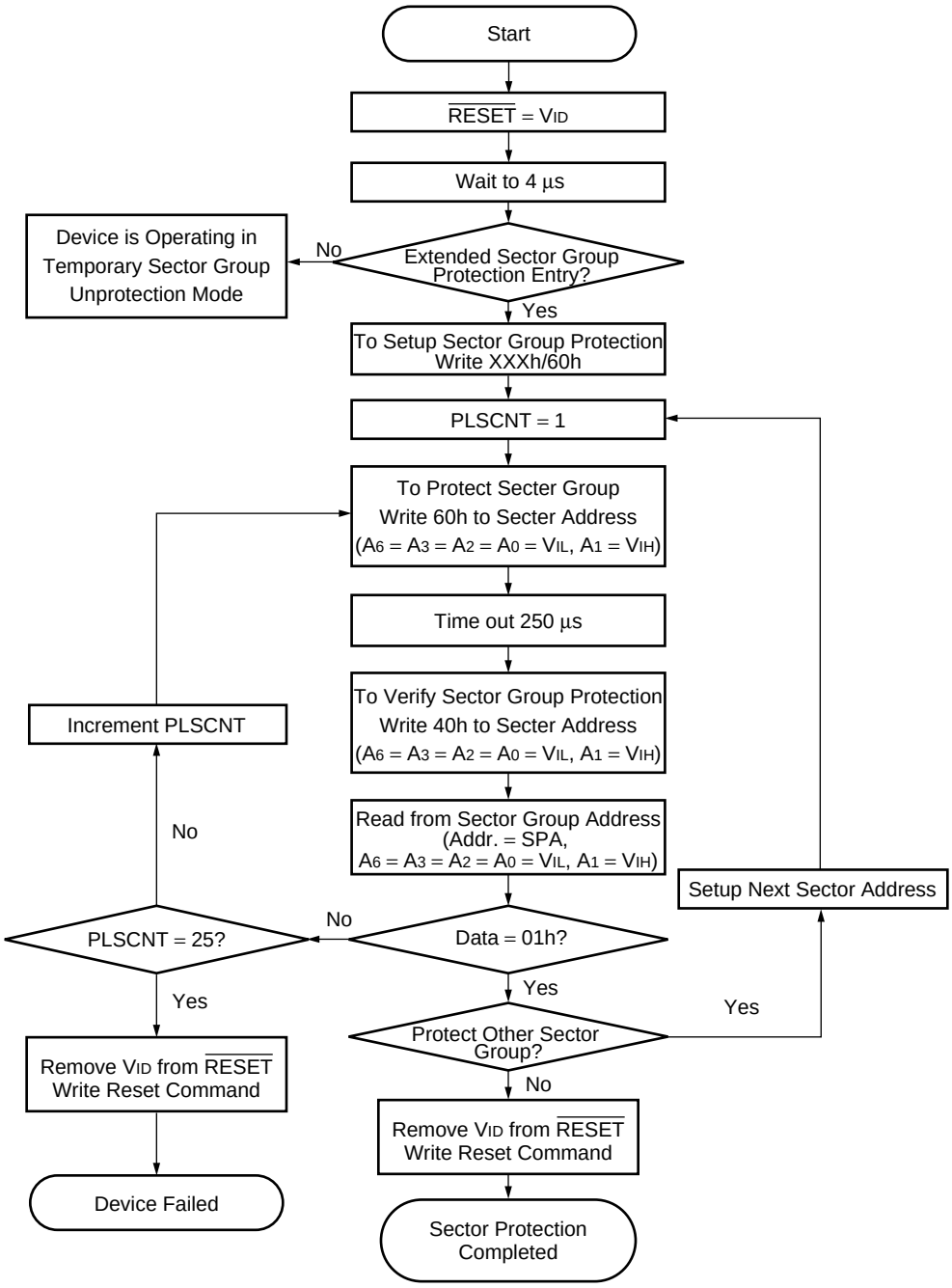



**Figure 26 Extended Sector Group Protection Algorithm**

**FAST MODE ALGORITHM**

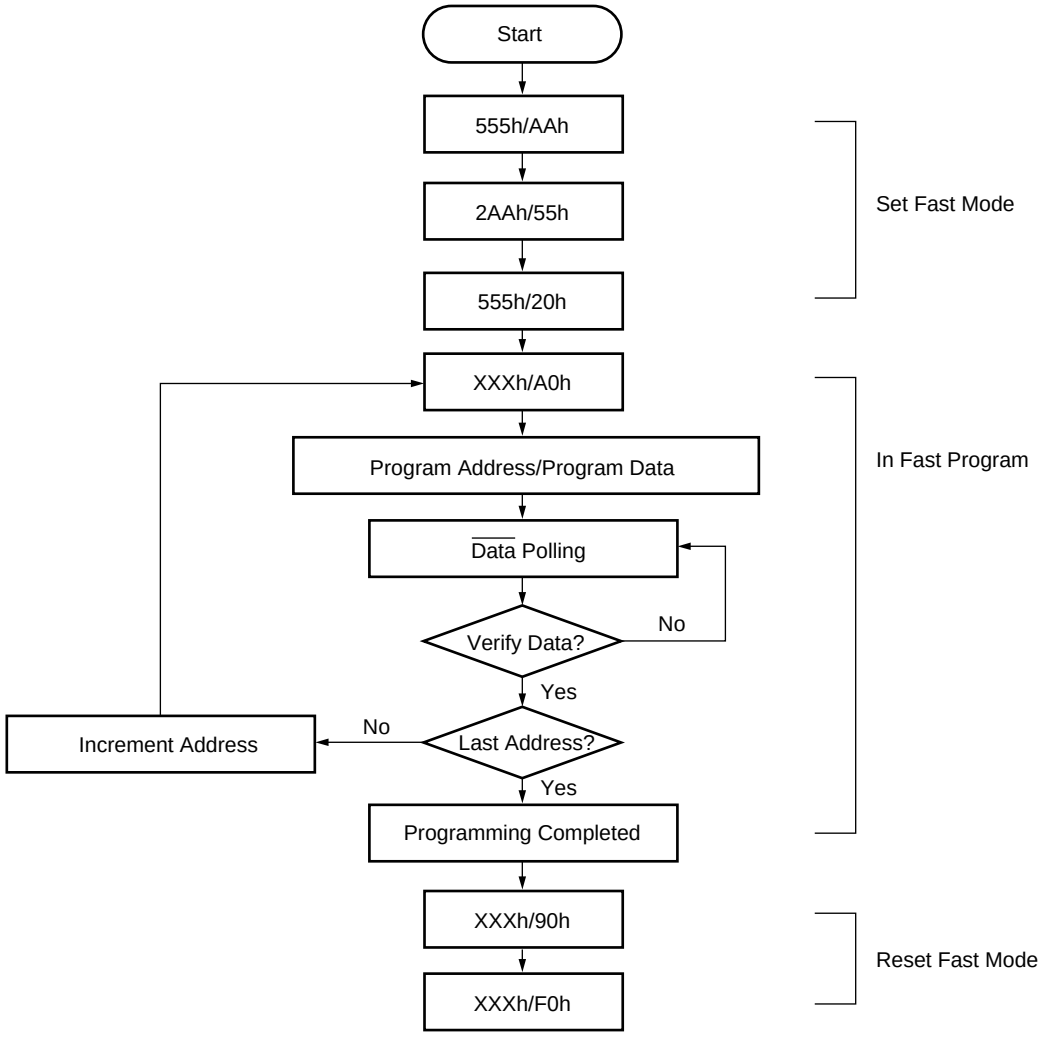
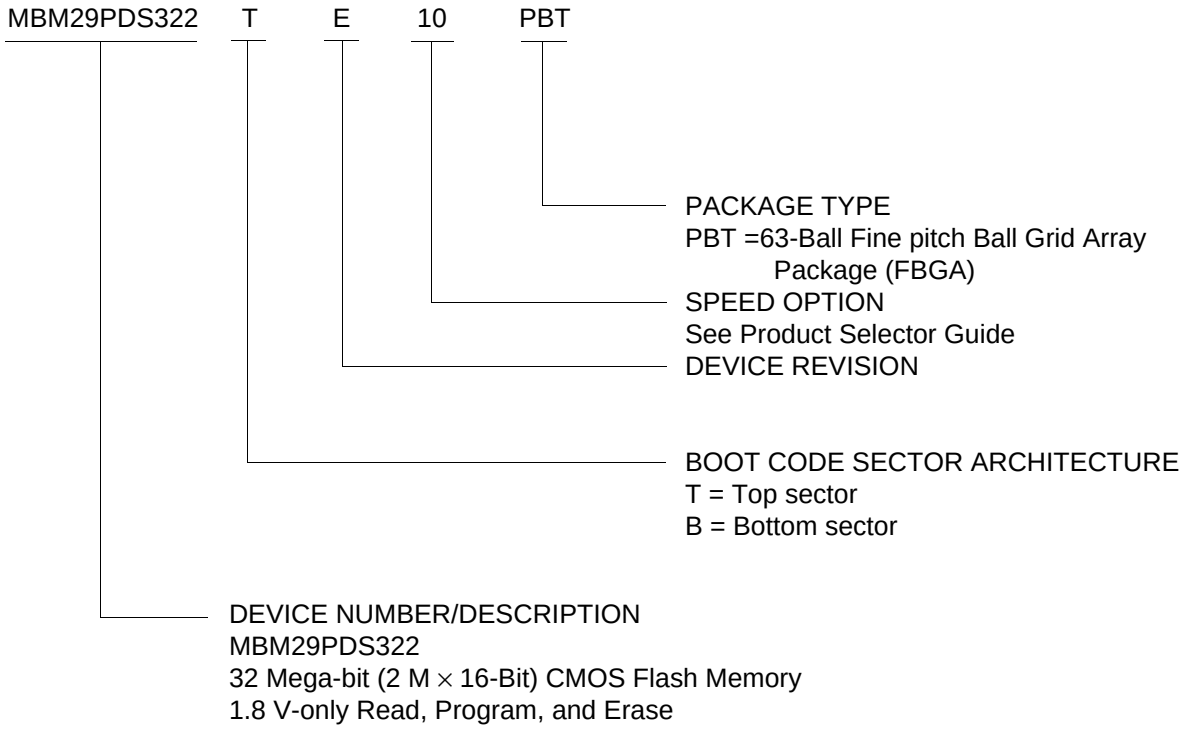



**Figure 27 Embedded Program™ Algorithm for Fast Mode**

## ■ ORDERING INFORMATION

### Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:



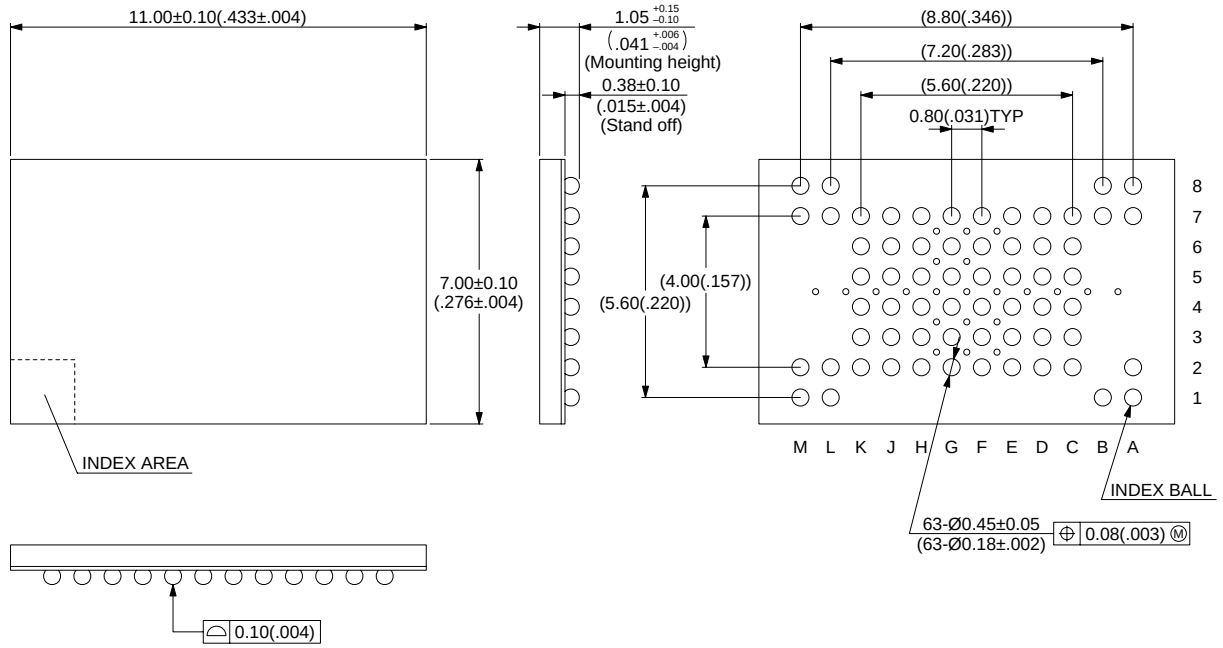

| Valid Combinations | | |
|---|---|---|
| MBM29PDS322TE/BE | 10<br>11 | PBT |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## ■ PACKAGE DIMENSION

63-pin plastic FBGA
(BGA-63P-M01)






Dimensions in mm (inches).

# FUJITSU LIMITED

*For further information please contact:*

**Japan**

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

*http://edevice.fujitsu.com/*

**North and South America**

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
*Mon. - Fri.: 7 am - 5 pm (PST)*
Tel: +1-800-866-8608
Fax: +1-408-922-9179

*http://www.fujitsumicro.com/*

**Europe**

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

*http://www.fujitsu-fme.com/*

**Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

*http://www.fmap.com.sg/*

**Korea**

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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