FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20110-1E

Semicustom

CMOS

Macro embedded type cell array

CE81 Series

■ DESCRIPTION

The CE81 series of 0.18 µm CMOS macro-embedded cell arrays is a line of highly integrated CMOS ASICs featuring high speed and low power consumption at the same time.

This series incorporates up to 34 million gates which have a gate delay time of 12 ps, resulting in both integration and speed about three times higher than conventional products.

In addition, this series can operate at a power-supply voltage of up to 1.1 V, substantially reducing power consumption.

■ FEATURES

- Technology : 0.18 µm silicon-gate CMOS, 3- to 5-layer wiring capable of integrating a mixture of high-speed processes and cells on a single chip (under development)
- Supply voltage : +1.8 V ± 0.15 V (typical) to +1.1 V ± 0.1 V
- Junction temperature range : –40 to +125 °C
- Gate delay time : t_{pd} = 12 ps (1.8 V, inverter, F/O = 1)
- Gate power consumption : 8 nW/MHz/BC (1.1 V, 2-NAND, F/O = 1)
- High-load drive capability : I_{OL} = 2/4/8/12 mA mixable
- Output buffer cells with noise reduction circuits
- Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells
- Buffer cell dedicated to crystal oscillator
- Special interfaces (P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, etc. under development)
- IP macros (CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, etc. under development)
- Capable of incorporating compiled cells (RAM/ROM/multiplier, etc.)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using a timing driven layout tool
- Support for static timing sign-off
  Dramatically reducing the time for generating test vectors for timing verification and the simulation time
- Hierarchical design environment for supporting large-scale circuits
- Simulation (before layout) considering the input slew rate and detailed RC delay calculation (after layout) , supporting development with minimized timing trouble after trial manufacture
- Support for memory (RAM/ROM) SCAN
- Support for memory (RAM) BIST
- Support for boundary SCAN

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- Support for path delay test
- A variety of package options
  (TQFP, HQFP, EBGA, FBGA, TAB-BGA, FCBGA)

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells (about 800 types)

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- SCAN Flip Flop
- ENOR
- AND-OR
- Decoder
- Non-SCAN Flip Flop
- Inverter
- Buffer
- OR-AND Inverter
- OR
- Selector
- BUS Driver
- EOR
- Others

2. IP macros

CPU/DSP	FR, SPARClite, standard CPU (under preparation) Communications DSP, DSP for AV
Interface macro	PCI, IEEE1394, USB, IrDA, etc.
Multimedia processing macros	JPEG, MPEG, etc.
Mixed signal macros	ADC, DAC, OPAMP, etc.
Compiled macros	RAM, ROM, multiplier, adder, multiplier-accumulator, etc.
PLL	Analog PLL, digital PLL

3. Special I/O interface macros

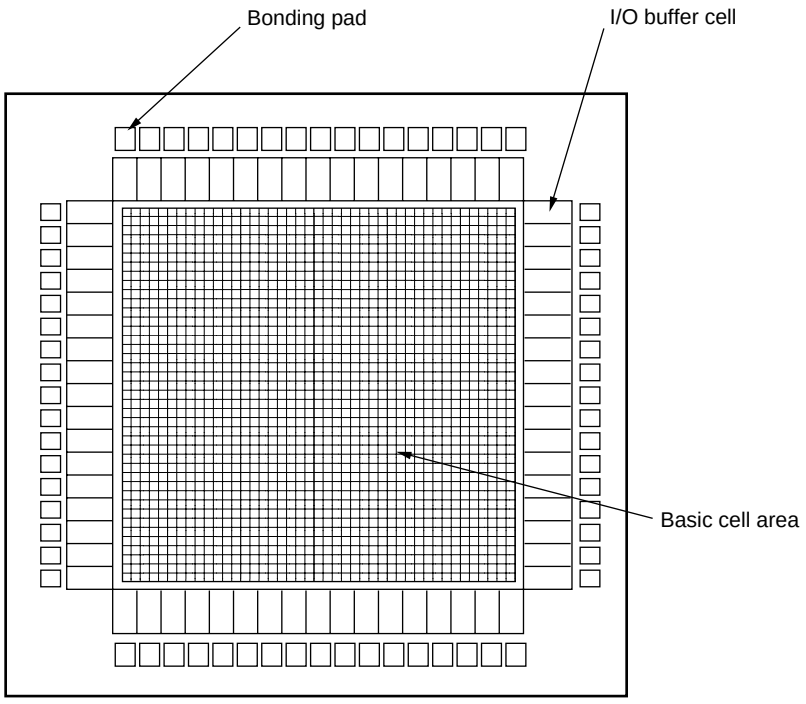
- T-LVTTL
- LVDS
- IEEE1394
- SSTL
- PCI
- HSTL
- AGP
- P-CML
- USB

■ CHIP STRUCTURE

The chip layout of the CE81 series consists of two major areas : chip peripheral area and basic cell area.

The chip peripheral area contains the input/output buffer cells for interfacing with external devices and the associated bonding pads. The basic cell area contains some of input/output buffer cells, the unit cells and the compiled cells.

- Chip configuration



■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CE81 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address, 1 RW)

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	Bit
16	64 to 72 K	64 to 4 K	1 to 18	Bit

2. Clock synchronous dual-port RAM (2 addresses, 1 RW/1 R)

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	Bit
16	64 to 72 K	64 to 4 K	1 to 18	Bit

3. Clock synchronous ROM

Column type	Memory capacity	Word range	Bit range	Unit
8	128 to 512 K	32 to 4 K	4 to 128	Bit
16	128 to 512 K	64 to 8 K	2 to 64	Bit

■ HIGH-CAPACITY MEMORY

• Clock synchronous single port RAM (1 address, 1 RW)

Column type	Memory capacity	Word range	Bit range	Unit
Under development				

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Application	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{DD}	V_{DD}, V_{DDI} (Internal)	V_{SS} – 0.5	+2.5	V
		V_{DDE} (External)	V_{SS} – 0.5	+4.0	V
Input voltage*1	V_I	1.8 V input pin	V_{SS} – 0.5	V_{DDI} + 0.5 (≤ 2.5 V)	V
		3.3 V input pin	V_{SS} – 0.5	V_{DDE} + 0.5 (≤ 4.0 V)	V
Output voltage	V_O	1.8 V output pin	V_{SS} – 0.5	V_{DDI} + 0.5 (≤ 2.5 V)	V
		3.3 V output pin	V_{SS} – 0.5	V_{DDE} + 0.5 (≤ 4.0 V)	V
Storage temperature	T_{ST}	Plastic package	–55	+125	°C
Power-supply pin current *2	I_D	Per V_{DD}/V_{DDI}/V_{DDE} pin	—	TBD	mA
		Per V_{SS} pin	—	TBD	mA
Output current*3	I_O	L type output buffer I_{OL} = 2 mA	—	±13	mA
		M type output buffer I_{OL} = 4 mA	—	±13	mA
		H type output buffer I_{OL} = 8 mA	—	±13	mA
		V type output buffer I_{OL} = 12 mA	—	±26	mA

*1 : Do not apply any voltage of 1.1 V or more between the LVDS (resistor built-in type) differential inputs.

*2 : Maximum supply current which can be supplied constantly.

*3 : Maximum output current which can be supplied constantly. Exceeding the rating is allowed only within 1 second for only one LSI pin. The maximum rating of the P-CML output buffer is 20 mA.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING TEMPERATURE

- **Single power supply (V_{DD} = +1.8 V ± 0.15 V)**

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage (1.8 V supply voltage)	V_{DD}	1.65	1.8	1.95	V
"H" level input voltage (1.8 V CMOS level)	V_{IH}	$V_{DD} \times 0.65$	—	$V_{DD} + 0.3$	V
"L" level input voltage (1.8 V CMOS level)	V_{IL}	–0.3	—	$V_{DD} \times 0.35$	V
Operating junction temperature	T_j	–40	—	+125	°C

- **Dual power supply (V_{DDI} = +1.8 V ± 0.15 V, V_{DDE} = +3.3 V ± 0.3 V)**

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	1.8 V supply voltage	V_{DDI}	1.65	1.8	1.95	V
	3.3 V supply voltage	V_{DDE}	3.0	3.3	3.6	
"H" level input voltage	1.8 V CMOS level	V_{IH}	$V_{DD} \times 0.65$	—	$V_{DDI} + 0.3$	V
	3.3 V CMOS level		2.0	—	$V_{DDE} + 0.3$	
"L" level input voltage	1.8 V CMOS level	V_{IL}	–0.3	—	$V_{DD} \times 0.35$	V
	3.3 V CMOS level		–0.3	—	0.8	
Operating junction temperature		T_j	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

- **Single power supply : V_{DD} = 1.8 V**

(V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	I_{DDS}	Static state*1, *2		—	—	TBD	mA
"H" level output voltage	V_{OH}	I_{OH} = –100 µA		V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = –100 µA		V_{DDE} – 0.2	—	V_{DDE}	V
"H" level output current	I_{OH}	Output pin $V_{OH} = V_{DD}$ – 0.2 V	L type	—	—	–1.0	mA
			M type			–2.0	
			H type			–4.0	
			V type			–6.0	
"L" level output current	I_{OL}	Output pin V_{OL} = 0.2 V	L type	1.0	—	—	mA
			M type	2.0			
			H type	4.0			
			V type	6.0			
Output short-circuit current*3	I_{OS1}	L type		—	—	TBD	mA
		M type					
		H type					
		V type					
Input leak current*4	I_{LI}	Input pin		—	—	5	µA
	I_{LZ}	Tristate pin (for input)		—	—	5	
Input pull-up/pull-down resistance*5	R_P	Pull-up V_I = 0 Pull-down $V_I = V_{DD}$		TBD	18	TBD	kΩ

*1 : When the memory macro is in standby mode and analog macro is in power-down mode. At both case, conditions are $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, and T_j = +25 °C.

*2 : The above value may not be guaranteed when the input/output buffer with pull-up/pull-down resistor or crystal oscillator buffer is used.

*3 : The maximum current which flows when the output pin is shorted to V_{DD} or V_{SS}. Keep the output short-circuit current below the maximum rating.

*4 : The input leakage current may exceed the above value when the input buffer with pull-up/pull-down resistor is used.

*5 : Input pull-up/pull-down is optional in input and bidirectional buffers.

- **Dual power supply : V_{DDI} = 1.8 V and V_{DDE} = 3.3 V**

(V_{DDI} = 1.8 V ± 0.15 V, V_{DDE} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	I_{DDS}	Static state[*1, *2]		—	—	TBD	mA
"H" level output voltage	V_{OH}	3.3 V Output pin I_{OH} = –100 µA		V_{DDE} – 0.2	—	V_{DDE}	V
		1.8 V Output pin I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL}	I_{OL} = –100 µA		V_{DDE} – 0.2	—	V_{DDE}	V
"H" level output current	I_{OH}	3.3 V Output pin V_{OH} = V_{DDE} – 0.4 V	L type	—	—	–2.0	mA
			M type			–4.0	
			H type			–8.0	
			V type			–12.0	
		1.8 V Output pin V_{OH} = V_{DDI} – 0.2 V	L type	—	—	–1.0	mA
			M type			–2.0	
			H type			–3.0	
			V type			–6.0	
"L" level output current	I_{OL}	3.3 V Output pin V_{OL} = 0.4 V	L type	2.0	—	—	mA
			M type	4.0			
			H type	8.0			
			V type	12.0			
		1.8 V Output pin V_{OL} = 0.2 V	L type	1.0	—	—	mA
			M type	2.0			
			H type	4.0			
			V type	6.0			
Output short-circuit current[*3]	I_{OSI}	Output pin V_O = 0 V or V_{DD}	L type	—	—	TBD	mA
			M type				
			H type				
			V type				
Input leak current[*4]	I_{LI}	Input pin		—	—	5	µA
	I_{LZ}	Tristate pin (for input)		—	—	5	
Input pull-up/pull-down resistance[*5]	R_P	1.8 V I/O buffer Pull-up V_I = 0 Pull-down V_I = V_{DDI}		TBD	18	TBD	kΩ
		3.3 V I/O buffer Pull-up V_I = 0 Pull-down V_I = V_{DDE}		10	33	60	

*1 : When the memory macro is in standby mode and analog macro is in power-down mode. At both case, conditions are $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, and $T_j = +25$ °C.

*2 : The above value may not be guaranteed when the input/output buffer with pull-up/pull-down resistor or crystal oscillator buffer is used.

*3 : The maximum current which flows when the output pin is shorted to V_{DD} or V_{SS}. Keep the output short-circuit current below the maximum rating.

*4 : The input leakage current may exceed the above value when the input buffer with pull-up/pull-down resistor is used.

*5 : Input pull-up/pull-down is optional in input and bidirectional buffers.

2. AC Characteristics

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Delay time	t_{pd}*1	typ*2 × m (TBD)	typ*2 × n (TBD)	ns

*1 : Delay time = propagation delay time, Enable time, Disable time

*2 : “typ” is calculated from the cell specification.

■ INPUT/OUTPUT CAPACITANCE

(f = 1 MHz, $V_{DD} = V_I$ = 0 V, Ta = 25 °C)

Parameter	Symbol	Value	Unit
Input pin	C_{IN}	Max.16	pF
Output pin	C_{OUT}	Max.16	pF
Input/output capacitance	$C_{I/O}$	Max.16	pF

■ DESIGN METHOD

Linking a floor plan tool and a logic synthesis tool enables automatic circuit optimization using floor plan information. In addition, also available are CDDM (Clock Driven Design Method) clock tree synthesis tools using floor plan information. Using floor plan information at a pre-layout stage prevents major problems with setup and hold timings which can occur after layout. Using a hierarchical layout method to support larger-scale circuit design considerably shortens the overall design cycle time.

■ SUPPORT TOOLS

- Simulation
  Synopsys, Inc. : VSS, VCS
  Cadence Design Systems, Inc. : Verilog-XL, NC-Verilog, Leapfrog
  Model Technology, Inc. : V-System
  FUJITSU LIMITED : LCADFE
- Logic synthesis
  Synopsys, Inc. : DesignCompiler
- Floor plan
  FUJITSU LIMITED : GLOSCAD
- Clock tree
  FUJITSU LIMITED : OPTING
- Timing analysis
  Synopsys, Inc. : PrimeTime
  FUJITSU LIMITED : GISTA
- Power calculation
  Sente, Inc. : Watt Watcher
  Synopsys, Inc. : DesignPower, PowerCompiler
  FUJITSU LIMITED : PScope, SilicoScope IRD
- Layout
  Cadence Design Systems, Inc. : Gate Ensemble DSM
  FUJITSU LIMITED : GLOSCAD
- Test tools
  FUJITSU LIMITED : ATREX, FANTCAD, RAPARA, TERBAN, FANSCAD
- Format verification
  Chrysalis Symbolic Design, Inc. : Design VERIFYer
- Verification tool
  Cadence Design Systems, Inc. : Dracula
- Design environment tool
  FUJITSU LIMITED : METRO/IPSymphony
- HW/SW co-simulation
  Synopsys, Inc. : EAGLE-i
  Yokogawa Electric Corporation : VIRTUAL-ICE
  GAIO Technology Co. LTD. : Asim-G

■ PACKAGES

The table below lists the package types available and the reference number of gates used.

Consult Fujitsu for the combination of each package and the availability.

- Number of gates used and package types

Package and pin count		CAVITY	pin pitch	material	Usable gate numbers (0 2000K 4000K 6000K 8000K 10000K 12000K 14000K 16000K)
TBGA	304	DOWN	0.80 mm/4 rows	●	833 K
	352	DOWN	0.80 mm/4 rows	●	1186 K
	480	DOWN	1.00 mm/5 rows	●	1819 K
	560	DOWN	1.00 mm/5 rows	●	2586 K
	660	DOWN	1.00 mm/5 rows	●	3489 K
	720	DOWN	1.00 mm/6 rows	●	8938 K
EBGA	576	DOWN	Ñ	●	6053 K
	672	DOWN		●	8033 K
HQFP	208	UP	0.50 mm	●	1115 K
	240	UP	0.50 mm	●	2106 K
	304	UP	0.50 mm	●	15406 K
	256	UP	0.40 mm	●	3790 K
TQFP	100	UP	Ñ	●	527 K
	120	UP		●	527 K
LQFP	144	UP	Ñ	●	527 K
	176	UP		●	735 K
	208	UP		●	1115 K
FBGA	112	UP	0.80 mm	●	527 K
	144	UP	0.80 mm	●	527 K
	168	UP	0.80 mm	●	735 K
	176	UP	0.80 mm	●	735 K
	192	UP	0.80 mm	●	1115 K
	224	UP	0.80 mm	●	1573 K
	272	UP	0.80 mm	●	2724 K
	320	UP	0.80 mm	●	2724 K
	288	UP	0.75 mm	●	4745 K
	240	UP	0.50 mm	●	2724 K
	304	UP	0.50 mm	●	4745 K
	368	UP	0.50 mm	●	4745 K
FCBGA	1089	DOWN	1.27 mm	●	TBD
	1225	DOWN	1.27 mm	●	
	1369	DOWN	1.27 mm	●	
	1681	DOWN	1.00 mm	●	
	1849	DOWN	1.00 mm	●	
	2116	DOWN	1.00 mm	●	

Note : This list contains packages under planning.

● : Plastic

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: 81(44) 754-3763
Fax: 81(44) 754-3329

http://www.fujitsu.co.jp/

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

http://www.fujitsumicro.com/

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

http://www.fujitsu-ede.com/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

http://www.fmap.com.sg/

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