PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

PE4243

SPDT MOSFET RF Switch

Features

- Single-pin or complementary CMOS logic control inputs
- +3.0-volt power supply needed for single-pin control mode
- Low insertion loss: 0.7 dB at 1.0 GHz, 0.9 dB at 2.0 GHz
- Isolation of 30 dB at 1.0 GHz, 21 dB at 2.0 GHz
- Typical 1 dB compression point of +27 dBm
- Ultra-small SOT23 package

Product Description

The PE4243 MOSFET RF Switch is designed to cover a broad range of applications from DC through 3.0 GHz. This switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a 1 dB compression point of +27 dBm can be achieved.

The PE4243 MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

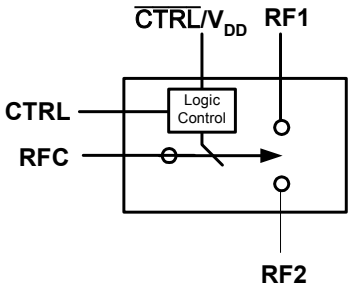


Figure 2. Package Type

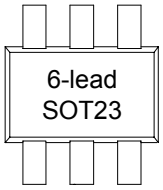


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		3000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.7 0.9	0.85 1.05	dB dB
Isolation	1000 MHz 2000 MHz	28 19	30 21		dB dB
Return Loss	1000 MHz 2000 MHz	18 16	22 19		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB of final value, 1 GHz		300		ns
'OFF' Switching Time	50% CTRL to 25 dB isolation, 1 GHz		200		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	2000 MHz	26	27		dBm
Input IP3	2000 MHz, 14 dBm input power	43	45		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Figure 3. Pin Configuration

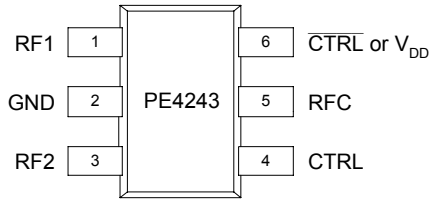


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF1 port (Note 1)
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF2 port (Note 1)
4	CTRL	Switch control input, CMOS logic level.
5	RFC	Common RF port for switch (Note 1)
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options: 1) *Single-pin control mode*. A nominal 3-volt supply connection is required. 2) *Complementary-pin control mode*. A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

Note 1: All RF pins must be DC blocked with an external series capacitor or held at $0V_{DC}$.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		30	dBm
V_{ESD}	ESD voltage (Human Body Model)		1500	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		250	500	nA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 = V_{DD} CTRL = Low	RFC to RF1
Pin 6 = V_{DD} CTRL = High	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
$\overline{\text{CTRL}}$ = High CTRL = Low	RFC to RF1
$\overline{\text{CTRL}}$ = Low CTRL = High	RFC to RF2

Control Logic Input

The PE4243 is a very versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CNTL and $\overline{\text{CNTL}}$ (pins 4 & 6), that can be directly driven by +3-volt CMOS logic or a suitable μProcessor I/O port. This enables the PE4243 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4243 operating limits.

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss – RFC to RF1

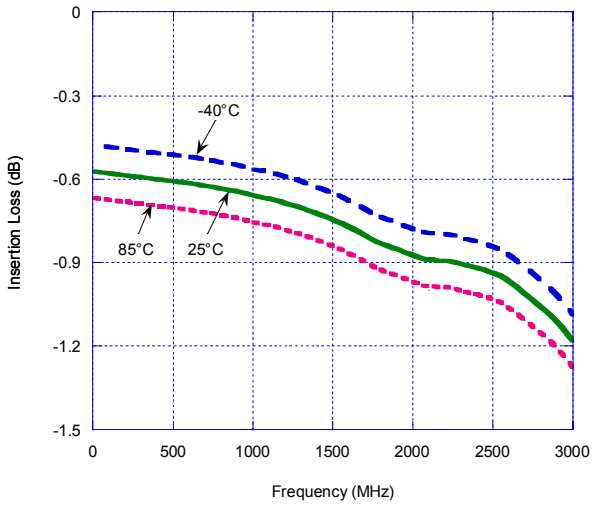


Figure 5. Input 1 dB Compression Point & IIP3 (Typical performance @ 25 °C)

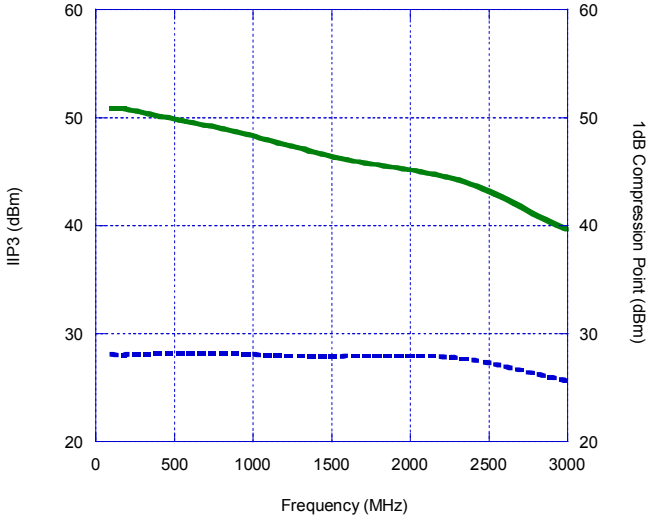


Figure 6. Insertion Loss – RFC to RF2

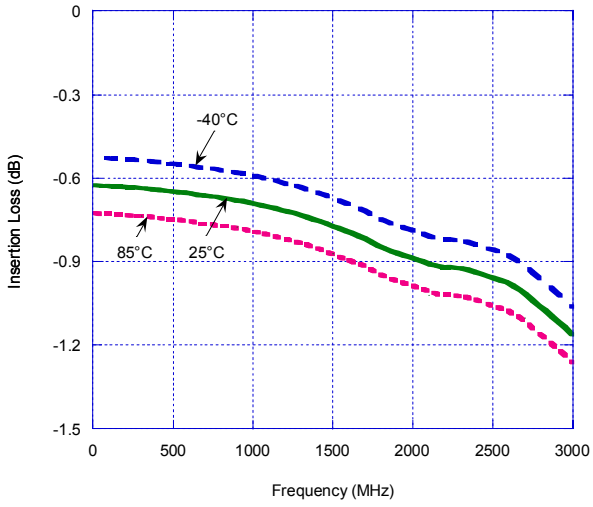
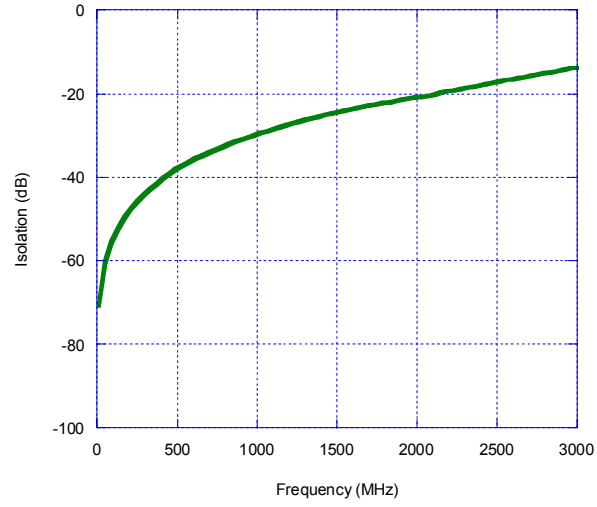


Figure 7. Isolation – RFC to RF1



Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 8. Isolation – RFC to RF2

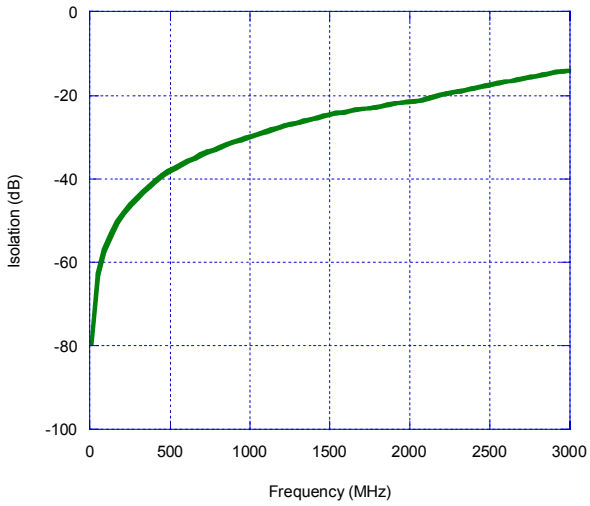


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

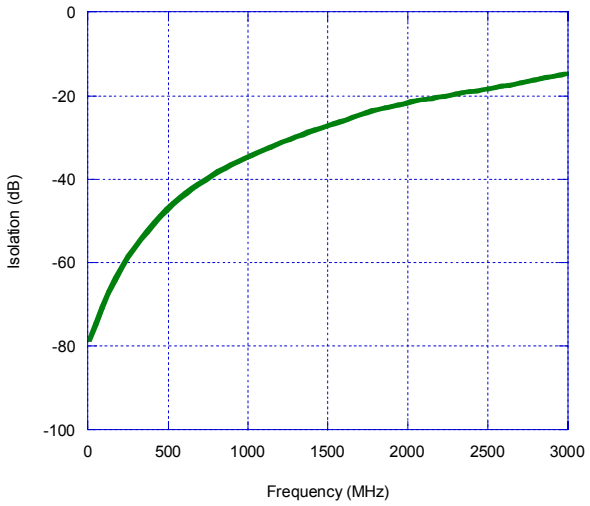


Figure 10. Return Loss – RFC to RF1, RF2

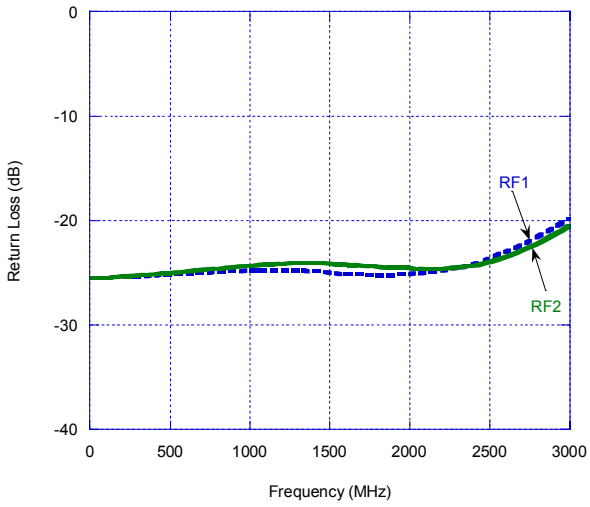
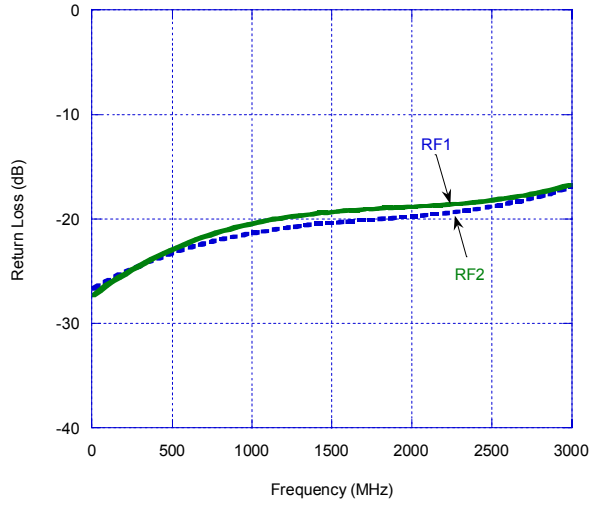


Figure 11. Return Loss – RF1, RF2



Evaluation Kit Information

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4243 SPDT switch. The RF common port is connected through a 50Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J2, respectively. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device V1 or CNTL input. The fourth pin to the right (J6-7) is connected to the device V2 or $\overline{\text{CNTL}}/V_{DD}$ input.

Figure 12. Evaluation Board Layouts

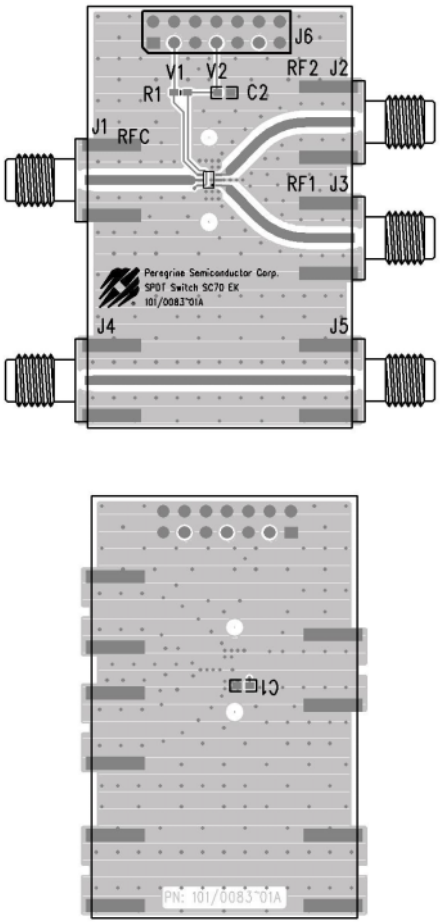


Figure 13. Evaluation Board Schematic

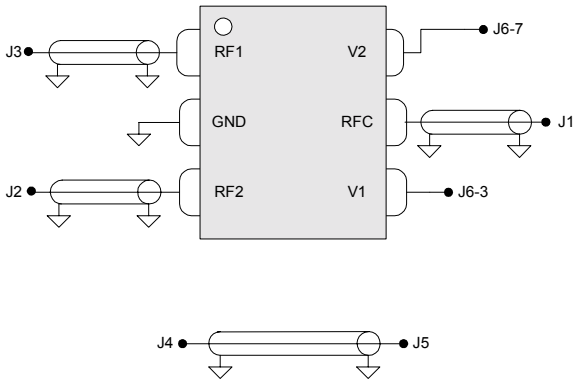
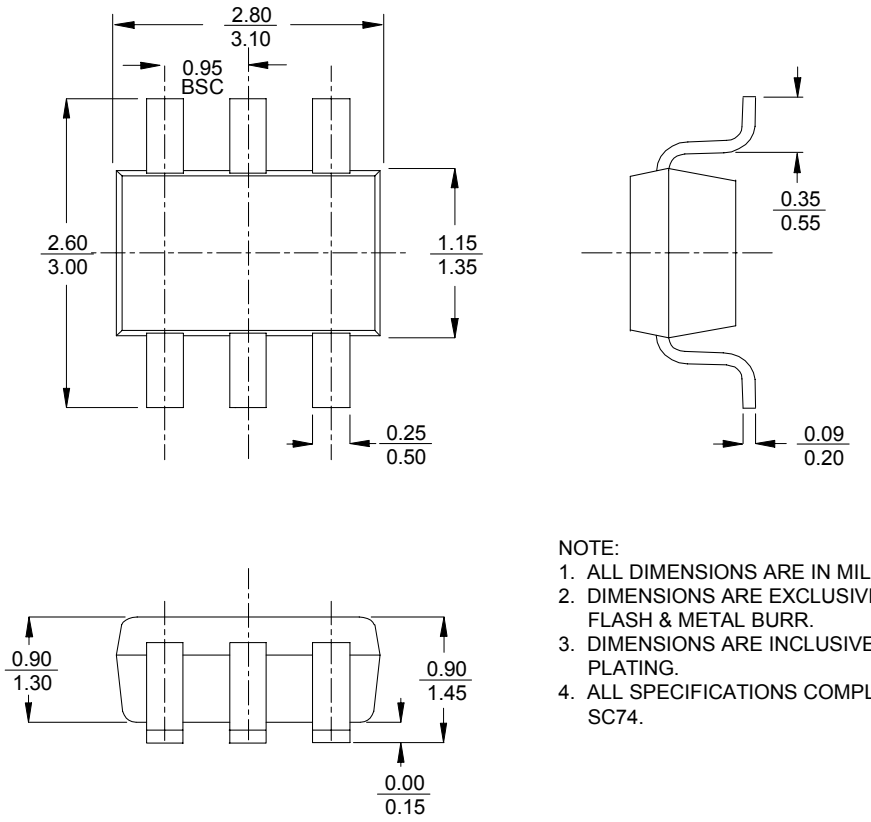


Figure 14. Package Drawing

6-lead SOT23



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
3. DIMENSIONS ARE INCLUSIVE OF SOLDER PLATING.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC74.

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4243-01	4243	PE4243-06SOT23-7680F	6-lead SOT23	7680 units / Canister
4243-02	4243	PE4243-06SOT23-3000C	6-lead SOT23	3000 units / T&R
4243-00	PE4243-EK	PE4243-06SOT23-EK	Evaluation Kit	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.