PRELIMINARY SPECIFICATION

PE4259

SPDT MOSFET RF Switch DC – 3.0GHz

Features

- Single-pin or complementary CMOS logic control inputs
- Low insertion loss: 0.3 dB at 1.0 GHz, 0.45 dB at 2.0 GHz
- Isolation of 32 dB at 1.0 GHz, 23 dB at 2.0 GHz
- Typical input 1 dB compression point of +34 dBm
- Ultra-small SC-70 package

Product Description

The PE4259 MOSFET RF Switch is designed to cover a broad range of applications from DC through 3.0 GHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a typical input 1 dB compression point of +34 dBm can be achieved.

The PE4259 MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

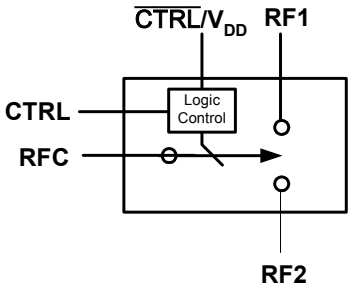


Figure 2. Pin Configuration

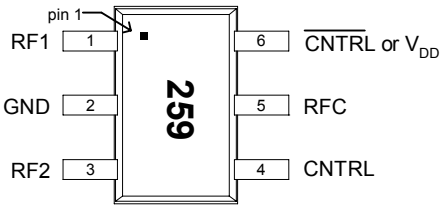


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		3000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.30 0.45		dB dB
Isolation	1000 MHz 2000 MHz		32 23		dB dB
Return Loss	1000 MHz 2000 MHz		20 18		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB of final value, 1 GHz		300		ns
'OFF' Switching Time	50% CTRL to 25 dB isolation, 1 GHz		200		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	2000 MHz		34		dBm
Input IP3	2000 MHz, 14 dBm input power		60		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF1 port (Note 1)
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF2 port (Note 1)
4	CTRL	Switch control input, CMOS logic level.
5	RFC	Common RF port for switch (Note 1)
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options: 1) *Single-pin control mode*. A nominal 3-volt supply connection is required. 2) *Complementary-pin control mode*. A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

Note 1: All RF pins must be DC blocked with an external series capacitor or held at $0V_{DC}$.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		35	dBm
V_{ESD}	ESD voltage (Human Body Model)		1500	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		8		µA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. Single-Pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 = V_{DD} CTRL = High	RFC to RF1
Pin 6 = V_{DD} CTRL = Low	RFC to RF2

Table 6. Complementary-Pin Control Logic Truth Table

Control Voltages	Signal Path
$\overline{CTRL}$ = Low CTRL = High	RFC to RF1
$\overline{CTRL}$ = High CTRL = Low	RFC to RF2

Control Logic Input

The PE4259 is a very versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CNTL and $\overline{CNTL}$ (pins 4 & 6), that can be directly driven by +3-volt CMOS logic or a suitable μProcessor I/O port. This enables the PE4259 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4259 operating limits.

Typical Performance Data @ +25°C

Figure 3. Insertion Loss

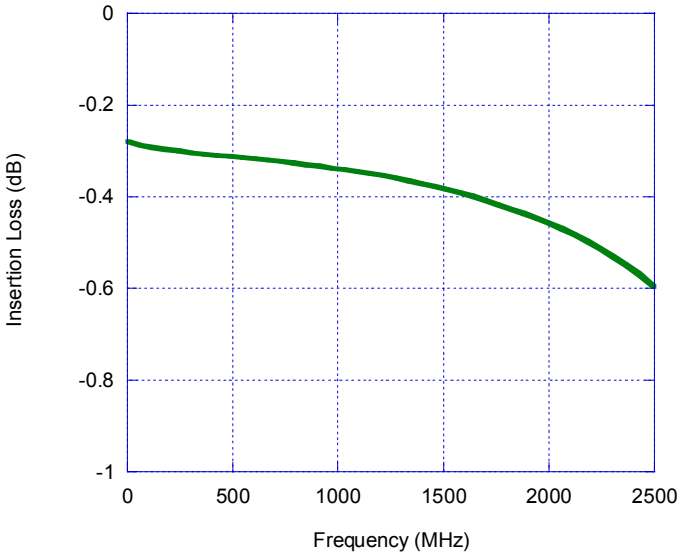


Figure 4. Isolation – Input to Output

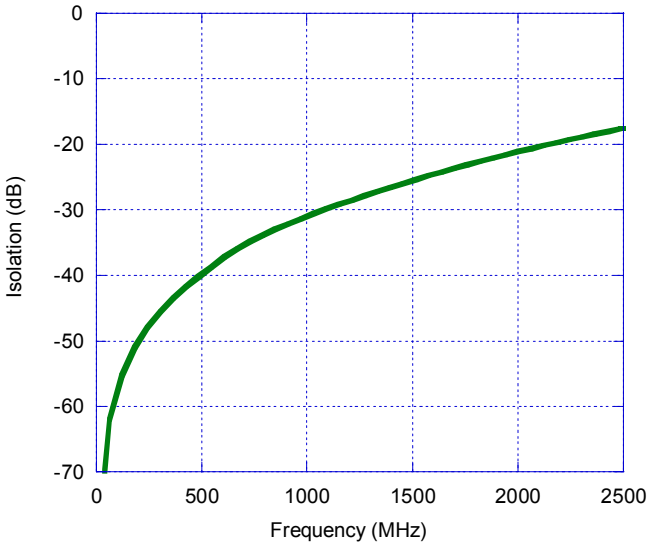


Figure 5. Isolation – Output to Output

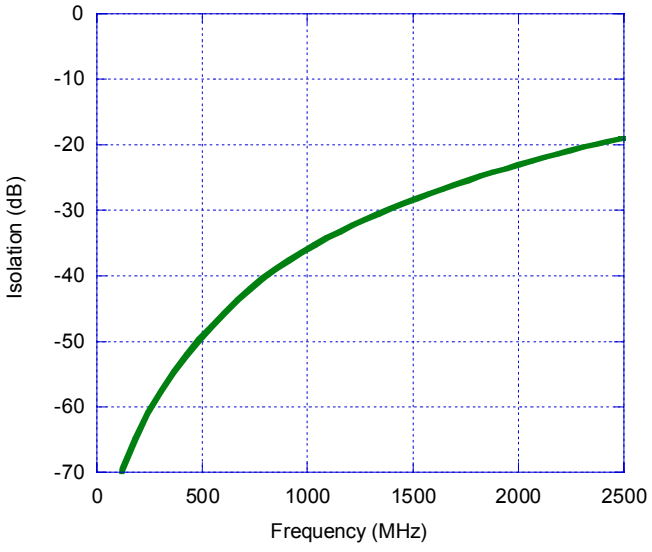
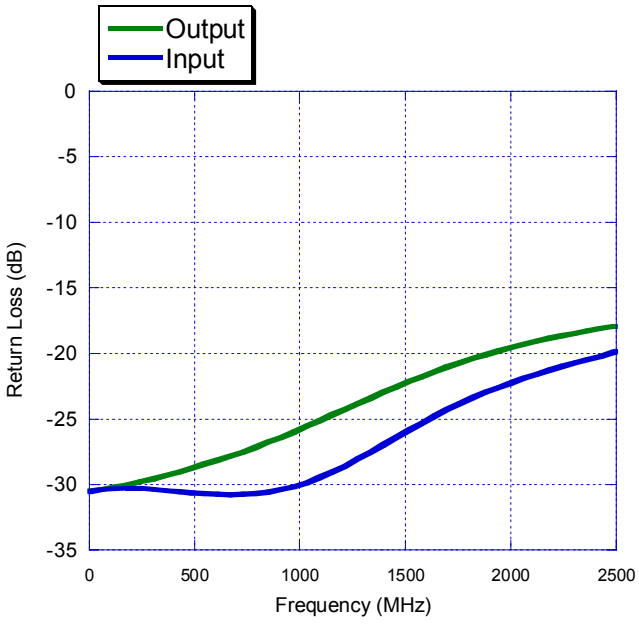


Figure 6. Return Loss



Evaluation Kit Information

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4259 SPDT switch. The RF common port is connected through a 50Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50Ω transmission lines to the two SMA connectors J3 and J2, respectively. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device VDD or CNTL / input. J7-1 is connected to the device CNTL input.

Figure 9. Evaluation Board Layouts

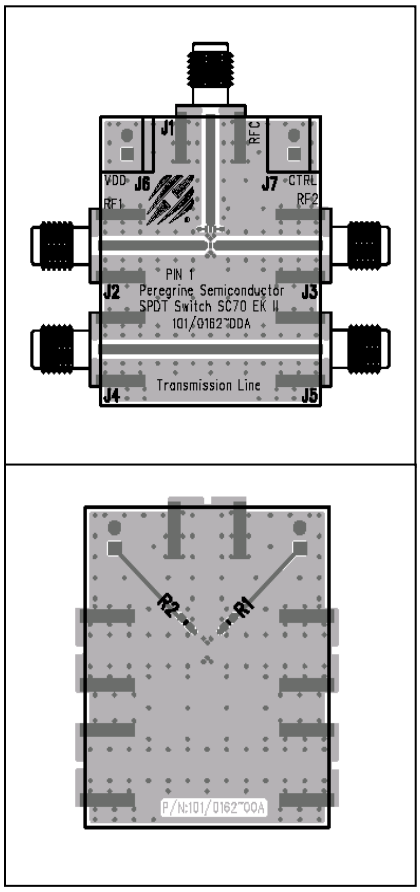


Figure 10. Evaluation Board Schematic

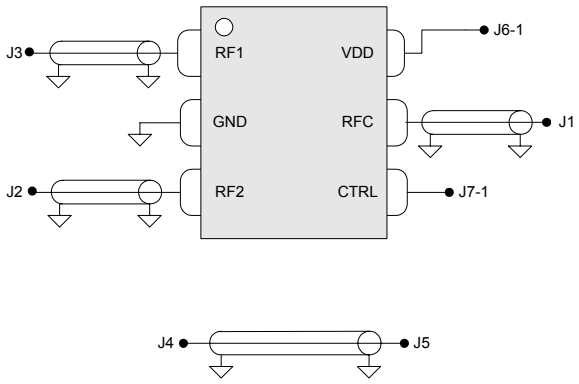


Figure 11. Package Drawing

6-lead SC-70

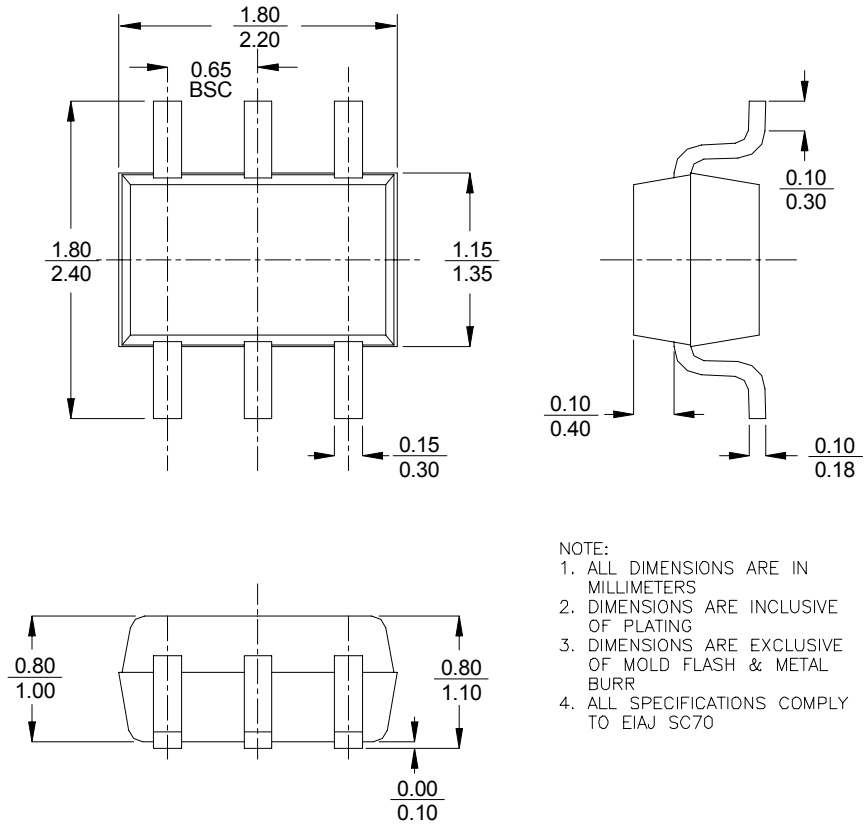


Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4259-01	259	PE4259-06SC70-7680F	6-lead SC-70	7680 units / Canister
4259-02	259	PE4259-06SC70-3000C	6-lead SC-70	3000 units / T&R
4259-00	PE4259-EK	PE4259-06SC70-EK	Evaluation Kit	1 / Box

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel 81-3-3502-5211
Fax 81-3-3502-5213

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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